Control Input Table 1

Table of Control Signals					
		F register		Shift_Out Register	
Major Step	Minor Step	reset	enable	reset	enable
M0	m0	0	0	0	x
	m1	0	0	0	x
	m2	0	0	0	x
	m3	1	0	1	x
M1	m0	0	0	0	1
	m1	0	1	0	x
	m2	0	0	0	1
	m3	0	0	0	x
M2	m0	0	0	0	1
	m1	0	0	0	x
	m2	0	0	0	1
	m3	0	0	0	x
M3	-	0	0	0	x

Control Input Table 1A

Table of Control Signals					
		F register		Shift_Out Register	
Major Step	Minor Step	reset	enable	reset	enable
M0	m0	0	0	0	x(1)
	m1	0	0	0	x(1)
	m2	0	0	0	x(1)
	m3	1	0	1	x(1)
M1	m0	0	0	0	1
	m1	0	1	0	x(1)
	m2	0	0	0	1
	m3	0	0	0	x(1)
M2	m0	0	0	0	1
	m1	0	0	0	x(1)
	m2	0	0	0	1
	m3	0	0	0	x(1)
M3	-	0	0	0	x(1)

Control Input Table 2

Table of Control Signals					
		Register File			
Major Step	Minor Step	write	addra	addrb	addrc
M0	m0	1	x	x	1
	m1	1	x	x	2
	m2	1	x	x	3
	m3	0	x	x	x
M1	m0	0	x	2	x
	m1	1 if shift_out	1	3	1
	m2	1	x	1	1
	m3	1	x	2	2
M2	m0	0	x	2	x
	m1	1 if shift_out	1	3	1
	m2	1	x	1	1
	m3	1	x	2	2
M3	-	0	1	2	x

Control Input Table 2A

Table of Control Signals					
		Register File			
Major Step	Minor Step	write	addra	addrb	addrc
M0	m0	1	x(1)	x(2)	1
	m1	1	x(1)	x(3)	2
	m2	1	x(1)	x(1)	3
	m3	0	x(1)	x(2)	x(2)
M1	m0	0	x(1)	2	x(1)
	m1	1 if shift_out	1	3	1
	m2	1	x(1)	1	1
	m3	1	x(1)	2	2
M2	m0	0	x(1)	2	x(1)
	m1	1 if shift_out	1	3	1
	m2	1	x(1)	1	1
	m3	1	x(1)	2	2
M3	-	0	1	2	x(1)

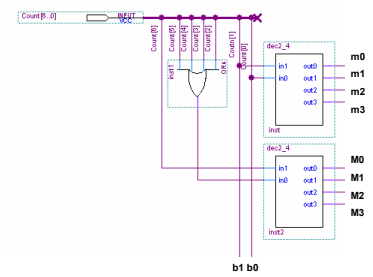
Control Input Table 3

Table of Control Signals					
		ALU		Shifter	4-1 Mux
Major Step	Minor Step	Op	Add/Sub	sel	sel
M0	m0	x	x	x	0
	m1	x	x	x	0
	m2	x	x	x	0
	m3	x	x	x	x
M1	m0	x	x	1100	x
	m1	0	0	0001	1
	m2	x	x	1111	2
	m3	x	x	1100	2
M2	m0	x	x	1100	x
	m1	0	1	0001	1
	m2	x	x	1000	2
	m3	x	x	1100	2
M3	-	x	x	x	x

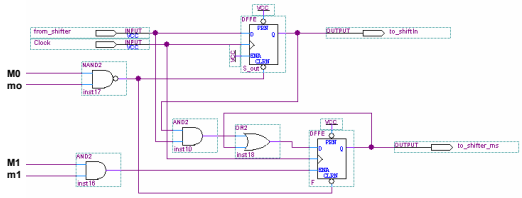
Control Input Table 3A

Table of Control Signals					
		ALU		Shifter	4-1 Mux
Major Step	Minor Step	Op	Add/Sub	sel	sel
M0	m0	x(0)	x(0)	x(1100)	0
	m1	x(0)	x(0)	x(0001)	0
	m2	x(0)	x(0)	x(1111)	0
	m3	x(0)	x(0)	x(1100)	x(2)
M1	m0	x(0)	x(0)	1100	x(0)
	m1	0	0	0001	1
	m2	x(0)	x(0)	1111	2
	m3	x(0)	x(0)	1100	2
M2	m0	x(0)	x(0)	1100	x(0)
	m1	0	1	0001	1
	m2	x(0)	x(0)	1111	2
	m3	x(0)	x(0)	1100	2
M3	-	x(0)	x(0)	x(1100)	x(0)

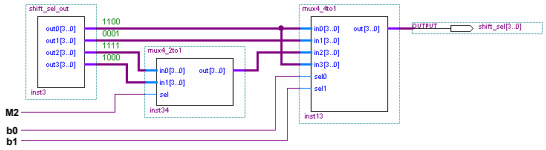
Initial Decode Logic



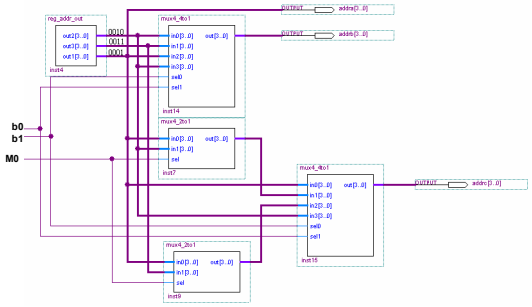
Shift_out and F Registers



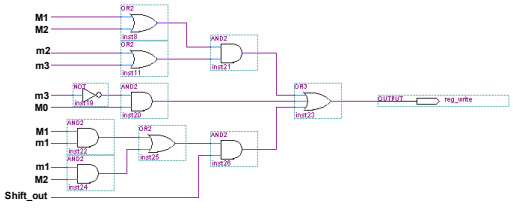
Shift Select



Regfile addra, addrb, addrc



Reg_write Logic



B-invert, Alu_sel, and mux_sel