Cpr E 381 Homework 12

1. Problem 8.1 Here are two different I/O systems intended for use in transaction processing:
   - System A can support 1500 I/O operations per second.
   - System B can support 1000 I/O operations per second.

   The systems use the same processor that executes 500 million instructins per second. Assume that each transaction requires 5 I/O operations and that each I/O operation requires 10,000 instructions. Ignoring response time and assuming that transactions can be arbitrarily overlapped, what is the maximum transaction-per-second rate that each machine can sustain?

2. Problem 8.3 Suppose we want to use a laptop to send 100 files of approximately 40MB each to another computer over a 5 Mbit/sec wireless connection. The laptop battery currently holds 100,000 joules of energy. The wireless networking card alone consumes 5 watts while transmitting, while the rest of the laptop always consumes 35 watts. Before each file transfer we need 10 seconds to choose which file to send. How many complete files can we transfer before the laptop's battery runs down to zero?

3. Problem 8.4 Consider the laptop's hard disk power consumption in Exercise 8.3. Assume that it no longer is constant, but varies between 6 watts when it is spinning and 1 watt when it is not spinning. The power consumed by the laptop apart from the hard disk and wireless card is a constant 32 watts. Suppose that the hard disk's transfer rate is 50MB/sec, it's delay before it can begin transfer is 20 ms, and at all other times it does not spin. How many complete files can we transfer before the latop's battery runs down to zero? How much energy would we need to send all 100 files? (Consider that the wireless card cannot send data until it is in memory.)

4. Problem 8.12 A secret agency simultaneously monitors 100 cellular phone connections and multiplexes the data onto a network with a bandwidth of 5 MB/sec and an overhead latency of 150 us per 1 KB message. Calculate the transmission time per message and determine whether there is sufficient bandwidth to support the application. Assume that the phone conversation data consists of 2 bytes sampled at a rate of 4 KHz.

5. Problem 8.18 Suppose we have a system with the following characteristics:
   1. A memory and bus system supporting block access of 4 or 16 32-bit words.
   2. A 64-bit synchronous bus clocked at 200 MHz, with each 64-bit transfer taking 1 clock cycle, and 1 clock cycle required to send an address to memory.
   3. Two clock cycles needed between each bus operation. (Assume the bus is idle before an access.)
   4. A memory access time for the first four words of 200 ns; each additional set of four words can be read in 20 ns.

   Assume that the bus and memory systems described above are used to handle disk accesses from disks like the one described in the example on page 570. If the I/O is allowed to consume 100% of the bus and memory bandwidth, what is the maximum number of simultaneous disk transfers that can be sustained for the two block sizes?

6. Problem 8.27 We want to compare the maximum bandwidth for a synchronous and an asynchronous bus. The synchronous bus has a clock cycle time of 50 ns, and each bus transmission takes 1 clock cycle. The asynchronous bus requires 40 ns per handshake. The data portion of both buses is 32 bits wide. Find the bandwidth for each bus when performing one-word reads from a 200-ns memory.

7. Problem 8.29 Let's determine the impact of polling overhead for three different devices. Assume that the number of clock cycles for a polling operation – including transferring to the polling routine, accessing the device, and restarting the user program – is 400 and that the processor executes with a 500 MHz clock.

   Determine the fraction of CPU time consumed for the following three cases, assuming that you poll often enough so that no data is ever lost and assuming that the devices are potentially always busy:

   1. The mouse must be polled 30 times per second to ensure that we don not miss any movement made by the user.
   2. The floppy disk transfers data to the processor in 16-bit units and has a data rate of 50KB/sec. No data transfer can be missed.
   3. The hard disk transfers data in four-word chunks and can transfer at 4MB/sec. Again, no transfer can be missed.

8. Problem 8.39 Suppose we have the same hard disk and processor we used in Exercise 8.18, but we use interrupt-driven I/O. The overhead for each transfer, including the interrupt, is 500 clock cycles. Find the fraction of the processor consumed if the hard disk is only transferring data 5% of the time.

9. Problem 8.40 Suppose we have the same processor and hard disk as in Exercise 8.18. Assume that the initial setup of a DMA transfer takes 1000 clock cycles for the processor, and assume the handling of the interrupt at DMA completion requires 500 clock cycles for the processor. The hard disk has a transfer rate of 4MB/sec and uses DMA. If the average transfer from the disk is 8KB, what fraction of the 500-MHz processor is consumed if the disk is actively running 100% of the time? Ignore any impact from bus contention between the processor and DMA controller.

10. Problem 8.46 In order to perform a disk or network access, it is typically necessary for the user to have the operating system communicate with the disk or network controllers. Suppose that in a particular 5GHz computer, it takes 10,000 cycles to trap to the OS, 20 ms for the OS to perform a disk access, and 25 us for the OS to perform a network access. In a disk access, what percentage of the delay time is spent trapping to the OS? How about in a network access?