Homework 8

Part 1 Multicycle datapath problems

1. Problem 5.32 We wish to add the instruction lui (load upper immediate) described in Chapter 3 to the multicycle datapath described in this chapter. Use the same structure of the multicycle datapath of Figure 5.28 on page 323 and show the necessary modifications to the finite state machine of Figure 5.38 on page 339. You may find it helpful to examine the execution steps shown on pages 325 through 329 and consider the steps that will need to be performed to execute the new instruction. How many cycles are required to implement this instruction?

2. Problem 5.33 You are asked to modify the implementation of lui in Exercise 5.32 (previous problem) in order to cut the execution time by 1 cycle. Add any necessary datapaths and control signals to the multicycle datapath of Figure 5.28 on page 323. You can photocopy existing figures to make it easier to show your modifications. You have to maintain the assumption that you don't know what the instruction is before the end of state 1 (end of second cycle). Please explicitly state how many cycles it takes to execute the new instruction on your modified datapath and finite state machine.

3. Problem 5.35 Consider a change to the multiple-cycle implementation that alters the register file so that it has only one read port. Describe (via a diagram) any additional changes that will need to be made to the datapath in order to support this modification. Modify the finite state machine to indicate how the instructions will work, given your new datapath.

4. Problem 5.37 Your friends at C^3 (Creative Computer Corporation) have determined that the critical path that sets the clock cycle length o f the multicycle datapath is memory access for loads and stores (not for fetching instructions). This has caused their newest implementation of the MIPS 30000 to run at a clock rate of 4.8 GHz rather than the target clock rate of 5.6 Hz. However, Clara at C^3 has a solution. If all cycles that access memory are broken into two clock cycles, then the machine can run at its target clock rate.

   Using the SPEC CPUint 2000 mixes shown in Chapter 3 (Figure 3.26 on page 228), determine how much faster the machine with the two-cycle memory accesses is compared with the 4.8 GHz machine with the single-cycle memory access. Assume that all jumps and branches take the same number of cycles and that the set instructions and arithmetic immediate instructions are implemented ast R-type instructions. Would you consider the further step of splitting instruction fetch into two cycles if it would raise the clock rate to 6.4 GHz? Why?

5. Problem 5.46 Show how the jump register instruction (described on pages 76 and A-64) can be implemented simply by making changes to the finite state machine of Figure 5.37 on page 338. (It may help you to remember that $0 = $zero = 0.)

Part 2 Propose your on Instruction Set Architecture

Propose an instruction set architecture that you will implement for your final project

1. Select a datapath size for your machine (8-bit, 16-bit, 32-bit etc.).
2. Provide a list of all instructions you will implement. You may base your design on a subset of an existing architecture, or design your own. It must still be complete; meaning instructions left out must be able to be represented by sequences of implemented instructions (not necessarily efficiently).
3. Show the format of all instruction types
    a. Group the instructions into types
    b. Determine opcodes
    c. Determine register file size, immediate size etc.
4. Show the encoding for each instruction

Please submit this part separately.