CPRE 381 Lab 1
Review of Verilog – Combinational Logic

In this lab you will review basic verilog syntax to create several basic combinational devices. Use the Quartus II environment tutorial as a reference.

Part 1 – Structural and Behavioral Syntax

1. Draw the gate level diagram for a 2-to-1 multiplexor along with its truth table.
2. Implement a 2-to-1 multiplexor module in verilog using a structural description.
3. Implement a 2-to-1 multiplexor module in verilog using a behavioral description.
4. Simulate the two modules and verify their functionality against the truth table.
5. Implement an 8x2-to-1 multiplexor (selection between two 8bit buses) using a behavioral description.
6. Simulate and verify the 8x2-to-1 multiplexor.

Part 2 – Additional Practice

1. Draw the gate level diagrams for a 4-to-2 encoder (with an additional signal indicating if the encoding is valid, i.e. at least one of the four inputs is nonzero) and a 2-to-4 decoder with their truth tables (you may include don't care conditions).
2. Implement both the 4-to-2 encoder and 2-to-4 decoder in verilog with either a behavioral or structural description.
3. Simulate your two modules and verify their functionality against the truth tables.

Part 3 – Module reuse

1. Construct a 4-to-1 multiplexor by reusing instances of the 2-to-1 multiplexor.
2. Construct an 8-to-1 multiplexor using instances of both the 4-to-1 multiplexor and the 2-to-1 multiplexor.
3. Construct a 16-to-4 encoder and a 3-to-8 decoder using only instances of the 4-to-2 encoder and 2-to-4 decoder.
4. Simulate and verify the functionality of the devices.

Final check: All of these designs should be implemented as combinational logic only. Please verify using the log file in Quartus II that no registers were used in any of your designs. If you find that a register is used, please fix your implementation.