CPRE 381 Lab 2
Library of Parameterized Modules – Memory

RAM modules are very regular structures and have specialized implementations that can be instantiated directly within Quartus II when synthesizing for an FPGA. In this lab you will learn a little about the Library of Parameterized Modules, and specifically, the memory module.

Part 1 – Instantiating an LPM

1. Search the help in Quartus II and look for LPM.
2. Determine how to create an instance of LPM_RAM.
3. Create a verilog design for a RAM module containing 1024 entries 32-bits wide.
4. In the simulation environment ensure that every entry can be written to and read from. (Hint – This would be tedious to enter each address and data value by hand. Read the simulation tutorial if you need help automatically entering a large number of values. You will also need to increase the simulation time to accommodate the large number of simulation points.)

Part 2 – Initializing the memory and copying

1. The LPM_RAM module can have its contents initialized by a file. Read the directions on how to do this.
2. Construct a verilog module that has two RAM modules, the output of one connected to the input of the other.
3. Set up a simulation environment to initialize the first RAM module from a file and then copy its contents to the second in reverse order during the run of the simulation.

Final check: Check the log file. How many registers are used for the RAM? Can you explain this?