Cpr E 381 Lab 9
Data Forwarding and Hazard Detection in a Pipelined Datapath

In previous labs you developed single-cycle and multi-cycle datapaths. The multi-cycle implementation increased the efficiency of the design over the single-cycle implementation. Pipelining is a further enhancement that ideally utilizes all of the components of the datapath on every cycle. However, pipelining has the potential to incur problems when certain instructions appear in close proximity. These problems are hazards that require additional control logic to manage. In this lab you will develop two control components that address data forwarding and hazard detection in a pipelined processor.

Data Forwarding

1. Design a forwarding unit using only combinational logic:

FORWARD (IDEXRA1, IDEXRA2, EXMEMWA, MEMWBWA, EXMEMWRF, MEMWBWRF, IDEXRD1, IDEXRD2, EXMEMWD, MEMWBWD, ALUIND1, ALUIND2).

Variable	Meaning
IDEXRA1, IDEXRA2	INPUT: 4-bit addresses of registers being read from register file
IDEXRD1, EDEXRD2	INPUT: 16-bit values that are the contents of the registers read
EXMEMWA, MEMWBWA	INPUT: 4-bit addresses of the registers that could be written by the instructions by the execute and memory stages
EXMEMWD, MEMWBWD	INPUT: 16-bit data values to be written to the register file by the execute and memory stages
EXMEMWRF, MEMWBWRF	INPUT: 1-bit control signal that indicates whether the execute and memory stages will write to the register file
ALUIND1, ALUIND2	OUTPUT: 16-bit values ALU stage must use for actual computation (either the forwarded values, or the values read from the register file)

2. Test your forwarding unit and demonstrate that the unit properly handles forwarding from both the execution stage and the memory stage to either operand of the ALU. Also show that when forwarding is not needed, the unit properly passes the values from the register file to the ALU.

Hazard Detection

1. Design a hazard detection module using only combinational logic:

HAZARD (IDEXMR, IDEXWA, IFIDRA1, IFIDRA2, IFIDWE, INHINC, NOP)

IDEXMR	INPUT: 1-bit indicator if instruction in ID/EX is a memory read
IDEXWA	INPUT: 4-bit register address the ID/EX inst is writing
IFIDRA1, IFIDRA2	INPUT: Two 4-bit register addresses being read in ID stage
IFIDWE	OUTPUT: 1-bit value enabling writing to the IF/ID register by IF
INHINC	OUTPUT: 1-bit signal inhibiting the incrementing of the PC
NOP	OUTPUT: 1-bit MUX control choosing the control bits into the ID/EX reg

Note: All three outputs should be 1 if a hazard is detected and 0 otherwise. The three names indicate which part of the datapath they control.

2. Test your hazard detection unit for all hazard conditions as well as cases that do not introduce hazards.