Datapath & Control Design

- We will design a simplified MIPS processor
- The instructions supported are
  - memory-reference instructions: `lw, sw`
  - arithmetic-logical instructions: `add, sub, and, or, slt`
  - control flow instructions: `beq, j`
- Generic Implementation:
  - use the program counter (PC) to supply instruction address
  - get the instruction from memory
  - read registers
  - use the instruction to decide exactly what to do
- All instructions use the ALU after reading the registers

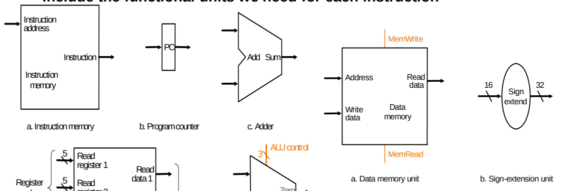
  Why? memory-reference? arithmetic? control flow?

What blocks we need

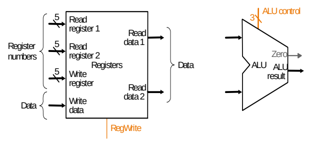
- We need an ALU
  - We have already designed that
- We need memory to store inst and data
  - Instruction memory takes address and supplies inst
  - Data memory takes address and supply data for lw
  - Data memory takes address and data and write into memory
- We need to manage a PC and its update mechanism
- We need a register file to include 32 registers
  - We read two operands and write a result back in register file
- Some times part of the operand comes from instruction
- We may add support of immediate class of instructions
- We may add support for J, JR, JAL

Simple Implementation

- Include the functional units we need for each instruction



a. Instruction memory b. Program counter c. Adder a. Data memory unit b. Sign-extension unit

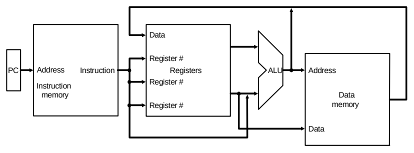


a. Registers b. ALU

Why do we need this stuff?

More Implementation Details

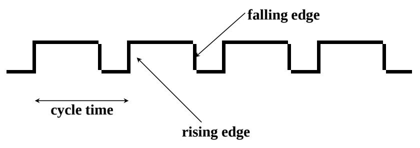
- Abstract / Simplified View:



- Two types of functional units:
  - elements that operate on data values (combinational)
    - Example: ALU
  - elements that contain state (sequential)
    - Examples: Program and Data memory, Register File

Managing State Elements

- Unclocked vs. Clocked
- Clocks used in synchronous logic
  - when should an element that contains state be updated?

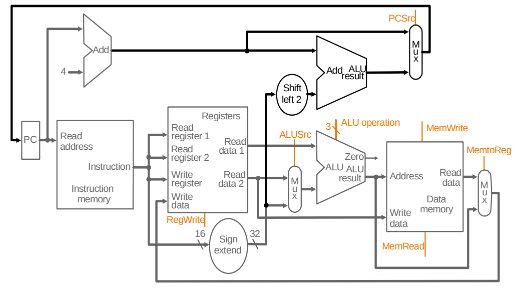


MIPS Instruction Format

31 26	25 21	20 16	15 11	10 6	5 0
LW	REG 1	REG 2	LOAD ADDRESS		OFFSET
SW	REG 1	REG 2	STORE ADDRESS		OFFSET
BEQ/BNE/J	REG 1	REG 2	BRANCH ADDRESS		OFFSET
R-TYPE	REG 1	REG 2	DST	SHIFT AMOUNT	ADD/AND/OR/SLT
I-TYPE	REG 1	REG 2	IMMEDIATE DATA		
JUMP	JUMP			ADDRESS	

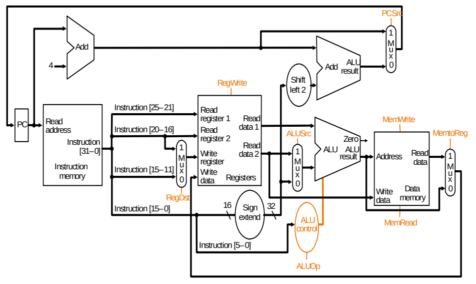
Building the Datapath

- Use multiplexors to stitch them together



A Complete Datapath for R-Type Instructions

- Lw, Sw, Add, Sub, And, Or, Slt can be performed
- For j (jump) we need an additional multiplexor



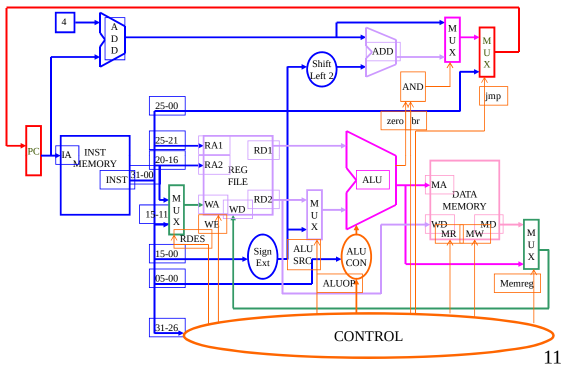
What Else is Needed in Data Path

- Support for j and jr
  - For both of them PC value need to come from somewhere else
  - For J, PC is created by 4 bits (31:28) from old PC, 26 bits from IR (27:2) and 2 bits are zero (1:0)
  - For JR, PC value comes from a register
- Support for JAL
  - Address is same as for J inst
  - OLD PC needs to be saved in register 31
- And what about immediate operand instructions
  - Second operand from instruction, but without shifting
- Support for other instructions like lw and immediate inst write

Operation for Each Instruction

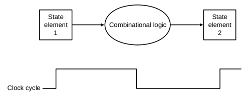
LW:	SW:	R/I/S-Type:	BR-Type:	JMP-Type:
1. READ INST	1. READ INST	1. READ INST	1. READ INST	1. READ INST
2. READ REG 1 *READ REG 2*	2. READ REG 1 READ REG 2	2. READ REG 1 READ REG 2	2. READ REG 1 READ REG 2	2.
3. ADD REG 1 + OFFSET	3. ADD REG 1 + OFFSET	3. OPERATE on REG 1 / REG 2	3. SUB REG 2 from REG 1	3.
4. READ MEM	4. WRITE MEM	4.	4.	4.
5. WRITE REG2	5.	5. WRITE DST	5.	5.

Data Path Operation



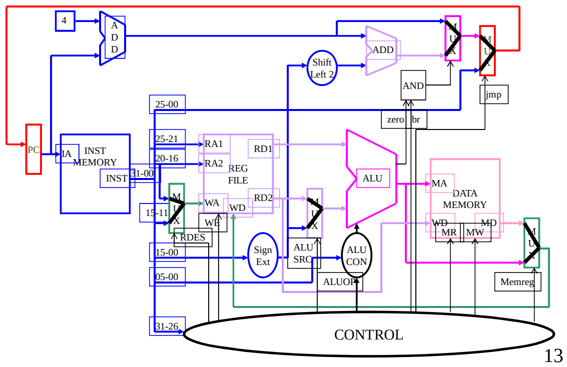
Our Simple Control Structure

- All of the logic is combinational
- We wait for everything to settle down, and the right thing to be done
  - ALU might not produce “right answer” right away
  - we use write signals along with clock to determine when to write
- Cycle time determined by length of the longest path

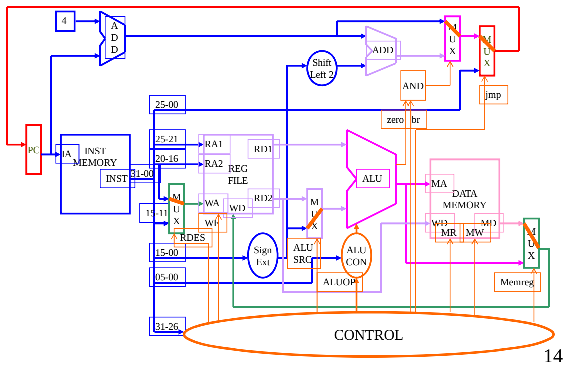


We are ignoring some details like setup and hold times

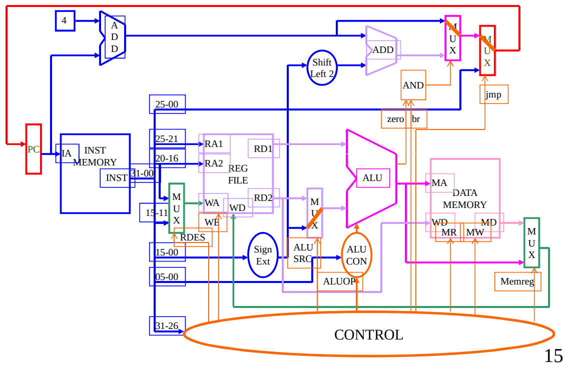
Control Points



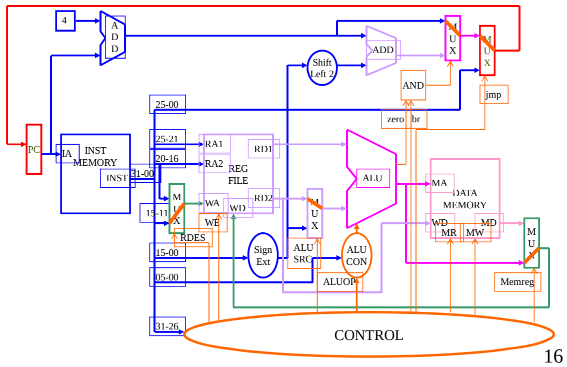
LW Instruction Operation



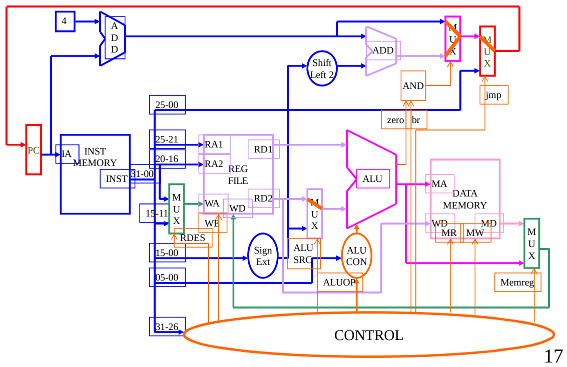
SW Instruction Operation



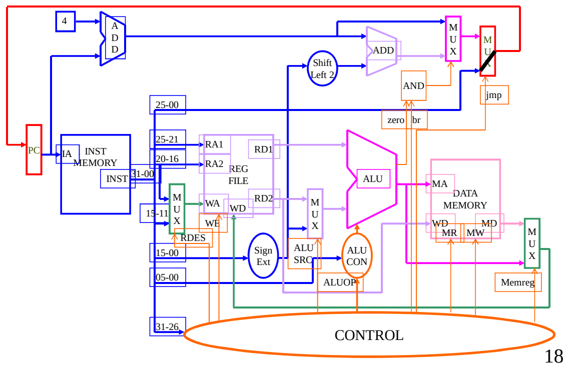
R-Type Instruction Operation



BR-Instruction Operation



Jump Instruction Operation



Control

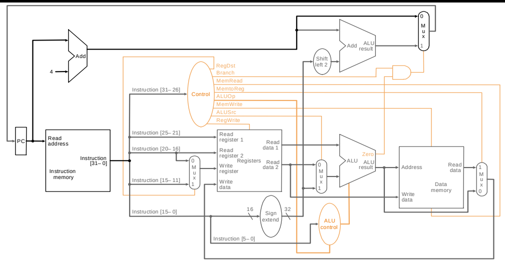
- For each instruction
  - Select the registers to be read (always read two)
  - Select the 2nd ALU input
  - Select the operation to be performed by ALU
  - Select if data memory is to be read or written
  - Select what is written and where in the register file
  - Select what goes in PC
- Information comes from the 32 bits of the instruction
- Example:

  add $8, $17, $18   Instruction Format:

000000	10001	10010	01000	00000	100000

op	rs	rt	rd	shamt	funct

Adding Control to DataPath



Instruction	RegDst	ALUSrc	Memto-Reg	Reg Write	Mem Read	Mem Write	Branch	ALUOp1	ALUp0
R-format	1	0	0	1	0	0	0	1	0
lw	0	1	1	1	1	0	0	0	0
sw	X	1	X	0	0	1	0	0	0
beq	X	0	X	0	0	0	1	0	1

ALU Control

- ALU's operation based on instruction type and function code
  - e.g., what should the ALU do with any instruction
- Example: lw $1, 100($2)
-

35	2	1	100

op	rs	rt	16 bit offset

- ALU control input

```
000     AND
001     OR
010     add
110     subtract
111     set-on-less-than
```

- Why is the code for subtract 110 and not 011?

Other Control Information

- Must describe hardware to compute 3-bit ALU conrol input
  - given instruction type

    00 = lw, sw

    01 = beq,

    10 = arithmetic

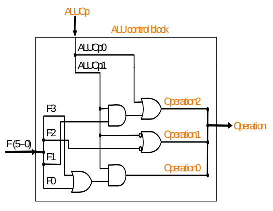
    11 = Jump

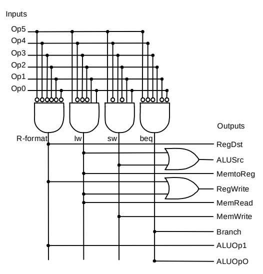
    ALUOp computed from instruction type
  - function code for arithmetic
- Control can be described using a truth table:

ALUOp		Funct field						Operation
ALUOp1	ALUOp0	F5	F4	F3	F2	F1	F0	
0	0	X	X	X	X	X	X	010
X	1	X	X	X	X	X	X	110
1	X	X	X	0	0	0	0	010
1	X	X	X	0	0	1	0	110
1	X	X	X	0	1	0	0	000
1	X	X	X	0	1	0	1	001
1	X	X	X	1	0	1	0	111

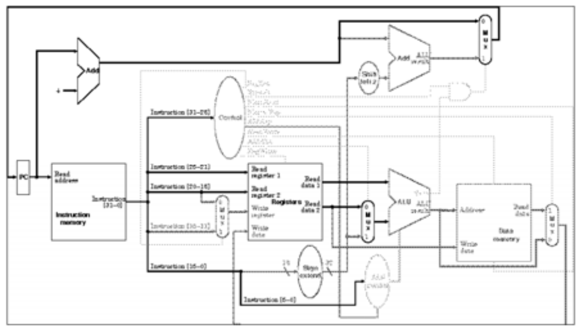
Implementation of Control

- Simple combinational logic to realize the truth tables

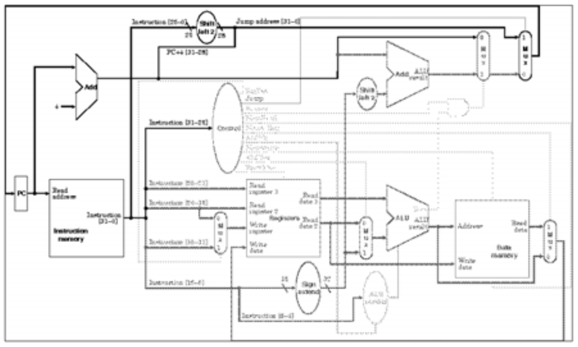




A Complete Datapath with Control



Datapath with Control and Jump Instruction



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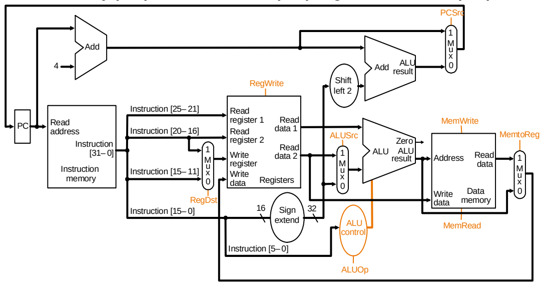
Timing: Single Cycle Implementation

- Calculate cycle time assuming negligible delays except:
  - memory (2ns), ALU and adders (2ns), register file access (1ns)



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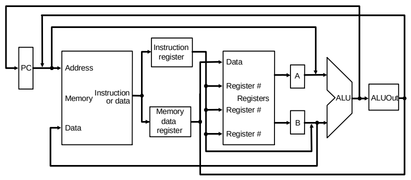
Where we are headed

- Design a data path for our machine specified in the next 3 slides
- Single Cycle Problems:
  - what if we had a more complicated instruction like floating point?
  - wasteful of area
- One Solution:
  - use a “smaller” cycle time and use different numbers of cycles for each instruction using a “multicycle” datapath:



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Machine Specification

- 16-bit data path (can be 4, 8, 12, 16, 24, 32)
- 16-bit instruction (can be any number of them)
- 16-bit PC (can be 16, 24, 32 bits)
- 16 registers (can be 1, 4, 8, 16, 32)
- With m register, log m bits for each register
- Offset depends on expected offset from registers
- Branch offset depends on expected jump address
- Many compromise are made based on number of bits in instruction

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Instruction

- LW R2, #v(R1) ; Load memory from address (R1) + v
- SW R2, #v(R1) ; Store memory to address (R1) + v
- R-Type – OPER R3, R2, R1 ; Perform R3 ← R2 OP R1
  - Five operations ADD, AND, OR, SLT, SUB
- I-Type – OPER R2, R1, V ; Perform R2 ← R1 OP V
  - Four operation ADDI, ANDI, ORI, SLTI
- B-Type – BC R2, R1, V; Branch if condition met to address PC+V
  - Two operation BNE, BEQ
- Shift class – SHIFT TYPE R2, R1 ; Shift R1 of type and result to R2
  - One operation
- Jump Class -- JAL and JR (JAL can be used for Jump)
  - What are th implications of J vs JAL
  - Two instructions

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Instruction bits needed

- LW/SW/BC – Requires opcode, R2, R1, and V values
- R-Type – Requires opcode, R3, R2, and R1 values
- I-Type – Requires opcode, R2, R1, and V values
- Shift class – Requires opcode, R2, R1, and shift type value
- JAL requires opcode and jump address
- JR requires opcode and register address
- Opcode – can be fixed number or variable number of bits
- Register address – 4 bits if 16 registers
- How many bits in V?
- How many bits in shift type?
  - 4 for 16 types, assume one bit shift at a time
- How many bits in jump address?

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