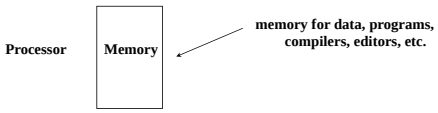
Stored Program Concept

- Instructions are bits
- Programs are stored in memory
  — to be read or written just like data
- 

- Fetch & Execute Cycle
  - Instructions are fetched and put into a special register
  - Bits in the register "control" the subsequent actions
  - Fetch the “next” instruction and continue

Instructions:

- Language of the Machine
- More primitive than higher level languages
  e.g., no sophisticated control flow
- Very restrictive
  e.g., MIPS Arithmetic Instructions
- We’ll be working with the MIPS instruction set architecture
  - similar to other architectures developed since the 1980's
  - used by NEC, Nintendo, Silicon Graphics, Sony

Design goals: maximize performance and minimize cost, reduce design time

Architecture Specification

- Data types:
  - bit, byte, bit field, signed/unsigned integers logical, floating point, character
- Operations:
  - data movement, arithmetic, logical, shift/rotate, conversion, input/output, control, and system calls
- # of operands:
  - 3, 2, 1, or 0 operands
- Registers:
  - integer, floating point, control
- Instruction representation as bit strings

Characteristics of Instruction Set

- Complete
  - Can be used for a variety of application
- Efficient
  - Useful in code generation
- Regular
  - Expected instruction should exist
- Compatible
  - Programs written for previous versions of machines need it
- Primitive
  - Basic operations
- Simple
  - Easy to implement
- Smaller
  - Implementation

Example of multiple operands

- Instructions may have 3, 2, 1, or 0 operands
- Number of operands may affect instruction length
- Operand order is fixed (destination first, but need not that way)

```
add $s0, $s1, $s2      ; Add $s2 and $s1 and store result in $s0

add $s0, $s1           ; Add $s1 and $s0 and store result in $s0

add $s0                ; Add contents of a fixed location to $s0

add                    ; Add two fixed locations and store result
```


Where operands are stored

- Memory locations
  - Instruction include address of location
- Registers
  - Instruction include register number
- Stack location
  - Instruction opcode implies that the operand is in stack
- Fixed register
  - Like accumulator, or depends on inst
  - Hi and Lo register in MIPS
- Fixed location
  - Default operands like interrupt vectors

MIPS arithmetic

- All instructions have 3 operands
- Operand order is fixed (destination first)

Example:

C code: `A = B + C`

MIPS code: `add $s0, $s1, $s2`

(associated with variables by compiler)

MIPS arithmetic

- Design Principle: simplicity favors regularity. Why?
- Of course this complicates some things...

C code:
```
A = B + C + D;
E = F - A;
```

MIPS code:
```
add $t0, $s1, $s2
add $s0, $t0, $s3
sub $s4, $s5, $s0
```

- Operands must be registers, only 32 registers provided
- Design Principle: smaller is faster. Why?
  - More register will slow register file down.

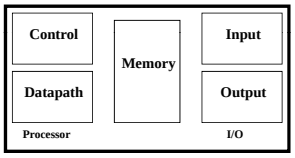
Machine Language

- Instructions, like registers and words of data, are also 32 bits long
  - Example: `add $t0, $s1, $s2`
  - registers have numbers, `$t0=9, $s1=17, $s2=18`
- Instruction Format:

000000	10001	10010	01000	00000	100000
op	rs	rt	rd	shamt	funct

Registers vs. Memory

- Arithmetic instructions operands must be registers,
  — only 32 registers provided
- Compiler associates variables with registers
- What about programs with lots of variables



Memory Organization

- Viewed as a large, single-dimension array, with an address.
- A memory address is an index into the array
- "Byte addressing" means that the index points to a byte of memory.

0	8 bits of data
1	8 bits of data
2	8 bits of data
3	8 bits of data
4	8 bits of data
5	8 bits of data
6	8 bits of data

...

Memory Organization

- Bytes are nice, but most data items use larger "words"
- For MIPS, a word is 32 bits or 4 bytes.

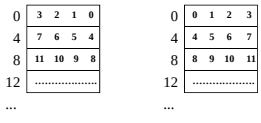
0	32 bits of data
4	32 bits of data
8	32 bits of data
12	32 bits of data

Registers hold 32 bits of data

- 2^{32} bytes with byte addresses from 0 to $2^{32}-1$
- 2^{30} words with byte addresses 0, 4, 8, ... $2^{32}-4$
- Words are aligned
  i.e., what are the least 2 significant bits of a word address?

Addressing within a word

- Each word has four bytes
- Which byte is first and which is last
- Two Choices
  - Least significant byte is byte “0” -> Little Endian
  - Most significant byte is byte “0” -> Big Endian



Addressing

- Memory address for load and store has two parts
  - A register whose content are known
  - An offset stored in 16 bits
- The offset can be positive or negative
  - It is written in terms of number of bytes
  - It is but in instruction in terms of number of words
  - 32 byte offset is written as 32 but stored as 8
- Address is content of register + offset
- All address has both these components
- If no register needs to be used then use register 0
  - Register 0 always stores value 0
- If no offset, then offset is 0

Machine Language

- Consider the load-word and store-word instructions,
  - What would the regularity principle have us do?
  - New principle: Good design demands a compromise
- Introduce a new type of instruction format
  - I-type for data transfer instructions
  - other format was R-type for register
- Example: `lw $t0, 32($s2)`

35	18	9	32

op	rs	rt	16 bit number

- Where's the compromise?

Instructions

- Load and store instructions
- Example:

C code: `A[8] = h + A[8];`

MIPS code:
```
lw $t0, 32($s3)
add $t0, $s2, $t0
sw $t0, 32($s3)
```

- Store word has destination last
- Remember arithmetic operands are registers, not memory!

Our First Example

- Can we figure out the code?

```
swap(int v[], int k);
{ int temp;
     temp = v[k]
     v[k] = v[k+1];
     v[k+1] = temp;
}
```

⇒

```
swap:
     muli $2, $5, 4
     add $2, $4, $2
     lw $15, 0($2)
     lw $16, 4($2)
     sw $16, 0($2)
     sw $15, 4($2)
     jr $31
```


So far we've learned:

- MIPS
  — loading words but addressing bytes
  — arithmetic on registers only
- Instruction / Meaning

```
add $s1, $s2, $s3       $s1 = $s2 + $s3
sub $s1, $s2, $s3       $s1 = $s2 – $s3
lw $s1, 100($s2)        $s1 = Memory[$s2+100]
sw $s1, 100($s2)        Memory[$s2+100] = $s1
```

Control

- Decision making instructions
  - alter the control flow,
  - i.e., change the "next" instruction to be executed
- MIPS conditional branch instructions:

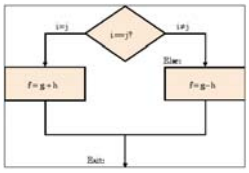
```
bne $t0, $t1, Label
beq $t0, $t1, Label
```

- Example: if (i==j) h = i + j;

```
        bne $s0, $s1, Label
        add $s3, $s0, $s1
Label: ....
```


Conditional Execution

- A simple conditional execution
- Depending on i==j or i!=j, result is different



Instruction Sequencing

- MIPS unconditional branch instructions:

```
j  label
```

- Example:
  f, g, and h are in registers $s3, $s4, and $s5

```
if (i!=j)          beq $s4, $s5, Lab1
    f=g-h;         sub $s3, $s4, $s5
else               j exit
    f=g+h;         Lab1:  add $s3, $s4, $s5
                   exit:  ...
```

- *Can you build a simple for loop?*

Branch Address Handling

- Instructions:

```
bne $t4,$t5,Label    Next instruction is at Label if $t4°$t5
beq $t4,$t5,Label    Next instruction is at Label if $t4=$t5
```

- Formats:

I	op	rs	rt	16 bit address

- Could specify a register (like lw and sw) and add it to address
  - use Instruction Address Register (PC = program counter)
  - most branches are local (principle of locality)
- Jump instructions just use high order bits of PC
  - address boundaries of 256 MB

So far:

- Instruction / Meaning

```
add $s1,$s2,$s3     $s1 = $s2 + $s3
sub $s1,$s2,$s3     $s1 = $s2 – $s3
lw $s1,100($s2)     $s1 = Memory[$s2+100]
sw $s1,100($s2)     Memory[$s2+100] = $s1
bne $s4,$s5,L       Next instr. is at Label if $s4 ° $s5
beq $s4,$s5,L       Next instr. is at Label if $s4 = $s5
j Label             Next instr. is at Label
```

- Formats:

R	op	rs	rt	rd	shamt	funct
I	op	rs	rt	16 bit address		
J	op	26 bit address				

Control Flow

- We have: beq, bne, what about Branch-if-less-than?
- New instruction:

```
                                  if  $s1 < $s2 then
                                     $t0 = 1
      slt $t0, $s1, $s2           else
                                     $t0 = 0
```

- Can use this instruction to build "blt $s1, $s2, Label"
  — can now build general control structures
- Note that the assembler needs a register to do this,
  — there are policy of use conventions for registers

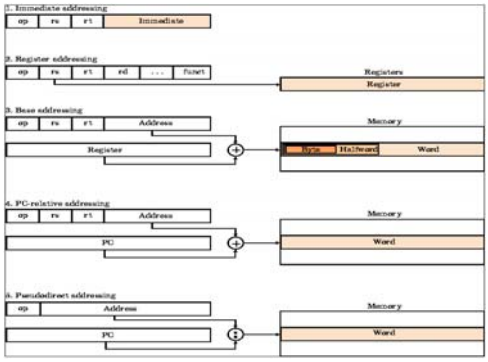
Constants

- Small constants are used quite frequently (50% of operands)
  e.g., A = A + 5;
  B = B + 1;
  C = C - 18;
- Solutions? Why not?
  - put 'typical constants' in memory and load them.
  - create hard-wired registers (like $zero) for constants like one.
- MIPS Instructions:

```
addi $29, $29, 4
slti $8, $18, 10
andi $29, $29, 6
ori $29, $29, 4
```

- How do we make this work?

Various Addressing Modes



To summarize:

MIPS operands

Name	Example	Comments
32 registers	$s0-$s7, $t0-$t9, $zero, $a0-$a3, $v0-$v1, $gp, $fp, $sp, $ra, $at	Fast locations for data. In MIPS, data must be in registers to perform arithmetic. MIPS register $zero always equals 0. Register $at is reserved for the assembler to handle large constants.
2^{30} memory words	Memory[0], Memory[4], ..., Memory[4294967292]	Accessed only by data transfer instructions. MIPS uses byte addresses, so sequential words differ by 4. Memory holds data structures, such as arrays, and spilled registers, such as those saved on procedure calls.

MIPS assembly language

Category	Instruction	Example	Meaning	Comments
Arithmetic	add	add $s1, $s2, $s3	$s1 = $s2 + $s3	Three operands; data in registers
	subtract	sub $s1, $s2, $s3	$s1 = $s2 - $s3	Three operands; data in registers
	add immediate	addi $s1, $s2, 100	$s1 = $s2 + 100	Used to add constants
Data transfer	load word	lw $s1, 100($s2)	$s1 = Memory($s2 + 100)	Word from memory to register
	store word	sw $s1, 100($s2)	Memory($s2 + 100) = $s1	Word from register to memory
	load byte	lb $s1, 100($s2)	$s1 = Memory($s2 + 100)	Byte from memory to register
	store byte	sb $s1, 100($s2)	Memory($s2 + 100) = $s1	Byte from register to memory
	load upper immediate	lui $s1, 100	$s1 = 100 * 2^{16}	Loads constant in upper 16 bits
Conditional branch	branch on equal	beq $s1, $s2, 25	if ($s1 == $s2) go to PC + 4 + 100	Equal test; PC-relative branch
	branch on not equal	bne $s1, $s2, 25	if ($s1 != $s2) go to PC + 4 + 100	Not equal test; PC-relative
	set on less than	slt $s1, $s2, $s3	if ($s2 < $s3) $s1 = 1; else $s1 = 0	Compare less than; for beq, bne
	set less than immediate	slti $s1, $s2, 100	if ($s2 < 100) $s1 = 1; else $s1 = 0	Compare less than constant
Unconditional jump	jump	j 2500	go to 10000	Jump to target address
	jump register	jr $ra	go to $ra	For switch, procedure return
	jump and link	jal 2500	$ra = PC + 4; go to 10000	For procedure call

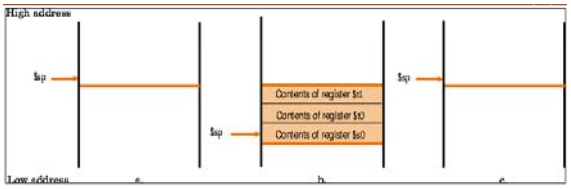
Other Issues

- support for procedures (Refer to section 3.6), stacks, frames, recursion
- manipulating strings and pointers
- linkers, loaders, memory layout
- Interrupts, exceptions, system calls and conventions
- Register use convention

Name	Register number	Usage
$zero	0	the constant value 0
$v0-$v1	2-3	values for results and expression evaluation
$a0-$a3	4-7	arguments
$t0-$t7	8-15	temporaries
$s0-$s7	16-23	saved
$t8-$t9	24-25	more temporaries
$gp	28	global pointer
$sp	29	stack pointer
$fp	30	frame pointer
$ra	31	return address

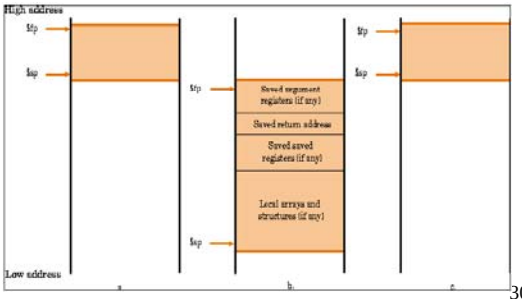
Stack Manipulation

- Register $29 is used as stack pointer
- Stack grows from high address to low address
- Stack pointer should point to the last filled address
- Once entries are removed, stack pointer should be adjusted



Frame Pointer

- Stores the last address for the last frame
- When completing a subroutine, frame address can be used as the starting stack pointer value



How about larger constants?

- We'd like to be able to load a 32 bit constant into a register
- Must use two instructions, new "load upper immediate" instruction

```
lui $t0, 1010101010101010
```

filled with zeros

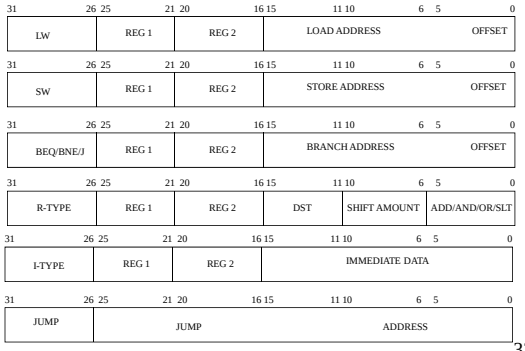
1010101010101010	0000000000000000

- Then must get the lower order bits right, i.e.,

```
ori $t0, $t0, 1010101010101010
```

	1010101010101010	0000000000000000
ori	0000000000000000	1010101010101010
	1010101010101010	1010101010101010

MIPS Instruction Format



Our Example Machine Specification

- 16-bit data path (can be 4, 8, 12, 16, 24, 32)
- 16-bit instruction (can be any number of them)
- 16-bit PC (can be 16, 24, 32 bits)
- 16 registers (can be 1, 4, 8, 16, 32)
- With m register, log m bits for each register
- Offset depends on expected offset from registers
- Branch offset depends on expected jump address
- Many compromise are made based on number of bits in instruction

Instruction

- LW R2, #v(R1) ; Load memory from address (R1) + v
- SW R2, #v(R1) ; Store memory to address (R1) + v
- R-Type – OPER R3, R2, R1 ; Perform R3 ← R2 OP R1
  - Five operations ADD, AND, OR, SLT, SUB
- I-Type – OPER R2, R1, V ; Perform R2 ← R1 OP V
  - Four operation ADDI, ANDI, ORI, SLTI
- B-Type – BC R2, R1, V; Branch if condition met to address PC+V
  - Two operation BNE, BEQ
- Shift class – SHIFT TYPE R2, R1 ; Shift R1 of type and result to R2
  - One operation
- Jump Class -- JAL and JR (JAL can be used for Jump)
  - What are th implications of J vs JAL
  - Two instructions

Instruction Encoding

- LW/SW/BC – Requires opcode, R2, R1, and V values
- R-Type – Requires opcode, R3, R2, and R1 values
- I-Type – Requires opcode, R2, R1, and V values
- Shift class – Requires opcode, R2, R1, and shift type value
- JAL requires opcode and jump address
- JR requires opcode and register address
- Opcode – can be fixed number or variable number of bits
- Register address – 4 bits if 16 registers
- How many bits in V?
- How many bits in shift type?
  - 4 for 16 types, assume one bit shift at a time
- How many bits in jump address?

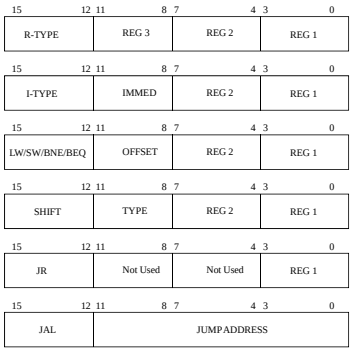
Encoding Selection

- Two fields Opcode
  - Class of function and function in that class, may require more bits as in each class functions needs to be encoded
- One level opcode
  - In our example it is more optimal, 16 op codes are sufficient
- Each register takes 4 bits to encode
- Shift type requires four bits
- To pack instructions in 16 bits
  - V is 4 bits
  - Branch offset 4 bits
  - How many bits in jump address?
    - Only 12 bits jump address required

Trade Offs

- Only 4 bit immediate value
  - It is ok as constants are usually small
- Only 4-bit LW/SW address offset
  - This is real small
  - Good for small programs
- 12-bit jump address
  - Not a real limitation
- Branch offset 4 bits
  - Has constraints, but can be managed with jump
  - Depends on types of program
- Instructions are few
  - It is a quite a complete instruction set
- The instruction set is slightly redundant

Instruction Format



Operation for Each Instruction

LW:	SW:	R/I/S-Type:	BR-Type:	JMP-Type:
1. READ INST	1. READ INST	1. READ INST	1. READ INST	1. READ INST
2. READ REG 1	2. READ REG 1	2. READ REG 1	2. READ REG 1	2.
READ REG 2	READ REG 2	READ REG 2	READ REG 2	
3. ADD REG 1 + OFFSET	3. ADD REG 1 + OFFSET	3. OPERATE on REG 1 & REG 2	3. SUB REG 2 from REG 1	3.
4. READ MEM	4. WRITE MEM	4.	4.	4.
5. WRITE REG2	5.	5. WRITE DST	5.	5.

Alternative Architectures

- Design alternative:
  - provide more powerful operations
  - goal is to reduce number of instructions executed
  - danger is a slower cycle time and/or a higher CPI
- Sometimes referred to as "RISC vs. CISC"
  - virtually all new instruction sets since 1982 have been RISC
  - VAX: minimize code size, make assembly language easy
    instructions from 1 to 54 bytes long!
- We'll look at PowerPC and 80x86

PowerPC

- Indexed addressing
  - example: `lw $t1,$a0+$s3 #$t1=Memory[$a0+$s3]`
  - What do we have to do in MIPS?
- Update addressing
  - update a register as part of load (for marching through arrays)
  - example: `lwu $t0,4($s3) #$t0=Memory[$s3+4];$s3=$s3+4`
  - What do we have to do in MIPS?
- Others:
  - load multiple/store multiple
  - a special counter register "`bc Loop`"
    decrement counter, if not 0 goto loop

80x86

- 1978: The Intel 8086 is announced (16 bit architecture)
- 1980: The 8087 floating point coprocessor is added
- 1982: The 80286 increases address space to 24 bits, +instructions
- 1985: The 80386 extends to 32 bits, new addressing modes
- 1989-1995: The 80486, Pentium, Pentium Pro add a few instructions (mostly designed for higher performance)
- 1997: MMX is added

"This history illustrates the impact of the "golden handcuffs" of compatibility

"adding new features as someone might add clothing to a packed bag"

"an architecture that is difficult to explain and impossible to love"