Performance measures, report, and summarize Make intelligent choices See through the marketing hype Key to understanding underlying organizational motivation				n ere
Airplane Pas	sengers	Range (mi)	Speed (mph)	
Boeing 737-100	101	630	598	
Boeing 747	470	4150		
BAC/Sud Concorde Douglas DC-8-50	132 146	4000 8720	1350 544	







Now that we understand cycles

- A given program will require
 - some number of instructions (machine instructions)
 - some number of cycles
 - some number of seconds
- · We have a vocabulary that relates these quantities:
 - cycle time (seconds per cycle)
 - clock rate (cycles per second)
 - CPI (cycles per instruction)
 - a floating point intensive application might have a higher CPI – MIPS (millions of instructions per second)
 - this would be higher for a program using simple instructions

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Performance

- Performance is determined by execution time
- Do any of the other variables equal performance?
- # of cycles to execute program?
- # of instructions in program?
- # of cycles per second?
- average # of cycles per instruction?
- average # of instructions per second?
- Common pitfall: thinking one of the variables is indicative of performance when it really isn't.

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CPI Example

 Suppose we have two implementations of the same instruction set architecture (ISA).

For some program,

Machine A has a clock cycle time of 10 ns. and a CPI of 2.0 Machine B has a clock cycle time of 20 ns. and a CPI of 1.2

What machine is faster for this program, and by how much?

• If two machines have the same ISA which of our quantities (e.g., clock rate, CPI, execution time, # of instructions, MIPS) will always be identical?

- # of Instructions Example
- A compiler designer is trying to decide between two code sequences for a particular machine. Based on the hardware implementation, there are three different classes of instructions: Class A, Class B, and Class C, and they require one, two, and three cycles (respectively).

The first code sequence has 5 instructions: 2 of A, 1 of B, and 2 of C The second sequence has 6 instructions: 4 of A, 1 of B, and 1 of C.

Which sequence will be faster? How much? What is the CPI for each sequence?

MIPS example

 Two different compilers are being tested for a 100 MHz. machine with three different classes of instructions: Class A, Class B, and Class C, which require one, two, and three cycles (respectively). Both compilers are used to produce code for a large piece of software.

The first compiler's code uses 5 million Class A instructions, 1 million Class B instructions, and 1 million Class C instructions.

The second compiler's code uses 10 million Class A instructions, 1 million Class B instructions, and 1 million Class C instructions.

- Which sequence will be faster according to MIPS?
- Which sequence will be faster according to execution time?

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Benchmarks

- Performance best determined by running a real application
 Use programs typical of expected workload
 - Or, typical of expected class of applications
 - e.g., compilers/editors, scientific applications, graphics, etc.
- Small benchmarks
- nice for architects and designers
- easy to standardize
- can be abused
- SPEC (System Performance Evaluation Cooperative)

 companies have agreed on a set of real program and inputs
 - companies have agreed on a set or real program and inputs
 can still be abused (Intel's "other" bug)
 - valuable indicator of performance (and compiler technology)
 Spec 95 programs
- Spec 2000 programs

Amdahl's Law

Execution Time After Improvement =

Execution Time Unaffected +(Execution Time Affected / Amount of Improvement)

• Example:

"Suppose a program runs in 100 seconds on a machine, with multiply responsible for 80 seconds of this time. How much do we have to improve the speed of multiplication if we want the program to run 4 times faster?"

How about making it 5 times faster?

• Principle: Make the common case fast

Remember

- Performance is specific to a particular program/s
 - Total execution time is a consistent summary of performance
- · For a given architecture performance increases come from:
 - increases in clock rate (without adverse CPI affects)
 - improvements in processor organization that lower CPI
 - compiler enhancements that lower CPI and/or instruction count
- Pitfall: expecting improvement in one aspect of a machine's performance to affect the total performance
- You should not always believe everything you read! Read carefully!
 (see newspaper articles, e.g., Exercise 2.37)

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