

# CprE 488 – Embedded Systems Design

## HW-0: VGA Timing

**Assigned:** Monday of Week 1

**Due:** Friday of Week 1

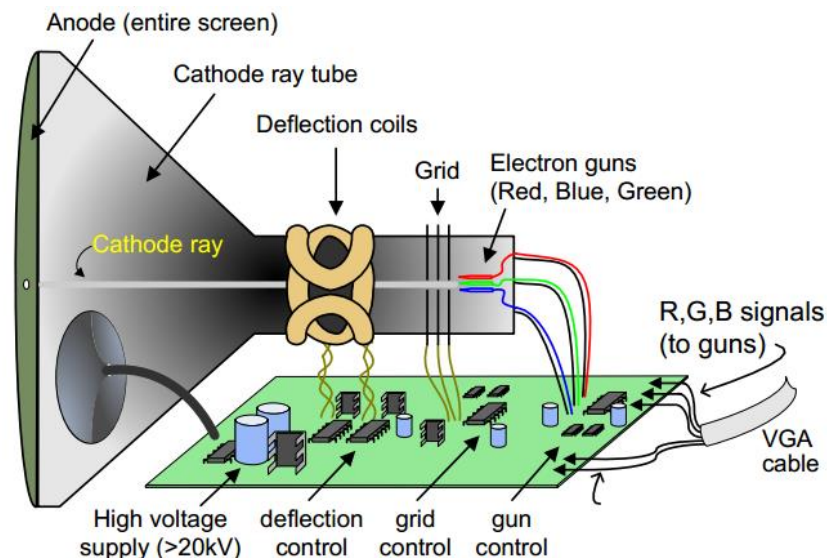
**Points:** 10

**1) Embedded Example.** Write a brief description of an embedded system with which you are familiar, that is separate from one of the examples discussed in class. Explain three ways in which your chosen system fits the definitions of an embedded system presented in Lect-01.

**2) VGA Timing.** Video Graphics Array (VGA) refers to a standard for analog computer display that was first introduced in the late 1980s. While the precise signal timings for driving a VGA display are specified, published, and sold by the VESA organization ([www.vesa.org](http://www.vesa.org)), the Wikipedia article on VGA ([en.wikipedia.org/wiki/Video\\_Graphics\\_Array](http://en.wikipedia.org/wiki/Video_Graphics_Array)) is sufficient for our understanding.

Consider the display on a CRT-based VGA monitor (LCDs use significantly different display technology but the controller circuit is not substantially different). Color CRT displays use three amplitude-modulated moving electron beams (one each for red, blue, and green color intensity) to energize a phosphor coated screen on the display end of the CRT. Between the electron guns and the display surface, the beam passes through the neck of the CRT where magnetic fields are manipulated to cause the rays to traverse the display surface in a “raster” pattern, horizontally from left to right and vertically from top to bottom. As the cathode ray traverses the surface of the display, the current sent to the electron guns can be increased or decreased to change the brightness of the red, blue, and green components at the ray impact point. The figure below (from the excellent Digilent BASYS2 reference manual chapter on this topic:

[https://reference.digilentinc.com/media/basys2:basys2\\_rm.pdf](https://reference.digilentinc.com/media/basys2:basys2_rm.pdf)) illustrates this process.



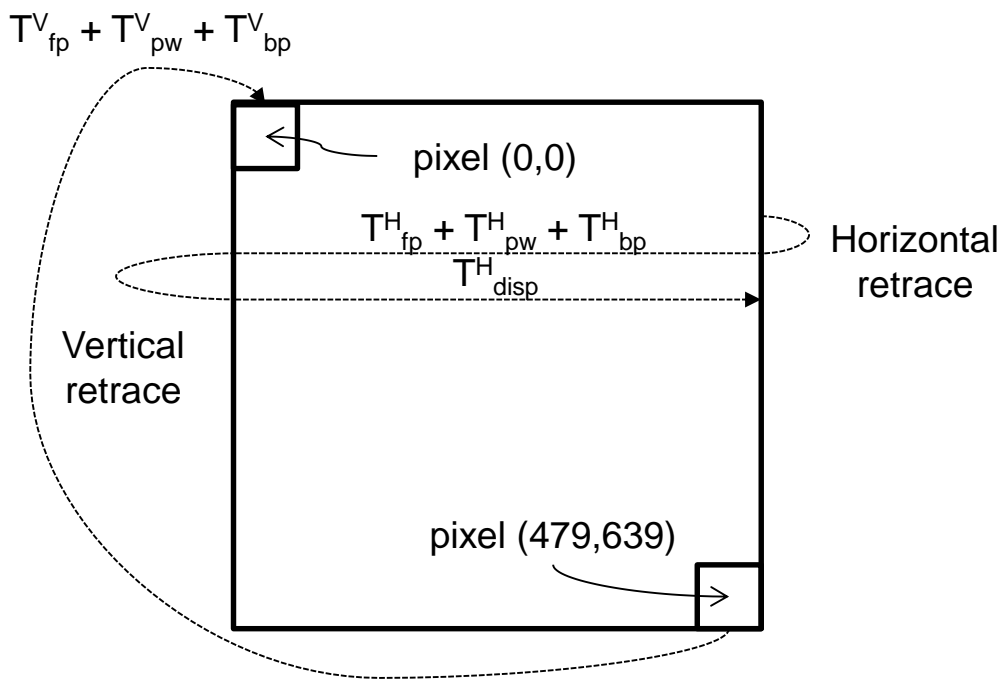
The video data comes from the video framebuffer (or equivalent video refresh region of memory), and the controller must index into this video memory as the beams move across the display. For a 640x480 display, there are several precisely-timed stages for each horizontal scan line displayed during this process:

1. A “front porch”, which provides time for the electron gun to stabilize to the start of the active row:  $T_{fp}$ , during the horizontal blanking / retrace period.
2. A sync pulse that denotes the start of a horizontal row to be displayed:  $T_{pw}$ .
3. A “back porch”, which is the portion of the scan line between the end of the horizontal sync pulse and the start of active video:  $T_{bp}$ .
4. The time it takes to display the 640 pixels in a given row:  $T_{disp}$ .

These stages are illustrated (for a single horizontal line) in the figure below. Taken together, these stages are referred to as the horizontal sync pulse  $T_S$ .



For the vertical scan, there are a corresponding set of stages whose timing is determined by the refresh rate of the display. A simplified version of the VGA display process is represented in the figure below.



For a 640x480 VGA display using a 25 MHz pixel clock, the following horizontal signal timings can be derived. Convert the VGA signal timings to the equivalent number of clock cycles. Briefly explain your reasoning.

Symbol	Parameter	Time	# Clocks
$T_s$	Synchronization time	32 us	
$T_{fp}$	Front porch	640 ns	
$T_{pw}$	Sync pulse width	3.84 us	
$T_{bp}$	Back porch	1.92 us	
$T_{disp}$	Display time	25.6 us	

For a 60 Hz display refresh rate, what would be the appropriate value (as measured in seconds, clocks, and horizontal lines) for the vertical sync time  $T^v_s$ ? Explain your reasoning.