Reconfigurable Computing: Homework 2
(CPRE 583, Fall 2010)
Due: Wed 10/6/2010

1. State machines (5 pts)
    a. Draw a Mealy and Moore statemachine bubble diagram for each the following patterns. Make sure to detect overlapping patterns. For example "0110110" contains two "0110" patterns.
        i. 1110
        ii. 0110

2. VHDL to FPGA implementation example (Still being developed) (60 pts)
    a. Draw a block/schematic diagram for the VHDL given in HW2.vhd (see course webpage) . (10 pts)
        i. For the statemachine portion of the diagram draw the bubble diagram within a box, and show the inputs and outputs to and from the box containing the bubble diagram.

    b. Synthesis the design into D flip-flops, inverters, and two input AND and OR gates. (10pts)

    c. Map the synthesized design to D flip-flops and 3 input LUTs. (10 pts)
        i. Name each LUT that gets allocated A, B, C, … And name each D flip-flop allocated DFF_A, DFF_B, …
        ii. How many LUT and how many D flip-flops did you use.

    d. Place the D flip-flops and LUTs on the FPGA given on the PowerPoint slide that can be found on the course webpage. (10 pts)
        i. Label each placed LUT and D flip-flop using the names from c.)
        ii. Highlight each used component in red.

    e. Route the design. (10 pts)
        i. Highlight all the used routes in red.

    f. Configure the FPGA (10 pts)
        i. Program all the boxes given in the PowerPoint slide. Note: since many will be high impendence (e.g. Z), I've initially filled most in as Z.

3. Looking inside the FPGA (if you are using NX, then make sure to add all the NX font packages or fpga_editor will give a segmentation fault error) (10 pts)
    a. Use fpga_editor to look at the MAPed version of MP1. After starting fpga_editor you will open MP1_top_map.ncd: Look around the design (7 pts)
        i. Identify 4 components. Two should be components that we have talked about little or not at all in class
        ii. Write 1-2 paragraphs about each of the 4 components (use the Virtex 5 user guide to help find information)

    b. Now use fpga_editor to open MP1_top.ncd. This is the post PAR version (3 pts)
        i. What is the main difference between MP1_top_map.ncd, and MP1_top.ncd. Turn on all the display options that the GUI gives to get a feel for the amount of detail that exists within the FPGA.
        ii. Step into one of the slices in the design (double click). Write down the equation for one of the LUTs

4. Trade-offs on reconfiguration granularity. (10 pts)
    a. Give a half to a full page discussion on the trade-offs associated with the size of the granularity used for a reconfiguration fabric.

5. Garp Details (15 pts)
    a. Read "The Garp Architecture and C compiler" year: 2000. This can be found on IEEE Xplorer.

    b. Reducing reconfiguration time
        i. What aspects of the Garp design help mitigate overheads associated with reconfiguration time?
        ii. Why is having a low reconfiguration time important in general?

    c. What implementation aspects of Garp help make multiplying by small constants efficient?

    d. Why is the iteration spacing in Figure 3 of the paper two clock cycles?

    e. In table 2 why does it make sense that strlen of a 1024 char string is accelerated more than strlen of a 16 character string?