Reconfigurable Computing: Homework 3
(CPRE 583, Fall 2010)
Due: Friday 12/17/2010

VHDL to FPGA implementation example

The automated tools used to take a hardware design described in VHDL, and implement the design on an FPGA are very powerful and safe you time. For most, the process of going from VHDL to a working FPGA design is very abstract and may seem like magic. The purpose of this assignment is to give you a concrete feel for what the tools are doing. By the end of this assignment, you should have a much clearer picture of how the tools go from a VHDL description to creating a bitfile that configures an FPGA.

Before starting this assignment become familiar with the following (located on the course page)

- HW3_FPGA.ppt: This is the FPGA you will be targeting for implementing the given VHDL circuit. It is an array of 6x4 (24) 3 input LUTs and D Flip-flops. The routing structure provides nearest neighbor routing, and regional routing resources.

- VHDL_to_FPGA.xise : This project contains the behavioral circuit you will be implementing on the FPGA. It also provides a testbench to help you verify that you performed the synthesis and mapping portion of the implementation flow correctly.

1. Draw a block/schematic diagram for the behavioral VHDL circuit given in the VHDL_to_FPGA ISE project (10 pts.)
    a. For the statemachine portion of the diagram draw the bubble diagram within a box, and show the inputs and outputs to and from the box containing the bubble diagram.

2. Synthesize the behavioral VHDL design from 1). You may only use the following gates: D flip-flops, inverters, 2 input AND and OR gates, 3 input AND and OR gates. (30pts)
    a. Show your K-maps and state transition tables that you use to perform synthesis, as discussed in class.
    b. Draw the synthesized gate-level schematic of the design

3. Map the synthesized design to D flip-flops and 3 input LUTs. (5 pts)
    a. Circle each group of gates that gets mapped to a given LUT. Name each LUT that gets allocated (e.g. A, B, C). Name each D flip-flop allocated (e.g. DFF_A, DFF_B)
    b. How many 3 input LUTs and how many D flip-flops did you use?
        i. Note: I only needed 15 LUTs. If you use 20 or more LUTs, then you are likely being inefficient with how you are mapping LUTs.
        ii. Note: The FPGA you are targeting only has 24 LUTs.

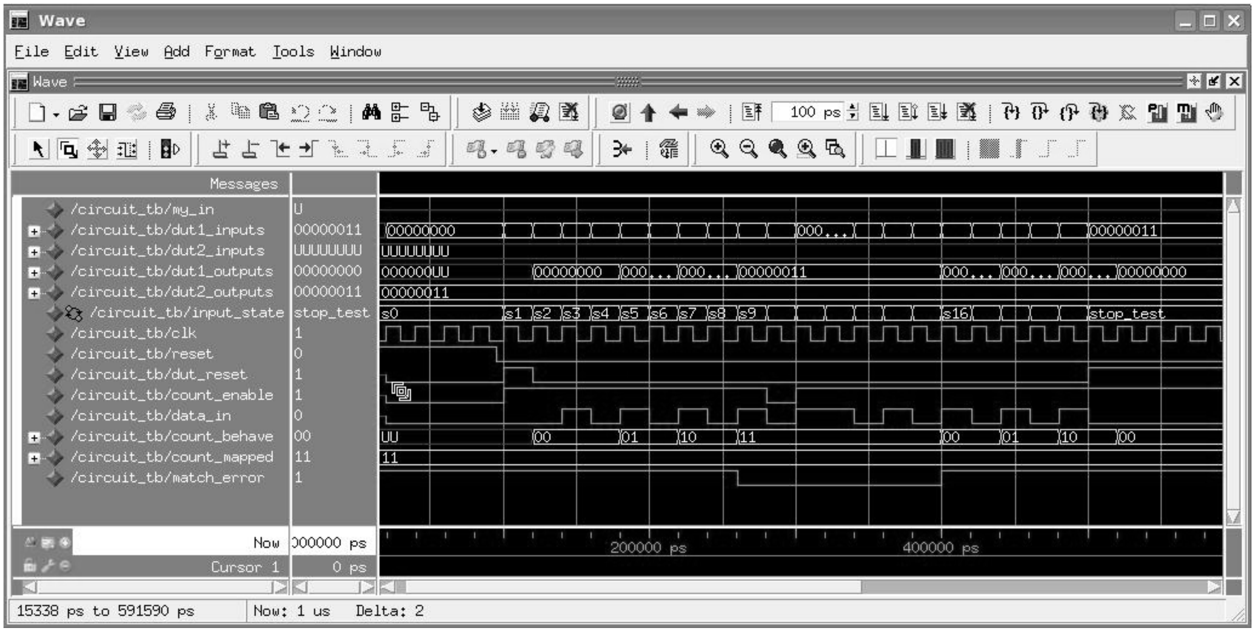
4. Verify your mapped circuit against the original behavioral circuit. (30 pts)
    a. Input your mapped circuit from 3) as purely structural VHDL into to the mapped circuit stub given in the ISE project.
        i. Before starting to implement your mapped circuit, simulate the ISE project as is. The result of simulation should match Figure 1.

b. Next simulate to verify both the original behavioral circuit and your mapped circuit give the exact same behavior. The testbench is setup to given the same exact stimulus to both the behavioral and mapped version of the design. If your mapped circuit is correct, then your simulation should match Figure 2.

5. Place the D flip-flops and LUTs onto the PowerPoint implemented FPGA. Zoom in as needed to view details of the FPGA (5 pts)
   a. Label each placed LUT and D flip-flop using the names from 3)
   b. Highlight each used component in red.

6. Route the design. (10 pts)
   a. Highlight all the used routes (i.e. wires) in red.
   b. Note: For each input to the circuit (i.e. reset, count_enable, data_in) use <u>one</u> open local or regional routing resource input. Highlight and label the three inputs that you choose in red.

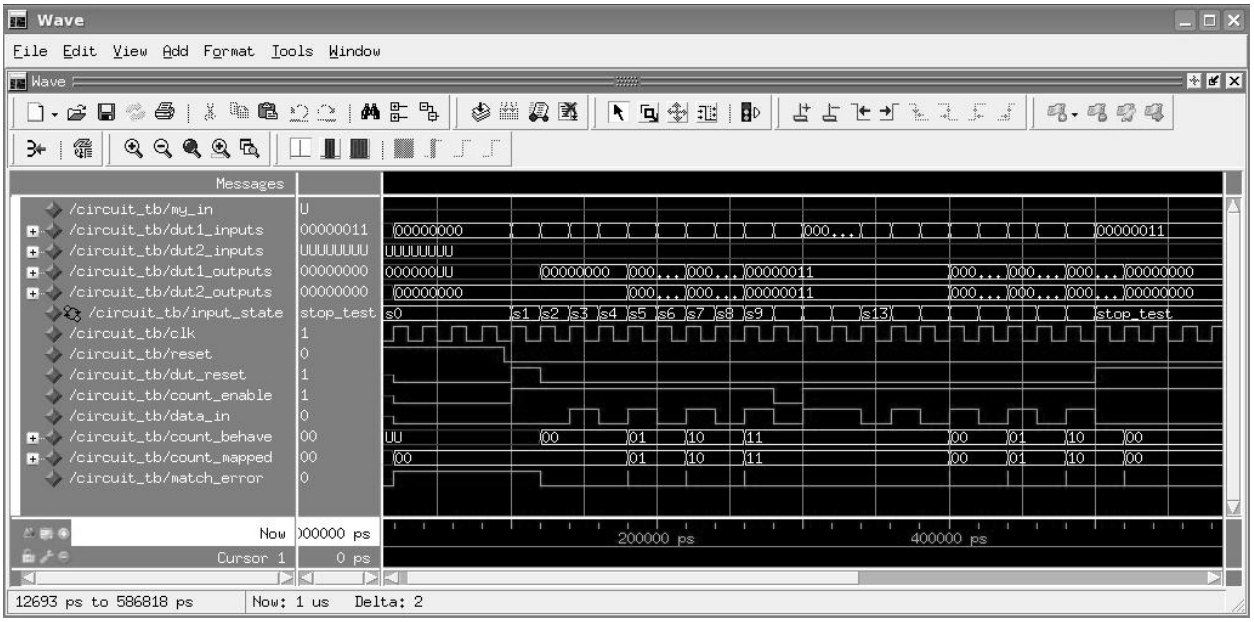
7. Configure the FPGA (10 pts)
   a. Program all of the LUTs and routing resources on the FPGA. The FPGA specifics how to program the routing resources. For programming the LUTs, refer to the 3 input LUTs you created using VHDL in 4).
   b. How large would the bitfile be (in bits) to configure the provided FPGA?



Messages	
/circuit_tb/my_in	U
/circuit_tb/dut1_inputs	00000011
/circuit_tb/dut2_inputs	UUUUUUUU
/circuit_tb/dut1_outputs	00000000
/circuit_tb/dut2_outputs	00000011
/circuit_tb/input_state	stop_test
/circuit_tb/clk	1
/circuit_tb/reset	0
/circuit_tb/dut_reset	1
/circuit_tb/count_enable	1
/circuit_tb/data_in	0
/circuit_tb/count_behave	00
/circuit_tb/count_mapped	11
/circuit_tb/match_error	1
Now	000000 ps
Cursor 1	0 ps

15338 ps to 591590 ps | Now: 1 us | Delta: 2

Figure 1: ISE Project simulation before adding your mapped circuit



Messages	
/circuit_tb/my_in	U
/circuit_tb/dut1_inputs	00000011
/circuit_tb/dut2_inputs	UUUUUUUU
/circuit_tb/dut1_outputs	00000000
/circuit_tb/dut2_outputs	00000000
/circuit_tb/input_state	stop_test
/circuit_tb/clk	1
/circuit_tb/reset	0
/circuit_tb/dut_reset	1
/circuit_tb/count_enable	1
/circuit_tb/data_in	0
/circuit_tb/count_behave	00
/circuit_tb/count_mapped	00
/circuit_tb/match_error	0
Now	)00000 ps
Cursor 1	0 ps

12693 ps to 586818 ps   Now: 1 us   Delta: 2

Figure 2: Expected simulation if the mapped circuit is correct