A Survey of Video Processing with Field Programmable Gate Arrays (FGPA)

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***Abstract*—This paper is a high-level, survey of recent developments in the area of video processing using reconfigurable logic implemented on FPGAs.**

***Index Terms*—Field Programmable Gate Array, FPGA, video, deinterlace, 3-D, quantization, DCT, motion estimation, video tracking.**

FIELD Programmable Gate Arrays are versatile devices. As a result video processing requires significant data bandwidth and processing capability when dealing with analog video sources. Reconfigurable computing systems have been integrated into systems for video processing because of their adaptability and speed. Some tasks that are well-suited for implementation on FPGAs are: video compression, stereo vision for 3-dimensional images, motion estimation within video, object tracking and FPGAs that are dynamically reconfigured for several processing algorithms. This paper gives a high level overview of some of the issues encountered in the video area and approaches that have been implemented on FPGs to handle them.

I. VIDEO COMPRESSION AND DE-INTERLACING

A. Deinterlacing

Interlacement is a scheme for compressing video to achieve reasonably good video quality. This scheme is not suitable for larger screens or for playing videos on computers. As a result, these compressed videos must be managed in a way that allows them to display properly, a method called deinterlacement.

There are numerous different algorithms and techniques that accomplish this same goal. [1] presents a wide choice of deinterlacement algorithms with different complexity, static, and dynamic performances.
The following is an overview of commonly used algorithms.
Weave: This technique recreates full resolution frames by interleaving odd fields with the following even ones. This main issues with this simple approaches are that the frame rate is reduced in half and fast moving video or frames with large changes between do not ”weave” together well (this undesirable effect is known as mouse teeth).

Discard: A simple technique where all of the odd or all of the even fields are discarded.

Blend: The Blend algorithm computes a pixel-by-pixel average between each odd field with the following even field in order to build each frame.

Bob: The best performing algorithm doubles the height of a frame by interpolating the pixels between adjacent rows using their pixel-by-pixel average to build the output frame.

Adaptive Algorithms: Additional algorithms can be implemented on FPGAs to handle fast moving scenes, in addition to static images (as in the previously described algorithms). Motion detection and motion compensation techniques implemented using complex algorithms are required for good performance. Motion detection techniques separate out the static and moving areas of the video in order to use the appropriate algorithm for further processing on the video. Motion compensation techniques follow scene movement more closely. This technique and the associated algorithms achieve excellent results, but computational costs are high.

Implementation: This is a more detailed description of the implement of deinterlacement algorithms on a FPGA device in order to do real-time video analysis and elaboration. The implemented logic performs the following: extract data and synchronization signals, deinterlace using a particular algorithm, and color conversion.

As shown in Figure 1 all four algorithms have been implemented onto a single FPGA. A multiplexer, whose control signals can be driven manually or, an auto motion detector, brings at the output of the system the output from the deinterlacer [1].

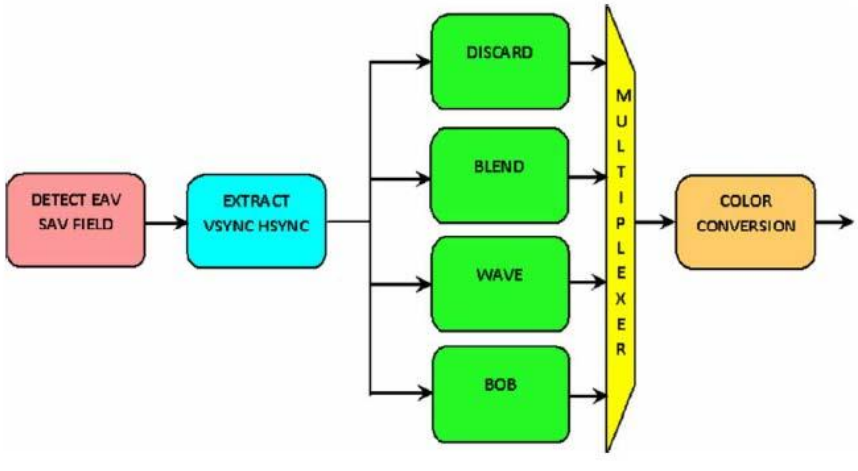

Fig. 1. FPGA schematic for video processing. The FPGA is configured for several different algorithms. [1]

B. Frame Frequency Multiplier for stereo video

A frame frequency multiplier system using a Field Programmable Gate Array (FPGA) can to be used to convert two interlaced NTSC videos from two different cameras into time-sequential progressive stereo (3-dimensional) video. See the system overview in Figure 2. Stereo video provides depth perception and great visual

representation

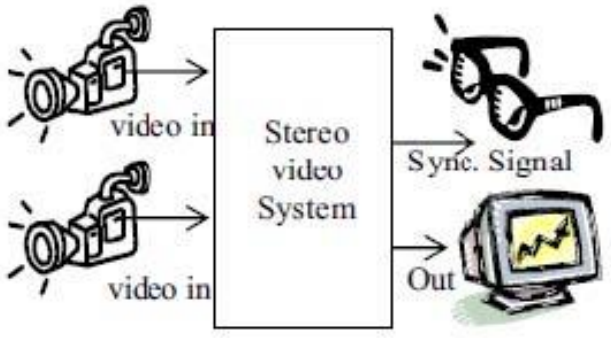

Fig. 2. Setup for stereo video system [4]

In order to do this, stereo video synchronization and control signals are generated from a FPGA-based on Look-Up Tables. Some data required for this generation are the inputs from two video sequences, as well as vertical and horizontal synchronization signals and field index from standard NTSC video. The inputs give reference for the generation of stereo video synchronization signals and control signals. These signals can be used to reassemble the stereo video information and to control video data acquisition and transmission in the system. This approach helps to provide high quality and flicker-free 3-D stereo images [4].

Processing and generation of 3-dimensional data is intensive and dynamic so there are many ways where FPGAs can help to speed up and improve this area.

II. MOTION ESTIMATION

A. Blur identification

Blur identification is critical to processing video when motion blur causes the image quality of the video sequence to degrade.

One approach to handle this issue is by using a dynamically reconfigurable imaging system. By combining several different techniques, such as algorithmic video enhancement, field programmable gate array (FPGA)-based video processing and adaptive image sensor technology, this approach is an effective method of handling blurring proposed and tested a combined blur identification and validation (BIV) scheme.

First, the initial linear and uniform motion assumptions are processed and validated. If these assumptions do not prove to be accurate, a real-time reconfiguration property of an adaptive image sensor is utilized. At this point the FPGA is reconfigured to process the video differently (reduce blur by using larger pixels that generate higher frame-rate samples).

FPGAs, using a BIV architecture, are able to perform dynamic reconfiguration to make use of more applicable processing techniques depending on the type and quality of the input video source [7].

B. Dynamic reconfiguration

In [5] the issue of motion estimation is addressed by using a flexible solution. Motion estimation is one of the most computationally intensive algorithms. The motion estimation logic is implemented on an FPGA. It takes the current-clock and search-region data and returns the results of motion vector computations. The FPGA is an effective component to the system because it can be dynamically adapted in real time to handle different constraints on the system such as video quality and power dissipation [5].

V. CONCLUSION

As you can see FPGAs are used in a variety of aspects of video processing from video compression to motion detection to reduce the effects of blurring for fast moving scenes to handling 3-D video.

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Appendix: Modified tree structure for mini literary survey