This report documents the design, simulation, layout, and post-layout simulation of a fully differential amplifier in the AMI06 process. The final amplifier design has a DC gain of 100dB, UGF of 200MHz, and PM of 50.5 degrees.
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INTRODUCTION

OBJECTIVE

The objective of this lab is to design a two-stage fully differential op-amp. In this process, we will learn how to compensate a differential amplifier, design a stable CMFB circuit to balance the outputs, and optimize the amplifier for various specifications. By the end, we will have an understanding of the fundamental limits in two-stage fully differential op-amp design and compensation.

A secondary objective is to gain experience with layout, specifically differential circuit layout. Post layout simulation will be performed to determine the impact of parasitic capacitance on the frequency response of the amplifier.

BENEFITS OF FULLY DIFFERENTIAL AMPLIFIERS

One of the benefits of a differential amplifier over a signal ended is the cancelation of even-order non-linearities. This is due to the symmetry of differential amplifiers and it can it justified as follows. For the fully differential inverting amplifier in Figure 1 a) let $V_{S1}=V_A$ and $V_{S2}=V_B$ and the resulting $V_{O1}=V_X$ and $V_{O2}=V_Y$. Then,

$$V_{sd} = V_A - V_B \text{ and } V_{ad} = V_X - V_Y$$

Now, if $V_{S1}=V_B$ and $V_{S2}=V_A$ and the resulting $V_{O1}=V_Y$ and $V_{O2}=V_X$ then,

$$V_{sd} = -(V_A - V_B) \text{ and } V_{ad} = -(V_X - V_Y)$$
showing that the output voltage is an odd function. This implies that only odd-order nonlinearities can pass through a differential amplifier (derivation from Gray and Meyer).

Another benefit of using a fully differential amplifier is that the differential output voltage swing range is greater than that of the single ended amplifier. This is demonstrated in Figure 1. For the single-ended output amplifier, the maximum output range is $V_{\text{MAX}}-V_{\text{MIN}}$. In the case of the differential amplifier, each output node can swing from $V_{\text{MAX}}$ to $V_{\text{MIN}}$ allowing a total differential output range of $2(V_{\text{MAX}}-V_{\text{MIN}})$.

Fully differential amplifiers also have the advantage of canceling common mode noise. This is due to the symmetry of the circuit – any common mode noise will be experienced equally at both output terminals and is subtracted when taking the differential signal,

$$V_{\text{OD}} = (V_{O+} + V_{C\text{noise}}) - (V_{O-} + V_{C\text{noise}}) = V_{O+} - V_{O-}$$

Also, because the output swing range is twice that of the single ended output, the signal to noise ratio (SNR) is 2 times as large. Therefore, differential amplifiers have greatly superior noise performance.

For all of these reasons, fully differential amplifiers are becoming more common in modern integrated circuits. The drawbacks are discussed in the next section, but they are less significant than the benefits in most cases.

Figure 1: a) Fully differential and b) single-ended inverting amplifiers (Gray and Meyer)
DRAWBACKS OF FULLY DIFFERENTIAL AMPLIFIERS

The first disadvantage of fully differential amplifiers is that they require two closely matched feedback networks. For the single ended amplifier in Figure 1 a), $R_3$ and $R_1$ should be closely matched to have an accurate closed loop gain. For the fully differential amplifier in Figure 1 b), both pairs of $R_3$ and $R_1$ should be closely matched. Also, $R_3$ should be matched with the other $R_3$ and $R_1$ should be matched with the other $R_1$. This introduces some complexity to layout, but sufficient matching can still be achieved through careful layout.

Another drawback is that these amplifiers require a common mode feedback (CMFB) circuit. Without common mode feedback, the average (DC) voltage at each output node will not be centered at 0V and clipping will cause nonlinearities in the differential output. This is demonstrated in the diagram below.

![Figure 2: Effects of output CM offset](image)

With CMFB, the output is held at zero. This is accomplished by sensing the averaged value of the output voltage and comparing it to zero. Using negative feedback, if the average is larger than zero, the CMFB circuit works to lower the output voltage. Likewise, if the average is less than zero, the CMFB works to increase the output voltage.

DESIGN SPECIFICATIONS

The specifications for the amplifier as given in the project definition are:

- Power supply variation tolerance: ±20%
- Total power consumption of the chip: ≤10mW at ±2.5V supply
- Output driving capability: capacitive load between 0 and 2pF
- Unity gain frequency: ≥ 50MHz
- Phase margin at UFG: ≥ 45°
- Peak DC gain: ≥ 90dB
- $V_{\text{OUT}}$ swing range: includes [-1.75V, +1.75V] at ±2.5V supply
- Input common mode range: ≥ 3V and include [-1V, +1V] at ±2.5V supply
- Systematic differential offset voltage: ≤ 1mV
- Slew rate: ≥100V/μs
- Settling time in 1V step response for unity feedback: ≤ 50ns to ±0.1%
- Overshoot in step response: ≤25%
- CMFB loop stability: PM ≥ 45°
- CMFB loop unity gain bandwidth: ~5 to 10MHz
- CMRR: ≥ 60dB
- PSRR: ≥ 60dB
- Input referred noise voltage: should be considered in design and reported but no specific requirement
- Gain linearity: simulate and report but no specific requirement
- AC response linearity: simulate and report but no specific requirement
  - THD versus frequency and/or versus signal magnitude
  - SFDR versus frequency and/or versus signal magnitude
- Once all specifications are met, focus should be placed on improving UGF

To meet these requirements, a PMOS input fully differential telescopic amplifier will be used for the first stage to drive two NMOS input common source output amplifiers. A differential PMOS input pair is chosen for multiple reasons. First, PMOS transistors have lower 1/f noise because electrons in NMOS transistors are more easily trapped than the holes in PMOS transistors. Also, this configuration allows for the use of NMOS input transistors to the common source output amplifiers. This allows for a larger $g_m$ with smaller parasitic capacitance because the mobility of electrons is greater than holes. This is important for high frequency operation because of the effects on the second pole. A high $g_m$ for the output transistor and low capacitance will tend to move the pole to higher frequencies. This is discussed in greater detail in the amplifier equations section. The amplifier and CMFB circuit are shown in Figure 3 below. Throughout the report, all equations refer to the transistor names give in this schematic.

![Figure 3: Amplifier and CMFB circuit architecture](image-url)
AMPLIFIER EQUATIONS

In order to meet the various specification targets of this design project, it was first important to understand the equations of those parameters. In this section, small signal and large signal analysis is used to derive various key equations relating to the differential amplifier operation.

DC ANALYSIS

In this section, low frequency analysis is used to find the differential mode ($A_{DM}$) and common mode gain ($A_{CM}$). Also, the common mode control gain ($A_{CMC}$) and the gain of the common mode circuit are found. First, the equivalent output resistance of a cascoded transistor pair is given because it is used frequently throughout this section.

CASCODE BENEFITS

Figure 4 gives an equivalent circuit diagram, where the bottom transistor was replaced by its drain to source resistance, $r_{o1}$. Small signal analysis will show that,

$$R_{OUT} = r_{o2}(1 + (g_{mb2} + g_{m2})r_{o1}) \approx r_{o2}r_{o1}g_{m2}$$

This shows that the output resistance is increased by the factor,

$$R_{OUT} = r_{o2}g_{m2} = \frac{2}{\lambda V_{EFF2}} \approx \frac{200}{V_{EFF2}}$$

This is a very large increase in resistance and is used in the first stage of the amplifier to greatly increase the gain.

DIFFERENTIAL MODE DC GAIN

The open-loop DC gain of an op-amp is a critical parameter because it directly impacts the linearity of feedback gain configurations. An op-amp that has a large gain can be connected in a negative feedback configuration with a very linear gain if the feedback gain is much less than the open-loop gain. The differential mode half-circuit is shown in Figure 5 and it can be used to find the gain of the differential circuit. The cascode transistors are not shown here, but are included in the equations by using the equation derived in the last section. The gain of the first stage is the transconductance, $g_{m2}$, times the output resistance. The output resistance is the parallel combinations of the cascode resistances at the output node. That is,

$$R_{OUT1} = g_{m2c}r_{ds2c}r_{ds2}||g_{m4c}r_{ds4c}r_{ds4}$$

and

$$A_{V1} = -g_{m2}(g_{m2c}r_{ds2c}r_{ds2}||g_{m4c}r_{ds4c}r_{ds4})$$
The gain of the second stage is the transconductance, $g_{m6}$, times the output resistance of the second stage. That is,

$$ R_{OUT2} = r_{ds6}||r_{ds7} $$

and

$$ A_{V2} = -g_{m6}(r_{ds6}||r_{ds7}) $$

The total differential mode gain is the product of the gain of each stage,

$$ A_{DM} = g_{m2}g_{m6}(r_{ds6}||r_{ds7})(g_{m2c}r_{ds2c}r_{ds2})(g_{m4c}r_{ds4c}r_{ds4}) $$

![Figure 5: Differential mode half circuit (Gray and Meyer)](image)

In this project, minimum gain specification is 90dB.

### COMMON MODE AND COMMON MODE CONTROL GAIN

The common mode gain of the circuit is important because it is inversely proportional to the common mode rejection ratio (CMRR) for constant differential mode gain. Common mode control gain is in the gain path of the common mode feedback (CMFB) circuit and multiplies the CMFB gain. Therefore, it is a critical parameter when designing the CMFB circuit. Figure 6 show the common mode half-circuit for the op-amp.

The input for the common mode (CM) path is shown as $V_{IC}$. The equation for the gain can be found using small signal analysis and is,

$$ A_{CM} = \left( \frac{1}{r_{ds5h}} \right) \left( g_{m2}g_{m2c}r_{ds2c}r_{ds2}r_{ds5h} || g_{m4c}r_{ds4c}r_{ds4} \right) \left( \frac{g_{m6}}{g_{o6} + g_{o7}} \right) \approx \left( \frac{1}{r_{ds5h}} \right) \left( g_{m4c}r_{ds4c}r_{ds4} \right) \left( \frac{g_{m6}}{g_{o6} + g_{o7}} \right) $$

The input for the common mode control path is the input to the tail current source. It is shown as $M_{5H}$, where the ‘H’ denotes that the transistor is only half of $M_5$. The equation for the gain can be found using small signal analysis and is,

$$ A_{CMC} = \left( g_{m5h}g_{m2}g_{m2c}r_{ds2c}r_{ds2}r_{ds5h} || g_{m4c}r_{ds4c}r_{ds4} \right) \left( \frac{g_{m6}}{g_{o6} + g_{o7}} \right) \approx \left( g_{m5h}g_{m4c}r_{ds4c}r_{ds4} \right) \left( \frac{g_{m6}}{g_{o6} + g_{o7}} \right) $$
Figure 6: Common mode half-circuit (Gray and Meyer)

COMMON MODE FEEDBACK GAIN

Figure 7: Common mode feedback circuit

Figure 7 shows a PMOS input CMFB circuit. In this project, an NMOS input pair was used, but the basic operation is the same. The gain from $V_o$ to $V_{cm}$ is,

$$A_{CMFB} = \frac{g_{m21}}{g_{m25}}$$
Therefore, using this gain and the common mode control gain found in the last section, the total gain of the CMFB loop is found to be,

\[ A_{CMFB\text{LG}} = A_{CMC}A_{CMFB} = \frac{g_{m21}}{g_{m25}} (g_{m5h} (g_{m4c} r_{ds4} r_{ds4})) \left( \frac{g_{m6}}{g_{o6} + g_{o7}} \right) \]

In order to increase the CMFB loop gain without modifying the amplifier, the transconductance ratio of the CMFB input and diode connected output transistor can be increased. This gain must be carefully controlled so that stability of the CMFB loop is maintained.

**COMMON MODE REJECTION RATIO**

In a differential amplifier, the output voltage is ideally independent of the common mode voltage and depends only on the differential input. There is always some dependence on the CM voltage, though, so \( A_{CM} \neq 0 \). It is important, though, that the differential gain is much larger than the CM gain and therefore the ratio is considered a figure of merit for the amplifier. The common mode rejections ratio is then defined as,

\[ CMRR = \left| \frac{A_{DM}}{A_{CM}} \right| \]

Substituting the \( A_{DM} \) and \( A_{CM} \) derived previously,

\[ CMRR = \left| \frac{A_{DM}}{A_{CM}} \right| = \frac{g_{m2} (g_{m2c} r_{ds2} r_{ds2}) (g_{m4c} r_{ds4} r_{ds4})}{\left( \frac{1}{r_{ds5h}} (g_{m4c} r_{ds4} r_{ds4}) \right)} \]

**POWER SUPPLY REJECTION RATIO (PSRR)**

The power supply rejection ratio is a measure of the rejection of power supply variations to the output. It can be formulated as,

\[ PSRR^+ = \frac{\Delta V_{DD}}{\Delta V_{OUT}} \text{ and } PSRR^- = \frac{\Delta V_{SS}}{\Delta V_{OUT}} \]

Ideally, the output would be completely independent of power supply variations, but this can never be the case. The DC PSRR is most limited by the PSRR of the biasing circuit. For this reason, it is important to design the biasing circuit with a maximum PSRR. This is discussed in greater detail in the section on the biasing circuit.

**SYSTEMATIC DIFFERENTIAL OFFSET VOLTAGE**

A fully differential amplifier will not have systematic differential offset voltage if it is designed symmetrically. Offset will still exist due to mismatch between transistor pairs. The importance of transistor matching is the same as that found in the section on input referred noise. This is because MOSFET noise is modeled at the gate and a \( V_T \) mismatch can be modeled at the gate as well. Therefore, the most important transistors to match are \( M_{1,2} \) and \( M_{3,4} \). The equation is derived later and found to be (where \( V_{tnm} \) is the transistor mismatch voltage).

\[ V_{o,seq}(f) = V_{t_{nm1}}(f) + V_{t_{nm3}}(f) \left( \frac{g_{m3}}{g_{m1}} \right) \]
Matching increases with transistor area which is convenient because flicker noise is inversely proportional to area. This is discussed in greater detail in the input referred noise section.

**INPUT COMMON MODE RANGE (ICMR)**

The input common mode range is an important parameter for a generic op-amp where the common mode input voltage is unknown during the design process. It can be found by finding the largest CM input voltage where M5 is still in saturation and the lowest CM input voltage where M1,2C and M3,4 are still in the saturation region. Therefore,

\[
\text{Max ICMV} = V_{DD} - V_{DSSAT5} - V_{DSSAT2} - |V_{TP}|
\]

and

\[
\text{Min ICMV} = V_{SS} + V_{DSSAT4} + V_{DSSAT4c} + V_{DSSAT2C} - |V_{TP}|
\]

If the gate of M2C is biased at a constant voltage, though, the minimum ICMV is,

\[
\text{Min ICMV} = V_{G2C} + V_{DSSAT2C}
\]

and the gate voltage of M2c is limited to,

\[
\text{Min } V_{G2c} = V_{GS6} - |V_{TP}| = V_{ON6} + V_{TN} - |V_{TP}|
\]

and \(V_{GS6}\) is limited to,

\[
\text{Min } V_{GS6} = V_{SS} + V_{DSSAT4} + V_{DSSAT4c}
\]

Substituting the minimum \(V_{GS6}\) into the minimum \(V_{G2c}\) equation and, in turn, substituting the minimum \(V_{G2c}\) equation into the minimum ICMV equation for constant gate voltage, the original minimum ICMV is found. This demonstrates the difficulty of obtaining the maximum ICMV because M6 and the gate bias for M2C must be sized precisely.

**OUTPUT VOLTAGE SWING RANGE**

The output voltage swing range is an important parameter of the op-amp and is becoming more important as the supply voltage continues to decrease. The output voltage swing range can be found by considering the largest output voltage where transistor M7 is still in saturation and subtract from that the lowest output voltage where M6 is still in saturation. For a transistor to be in the saturation region, \(V_{DS} > V_{DSSAT}\). Therefore, M7 is at the edge of saturation when \(V_{OUT}=V_{DD}-V_{DSSAT7}\) and M6 is at the edge of saturation when \(V_{OUT}=V_{SS}+V_{DSSAT6}\).

\[
\text{Output Swing Range} = V_{SS} + V_{DSSAT6} \text{ to } V_{DD} - V_{DSSAT7}
\]

where,

\[
V_{DSSATx} = \sqrt{\frac{2I_{Dx}}{\mu C_{OX} \left(\frac{W}{L}\right)_x}}
\]
The differential output voltage swing range is two times the single ended output voltage swing range which is one of the great benefits of differential amplifiers.

### POWER CONSUMPTION

Power consumed in a MOSFET transistor is,

\[ P = V_{DS}I_D \]

The \( V_{DS} \) of any branch will add up to the differential supply voltage. Therefore, the total power can be expressed in total current as,

\[ I_{TOT} = \frac{P_{TOT}}{V_{DD} - V_{SS}} \]

For this project, the total power is 10mW and the supply voltage is ±2.5V, then the total current is 2mA. In this way, the power consumption can be monitored by limiting the current delivered to the op-amp as opposed to viewing the power consumed by each device.

### INPUT REFERRED NOISE

The most dominant noise sources exist in the first stage of the amplifier. This is because any noise referred to the input of the second stage is attenuated by the gain of the first stage when being referred to the amplifier input. That is,

\[ V_{Tnoise} = V_{noise (1stStage)} + \frac{V_{noise (2ndStage)}}{A_V1} \]

Therefore, we need only consider the first stage to find the approximate total input referred noise.
The noise for each transistor pair is uncorrelated but equal in equation. Therefore, they can be squared and added. The small-signal transfer function from $M_{3,4}$ to the input can be found as,

$$\frac{V_{\text{in}}}{V_{n3}} = \frac{V_{\text{out}}}{V_{n3}} = \frac{1}{g_{m1} R_{\text{OUT}1}} g_{m3} R_{\text{OUT}1} = \frac{g_{m3}}{g_{m1}}$$

This is the equivalent of taking the gain from the gate at $M_3$ to the output and then dividing by the gain from the input to the output. Similarly,

$$\frac{V_{\text{in}}}{V_{n5}} = \frac{1}{g_{m1} R_{\text{OUT}1}} g_{m5} R_{\text{OUT}1} \ll \frac{V_{\text{in}}}{V_{n3}}$$

Therefore it is not considered. The transfer functions for $M_{3C,2C}$ and $M_{3C,4C}$ are small as well. Clearly the transfer function from the input gate to the input is 1. Therefore, the equivalent noise at the input is found to be,

$$V_{\text{neq}}^2(f) = 2V_{n1}^2(f) + 2V_{n3}^2(f) \left( \frac{g_{m3}}{g_{m1}} \right)^2$$

It is clear from this equation that $g_{m3}$ should be made smaller than $g_{m1}$. This input There are two dominant noise sources in MOSFET transistors: thermal and flicker. Modern processes are dominated by flicker noise, while thermal noise can be dominant in older processes. If the input equivalent noise is dominated by thermal noise, then the noise voltage is given by the equation,

$$V_{\text{noise (thermal)}}^2(f) = 4kT \left( \frac{2}{3} \right) \left( \frac{1}{g_{m1}} \right)$$

and the input referred noise is,

$$V_{\text{neq}}^2(f) = \frac{16}{3} kT \left( \frac{1}{g_{m1}} \right) + \frac{16}{3} kT \left( \frac{g_{m3}}{g_{m1}} \right)^2$$

Alternatively, if flicker noise is dominant, then the noise voltage is given by,

$$V_{\text{noise (flicker)}}^2(f) = \frac{K}{WLC_{\text{OX}}}$$

where $K$ is a process dependent parameter. Then the input referred noise is,

$$V_{\text{neq}}^2(f) = \frac{2}{C_{\text{OX}}} \left[ \frac{K_1}{W_1 L_1} + \left( \frac{\mu_n}{\mu_p} \right) \frac{K_3 L_1}{W_1 L_3} \right]$$
When this is the case, the noise from the NMOS transistors will dominate when $L_1=L_3$. Increasing $L_3$ decrease the second term noise as an inverse square and simultaneously increases the gain of the amplifier. The noise is independent of the width of $M3$, and therefore it can be made large. Increasing $W_1$ will decrease 1/f noise and also decrease white noise. (Johns and Martin)

**AC ANALYSIS (DIFFERENTIAL MODE)**

**POLES AND ZEROS**

For reasons to be discussed in a later section, it is important in be able to decrease the frequency of the first pole. To do this, the resistance of the capacitance at the node must be increased. In amplifier design, a miller capacitor is used to introduce a large capacitance at a node using a small capacitor (and likewise a minimal area). Figure 9 shows a schematic diagram of the miller effect. In this figure, the amplifier represents the gain of the second stage and the impedance is the compensation capacitance. The input impedance can be easily calculated and is shown to be,

$$Z_{IN} = \frac{1}{sC(1-A_V)} \approx \frac{1}{sC(-A_V)}$$

In this case, $A_V$ is the gain of the second stage of the amplifier. Therefore,

$$Z_{IN} \approx \frac{1}{sC(-A_V)} = \frac{g_{o6} + g_{o7}}{sCg_{m6}}$$

and

$$C_{EQ} = \frac{Cg_{m6}}{g_{o6} + g_{o7}}$$

The equivalent resistance at this node is just the cascaded output resistance of the first stage. The pole is then found to be,

$$p_1 = -\omega_1 = -\frac{1}{R_{OUT1}C_{EQ}} = \frac{-(g_{o6} + g_{o7})(g_{m2c}r_{ds2}r_{ds2}||g_{m4c}r_{ds4}r_{ds4})}{Cg_{m6}}$$

The second most dominant pole is located at the output node. The total output conductance at this node is,

$$g_{OUT} = g_{ds7} + g_{ds6} + \frac{g_{m6}C_C}{C_C + C_1}$$

and the capacitance at this node is,

$$C_{OUT} = C_L + \frac{C_1C_C}{C_C + C_1}$$

where,
\[ C_1 = C_{DDM4C} + C_{DDM2C} + C_{GGM6} \]

Therefore, the second pole is,
\[ p_2 = -\omega_2 = -\frac{C_G g_{m6} + (C_1 + C_G)(g_{ds5} + g_{ds7})}{C_L (C_1 + C_G) + C_G C_1} \]

Finally, there is a zero that should be taken into account.
\[ z_1 = g_{m6} \frac{C}{C_C} \]

These poles and zeros significantly affect crucial parameters of the op-amp such as UGF and PM.

**UNITY GAIN FREQUENCY AND PHASE MARGIN**

If the higher order poles and all the zeros are sufficiently greater than the unity gain frequency, then the transfer function of the op amp is,

\[ T(s) = \frac{A_{DM}}{1 - \frac{s}{p_1}} \]

For high frequencies, \( s/p_1 >> 1 \), and the magnitude of the transfer function (for the amplifier in this project) is,
\[ |T(s)| = -p_1A_{DM} \frac{\omega}{\omega} = g_{m2} \frac{\omega}{\omega C} \]

Therefore, the gain of the amplifier falls off inversely with frequency at frequencies larger than the first pole. Also, equating the transfer function to 1, the unity gain frequency is found to be,
\[ UGF = \omega_0 = -p_1 A_{DM} = g_{m2} \frac{C}{C} \]

This shows that the UGF is equal to the gain-bandwidth product for a single pole amplifier. A key parameter is the phase at this frequency or rather \( 180^\circ - \text{phase}(\omega_0) \). This is the phase margin and it is a measure of the stability of the closed loop amplifier. The gain of an op-amp in a feedback configuration is,
\[ A(j\omega) = \frac{A_{DM}(j\omega)}{1 + \beta A_{DM}(j\omega)} \]

So if \( \beta = 1 \), at the UGF the actual gain of the op-amp in feedback is,
\[ A(j\omega) = \frac{e^{j(180-\text{PM})}}{1 + e^{j(180-\text{PM})}} \]

So when PM goes to 0, the gain at the UGF goes to infinity and the amplifier oscillates. Therefore, phase margin can be used as a stability criterion. Figure 10 shows the relative gain (dB above \( 20\log(1/\beta) \)) normalized to the UGF of the loop transfer function. An op-amp with \( 60^\circ \) of phase margin will have a stable gain for all frequencies less than the UGF of the op-amp and for this reason it is often used as an optimum design specification.
The phase margin can be found by summing the phase contribution of each pole and zero at the unity gain frequency.

\[ PM = 180 - \tan^{-1}\left(\frac{UGF}{\omega_1}\right) - \tan^{-1}\left(\frac{UGF}{\omega_2}\right) - \tan^{-1}\left(\frac{UGF}{z_1}\right) \approx 90 - \tan^{-1}\left(\frac{UGF}{\omega_2}\right) - \tan^{-1}\left(\frac{UGF}{z_1}\right) \]

where the approximation is made from the fact that \( \omega_1 < UGF \). Using this fact and the equations for the poles and zeroes calculated in the last section, the op-amp can be compensated to be made stable.

**COMPENSATION**

For an op-amp in feedback, it is necessary to have a phase margin for the entire loop gain. Application specific amplifiers do not have to be stable at the UGF of the open loop amplifier. Instead, phase margin is measured at the UGF of the loop gain (UGF\(_{LG}\)) or,

\[ UGF_{LG} = \frac{UGF}{A_O} \]

where \( A_O \) is the closed loop gain of the amplifier. This allows the designer to increase the bandwidth of the amplifier. In our case, we are designing a generic amplifier, so it must be stable at the open loop UGF.

The most common method of compensation is to reduce the bandwidth of the amplifier. In our case, the dominant pole at the output of the first stage is reduced by adding a Miller capacitor (as discussed in a previous section). This also increases the frequency of the second pole, further improving the phase margin. With this in mind, we revisit the phase margin equation from the last section,

\[ PM \approx 90 - \tan^{-1}\left(\frac{UGF}{\omega_2}\right) - \tan^{-1}\left(\frac{UGF}{z_1}\right) = 90 - \tan^{-1}\left(\frac{g_{m2}c_1(c_1 + C) + CC_1}{C(g_{ms6} + (C_1 + C)(g_{ds6} + g_{ds}))}\right) - \tan^{-1}\left(\frac{g_{m2}}{g_{ms6}}\right) \]

where,
\[ C_1 = C_{DDMC4} + C_{DDMC2} + C_{GGM6} \]

To improve phase margin, \( g_{m6} \) should be increased while \( C_1 \) (which is dominated by \( C_{GGM6} \)) is decreased. This implies that M6 should have a minimum length and large current. With the largest \( g_{m6} \) allowed by power dissipation limitations, then \( g_{m2} \) can be increased to improve the UGF and gain until the phase margin approaches the limit of 45\(^\circ\). This will be discussed in greater detail in the design process section.

The phase contribution of the zero can be a problem when \( g_{m2} \) is similar in magnitude to \( g_{m6} \). To alleviate this problem, lead compensation can be used. This will move the zero to,

\[ z_1 = \frac{g_{mb}}{C(1 - g_{m6}R_Z)} \]

The lead compensation resistor, \( R_Z \), can be set to 1/\( g_{m6} \) to move the zero to infinity (or a really large frequency). Alternatively, the second pole can be canceled with,

\[ R_Z = \frac{C + C_L + C_1}{g_{m6}C} \]

In this case, the load capacitance is unknown, so if \( C_L \) is larger than designed for, the frequency of the zero will increase greatly reducing phase margin. Johns and Martin (Analog Integrated Circuit Design) recommend setting the zero 20% larger than the UGF without lead compensation instead.

**AC RESPONSE LINEARITY**

The fast Fourier transform (FFT) is a method for quickly calculating the discrete Fourier transform. From the FFT the total harmonic distortion (THD) can be found. The THD is the ratio of the power of the fundamental frequency to the power of all other harmonic frequencies. It can be written as,

\[ THD = \frac{P_2 + P_3 + \cdots + P_n}{P_1} \]

Another figure of merit for the linearity of the op-amp is the spurious free dynamic range. It is defined as,

\[ SFDR = \frac{P_1}{\text{Power of the largest harmonic distortion component}} \]

It is named so because when the plot is in dB, the SFDR is the difference between the signal and the next highest "spur".

**AC ANALYSIS (COMMON MODE FEEDBACK)**

**COMMON MODE POLES AND ZEROS**

The poles and zeroes of the CMFB loop are at the same nodes as those in the differential mode loop. In this case, though, the output resistance of the first stage increases because the path including \( M_{sih} \) looks like a triple cascode (very high impedance) to the path. Therefore, the poles and zeroes are found to be,
\[ p_1 = -\omega_1 = -\frac{1}{R_{\text{OUT}} C_{\text{EQ}}} = \frac{-(g_{o6} + g_{o7})}{(g_{m4c} r_{ds4c} r_{ds4}) C g_{m6}} \]

\[ p_2 = -\omega_2 = -\frac{C g_{m6} + (C_1 + C_C)(g_{ds6} + g_{ds7})}{C_L (C_1 + C_C) + C_C C_1} \]

\[ z_1 = \frac{g_{m6}}{C_C} \]

Due to this close relationship between the CMFB and DM poles and zeroes it is important to consider the CMFB stability when designing the op-amp. Often it is more difficult to obtain stability in the CMFB loop.

**COMMON MODE UNITY GAIN FREQUENCY AND PHASE MARGIN**

The gain of the CMFB loop was found in a previous section to be,

\[ A_{CMFB\text{LG}} = \frac{g_{m21} g_{m5c}}{g_{m5h} (g_{m4c} r_{ds4c} r_{ds4})} \left( \frac{g_{m6}}{g_{o6} + g_{o7}} \right) \]

If the assumption is made that this is a one pole gain path the UGF is,

\[ UGF = \frac{g_{m21} g_{m5h}}{g_{m2c}} \]

The phase margin is,

\[ PM = 180 - \tan^{-1} \left( \frac{UGF}{\omega_1} \right) - \tan^{-1} \left( \frac{UGF}{\omega_2} \right) - \tan^{-1} \left( \frac{UGF}{z_1} \right) \approx 90 - \tan^{-1} \left( \frac{UGF}{\omega_2} \right) - \tan^{-1} \left( \frac{UGF}{z_1} \right) \]

As discussed in the previous section, it is critical that the stability of the CMFB loop be considered during the design of the amplifier because of the interdependence of their poles and zeroes.

**TRANSIENT ANALYSIS**

**STEP RESPONSE**

The phase margin is a criteria for stability that can be determined from the AC response. Another test of stability is the step response in a transient analysis. The settling time of the op-amp is an important parameter for op-amps being used as comparators or during start up of an integrated circuit. The overshoot of the op-amp’s response to a step function can be damaging because it can reverse bias PN junctions (if the voltage overshoots the rail) or put a circuit into an undesirable state. Both the overshoot and the settling time are a measure of stability and are related to the PM. The damping ratio, \( \zeta \), is defined as,

\[ \zeta = \frac{PM}{100} \]

Table 1 gives the relationship of the damping ratio to the percentage overshoot.
Table 1: Relationship of damping ratio to overshoot

<table>
<thead>
<tr>
<th>Value of $\zeta$</th>
<th>1</th>
<th>0.7</th>
<th>0.6</th>
<th>0.5</th>
<th>0.4</th>
<th>0.3</th>
</tr>
</thead>
<tbody>
<tr>
<td>Overshoot:</td>
<td>0%</td>
<td>5%</td>
<td>10%</td>
<td>16%</td>
<td>25%</td>
<td>37%</td>
</tr>
</tbody>
</table>

Figure 1 shows the unit step response for various damping ratios. A damping ratio of 0.6 (corresponding to a PM of 60) settles quickly with minimal overshoot, demonstrating its superior stability and agreeing with the plot in Figure 10.

During the design process the AC response is emphasized and therefore the overshoot and settling time are assumed to follow this model until late in the design process.

**SLEW RATE**

The slew rate of an amplifier is the maximum rate of change of the output voltage. In the case of a differential amplifier, the limiting factor is often the charging or discharging of the compensation capacitor, $C_c$. The maximum rate of change of the voltage across this capacitor is when the differential input voltage is large enough to steer the entire first stage current, $I_s$, to one branch of the first stage. Then, from the capacitance voltage relationship,

$$I_s = C_c \frac{dV}{dt} \Rightarrow SR = \frac{dV}{dt} = \frac{I_s}{C_c}$$

Therefore, it is important to consider the slew rate when determining the current budget and sizing the compensation capacitor.
In this section, the design specifications are listed side-by-side with their equation. From this table, a design process will be formulated to maximize phase margin.

<table>
<thead>
<tr>
<th>Specification</th>
<th>Governing Rule or Equation</th>
</tr>
</thead>
<tbody>
<tr>
<td>$2 \text{pF} &gt; C_i &gt; 0 \text{pF}$</td>
<td>Worst case phase margin for maximum $C_i$</td>
</tr>
<tr>
<td>UGF &gt; 50MHz</td>
<td>$UGF = -p_1 A_{DM} = \frac{g_{m2}}{C}$</td>
</tr>
<tr>
<td>PM &gt; 45°</td>
<td>$PM = 90 - \tan^{-1}\left(\frac{UGF}{\omega_2}\right) - \tan^{-1}\left(\frac{UGF}{Z_1}\right)$</td>
</tr>
<tr>
<td>DC Gain &gt; 90dB</td>
<td>$A_{DM} = g_{m2} g_m (r_{ds6}</td>
</tr>
<tr>
<td>$V_{\text{OUT}}$ swing range includes [-1.75V, +1.75V]</td>
<td>Output Swing Range = $V_{SS} + V_{\text{DSSAT6}}$ to $V_{DD} - V_{\text{DSSAT7}}$</td>
</tr>
<tr>
<td>ICMR&gt;3V includes [-1V, +1V]</td>
<td>Max ICMV = $V_{DD} - V_{\text{DSSAT5}} - V_{\text{DSSAT2}} -</td>
</tr>
<tr>
<td></td>
<td>Min ICMV = $V_{SS} + V_{\text{DSSAT4}} + V_{\text{DSSAT4c}} + V_{\text{DSSAT2c}} -</td>
</tr>
<tr>
<td>Slew rate &gt; 100V/µs</td>
<td>$SR = \frac{dV}{dt} = \frac{I_5}{C_c}$</td>
</tr>
<tr>
<td>Overshoot&lt;25% and Settling time&lt;50ns</td>
<td>Should follow from PM &gt; 45°</td>
</tr>
<tr>
<td>CMFB PM &gt; 45°</td>
<td>$90 - \tan^{-1}\left(\frac{UGF}{\omega_2}\right) - \tan^{-1}\left(\frac{UGF}{Z_1}\right)$</td>
</tr>
<tr>
<td>CMFB UGF</td>
<td>$UGF = \frac{g_{m21} g_{m5h}}{g_{m25} C}$</td>
</tr>
<tr>
<td>Offset voltage</td>
<td>$V_{seq}^2(f) = V_{imm1}^2(f) + V_{imm3}^2(f) \left(\frac{g_{m3}}{g_{m1}}\right)^2$</td>
</tr>
<tr>
<td>Input Referred Noise</td>
<td>$V_{neq}^2(f) = \frac{2}{C_{OX} f} \left[ \frac{K_1}{W_1 L_1} + \left(\frac{\mu_n}{\mu_p}\right) \frac{K_1 L_1}{W_1 L_3^2} \right]$</td>
</tr>
<tr>
<td></td>
<td>$V_{noise(thermal)}(f) = 4 kT \left(\frac{2}{3}\right) \left(\frac{1}{g_{m1}}\right)$</td>
</tr>
</tbody>
</table>

Other important parameters that do not have a specification are included in the table below.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Equation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pole 1</td>
<td>$p_1 = -\left(\frac{g_{o6} + g_{o7}}{C}\right) g_{m2c} r_{ds2c} r_{ds2}</td>
</tr>
</tbody>
</table>
\[ p_2 = -\frac{C_C g_{m6} + (C_1 + C_C)(g_{ds6} + g_{ds7})}{C_1(C_1 + C_C) + C_C C_1} \]

\[ z_1 = \frac{g_{m6}}{C(1 - g_{m6}R_Z)} \]

\[ \left( \frac{1}{r_{ds5h}} \left( g_{m4c} r_{ds4c} r_{ds4} \right) \right) \left( \frac{g_{m6}}{g_{o6} + g_{o7}} \right) \]

\[ \left( g_{m5h} \left( g_{m4c} r_{ds4c} r_{ds4} \right) \right) \left( \frac{g_{m6}}{g_{o6} + g_{o7}} \right) \]

\[ A_{CMFB} = \frac{g_{m21}}{g_{m25}} \left( g_{m5h} \left( g_{m4c} r_{ds4c} r_{ds4} \right) \right) \left( \frac{g_{m6}}{g_{o6} + g_{o7}} \right) \]

**BIAS CIRCUIT EQUATIONS**

Figure 12 shows a \( V_T \) referenced self-bias reference circuit. The area of the diode in the right branch is 8 times the area of the transistor in the left branch. The NMOS and PMOS cascode transistors give the circuit a large PSRR and set the current in each branch to be nearly identical. Then \( V_{GS3} = V_{GS3} \) and \( V_{S4} = V_{BE1} \). Therefore the voltage across the resistor is,

\[ V_R = V_{BE1} - V_{BE2} = \Delta V_{BE} = V_T \ln \left( \frac{A_2}{A_1} \right) = V_T \ln(8) \]

This is called a PTAT voltage (proportional to absolute temperature) because \( V_T \) increases positively with temperature. The bias current can then be controlled by the magnitude of the resistance and is,

\[ I_{BIAS} = \frac{V_R}{R} = \frac{V_T \ln(8)}{R} \]

A value for the bias current is set in this way and transistor multipliers can be used to obtain a multiple of the bias current in necessary. Multipliers are used to maximize the matching of the current mirror. A diode can be created in a MOSFET process by forward biasing the P-source/drain to N-well interface of a PMOS transistor. This is discussed in greater detail in the layout section.
DESIGN PROCESS

In class, it was suggested that we try to maximize the unity gain frequency while maintaining stability and meeting the other design specifications. To simplify the design process, it is necessary to minimize the design variables and minimize the number of specifications to observe. Many of the project specifications are met inherently by the amplifier architecture chosen. For example, ICMR and OCMR, PSRR, and CMRR do not need to be monitored continuously during the design process. Overshoot and settling time requirements can be related to the phase margin and, therefore, can be monitored in the AC response. The worst case stability occurs at a maximum capacitive load, so the design process should be done with CL=2pF. The power consumption can be controlled by limiting the current through the amplifier.

Therefore, the only parameters that have to be constantly monitored and optimized are the slew rate, UGF, PM, and DC gain. Also, the UGF, PM, and DC gain of the CMFB loop should be monitored. Therefore, the following design strategy was used to maximize the UGF:

- $g_m$ should be made large to increase the GBW product
- Constantly monitor and maximize the term $\frac{g_m}{C_L+C_1}$, which is the upper bound on $p_1$
Increasing $g_{m6}$ by increasing the width also increases the gate capacitance which dominates $C_1$.

The length of M6 is minimum size to simultaneously increase $g_{m6}$ and decrease $C_1$.

$\frac{g_{m6}}{C_L + C_1}$ can be maximized by increasing the current through M6 because this increases the transconductance without increasing the gate capacitance.

- **Budget 100µA for the bias circuit and put the remaining current (after the second stage current) in the first stage**
  - Increase the compensation capacitance until PM is achieved
  - Optimize the UGF and PM by moving the zero with the lead resistance
  - Check the slew rate ($SR = \frac{I_s}{C_C}$)
    - If the slew rate is greatly exceeded, then current from the first stage can be directed to the second stage to further increase the second pole frequency
    - $C_C$ should be set to meet the PM specification and $R_z$ should be swept to optimize the zero location
  - Once the optimum current ratio is found where the slew rate is just above the project requirement and $p_2$ is maximized, the stability of the CMFB loop should be verified
    - The amplifier should be modified to meet the CMFB loop stability
  - Finally, each of the other specification targets should be verified

The gain of the amplifier was not considered in this process because it naturally increases $g_{m1}$ and $g_{m6}$ while minimizing the current in the first stage. This naturally leads to an amplifier with a large gain. The lengths of the NMOS first stage transistors can be increased to increase gain if necessary, though.

### Biasing Circuit Design

Figure 13 shows the finalized bias circuit schematic. The left 2 branches are collectively the PTAT current source. The resistor was set to 10kΩ so that the current at room temperature is,

$$I_R = \frac{V_T \ln(8)}{R} = 5.4\mu A$$

This current is mirrored to the second two branches and increased by a multiplier of 3 for a total current of 16µA. This is because the current through the first stage is 260µA or 130µA per branch and the NMOS transistors have a multiplier of 8. Therefore, the current densities are closely ratioed between these branches. The bias for these NMOS transistor is then set by using unit equal sized transistors in the first branch with the gate of the bottom transistor tied to the drain of the top transistor. The gate voltage for the top transistor is set by using the same current in the second branch and size the transistor with 4 times the length. This sets the $V_{DS}$ across the bottom transistor as its $V_{ON}$. This is a high swing cascode biasing circuit.

The last two branches mirror the current up to 49µA (simulated) to bias the first and second stage. A unit diode connect PMOS transistor is used to mirror the current to an equivalent sized M=5 transistor in the first stage (~260µA) and an equivalent sized M=15 transistor in the second stage (~750µA).

The bias circuit is self starting because there is only one stable state. Therefore, there is no need for a start up circuit.
The individual transistor sizes can be seen in Figure 13. Also, the method for making the diodes is shown in the schematic. A unit diode was designed by connecting the gate to bulk and drain to source of a 4.95µm x 4.95µm PMOS transistor. The gate source connection is the cathode and the source drain connection is the anode.

**FULLY DIFFERENTIAL AMPLIFIER DESIGN**

The table below summarizes the transistor sizes for all devices in the amplifier and CMFB circuit.

<table>
<thead>
<tr>
<th>Transistor</th>
<th>W/L</th>
<th>Multiplier</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1,2</td>
<td>10.05/1.2</td>
<td>32</td>
</tr>
<tr>
<td>M1C,2C</td>
<td>10.05/0.6</td>
<td>8</td>
</tr>
<tr>
<td>M3,4</td>
<td>10.05/4.95</td>
<td>8</td>
</tr>
<tr>
<td>M3C,4C</td>
<td>10.05/4.95</td>
<td>8</td>
</tr>
<tr>
<td>M5</td>
<td>10.05/2.4</td>
<td>5</td>
</tr>
<tr>
<td>M5CMC</td>
<td>10.05/1.2</td>
<td>10</td>
</tr>
<tr>
<td>M6,9</td>
<td>12.45/0.6</td>
<td>4</td>
</tr>
<tr>
<td>M7,10</td>
<td>10.05/2.4</td>
<td>15</td>
</tr>
<tr>
<td>R₂</td>
<td>1kΩ</td>
<td>n/a</td>
</tr>
<tr>
<td>Cₜ</td>
<td>1.6pF</td>
<td>n/a</td>
</tr>
<tr>
<td>M25,26</td>
<td>10.05/1.2</td>
<td>2</td>
</tr>
<tr>
<td>M21,22,23,24</td>
<td>12/1.2</td>
<td>2</td>
</tr>
<tr>
<td>M26,27</td>
<td>10.05/4.95</td>
<td>2</td>
</tr>
</tbody>
</table>
Figure 14 shows the entire final schematic view including the bias circuit, amplifier, and CMFB circuit.
The finalized current budget is shown in the table below.

<table>
<thead>
<tr>
<th></th>
<th>First Stage</th>
<th>Second Stage</th>
<th>CMFB Circuit</th>
<th>Bias Circuit</th>
<th>Total</th>
</tr>
</thead>
<tbody>
<tr>
<td>Current</td>
<td>258.07µA</td>
<td>2x742.1µA</td>
<td>2x34.46 µA</td>
<td>97.2µA</td>
<td>1.908mA</td>
</tr>
<tr>
<td>Power</td>
<td>1.29mW</td>
<td>7.42mW</td>
<td>0.344mW</td>
<td>0.49mW</td>
<td>9.54mW</td>
</tr>
</tbody>
</table>

This is within the allowed 10mW of power specified in the project definition. The simulation results for the circuit with these parameters are given in the next section.

**PRELAYOUT SIMULATION RESULTS**

In this section, the test results for the amplifier are presented and discussed. The testing methods are outlined and test bench circuits are provided for reference.

**DIFFERENTIAL MODE GAIN AND STABILITY**

The circuit used to measure the differential mode AC response is shown in Figure 15. The amplifier is configured as an inverting unity gain amplifier. The gain and phase from the differential input to the differential output was plotted. This plot can be seen in Figure 16.

![Figure 15: Closed loop test bench for measuring the differential mode AC response](image)

The DC gain is 100.1dB, -3dB point is 1.45kHz, UGF is 198MHz, and the PM is 50.7°. All these parameters exceed the specifications from the project definition and the UGF was maximized as recommended in class. To further demonstrate the frequency response of the amplifier, the poles and zeroes are shown in the plot in Figure 17. These figures represent the response at the maximum CL (2pF), at room temperature, and with ±2.5V supplies. In the next sections, the frequency response is shown to meet the specifications for all transistor corners, all temperatures, all capacitive loads, and all power supply voltages.
Figure 16: AC response for the differential amplifier

Figure 17: Poles and zeroes of the differential amplifier
PERFORMANCE VERSUS TEMPERATURE (VARIOUS CAPACITIVE LOADS)

The AC response versus temperature for CL=0pF, 1pF, and 2pF is given in this section.

Figure 18: Gain versus temperature for CL=2pF

Figure 19: Phase versus temperature for CL=2pF

Figure 20: Gain versus temperature for CL=1pF

Figure 21: Phase versus temperature for CL=1pF
The table below summarizes the results. The zero can be seen in Figure 22 to be less than the UGF. This causes problem in post layout simulations.

<table>
<thead>
<tr>
<th></th>
<th>CL=2pF</th>
<th>CL=1pF</th>
<th>CL=0pF</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Temperature</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>-40°C</td>
<td>104.3dB</td>
<td>104.3dB</td>
<td>104.3dB</td>
</tr>
<tr>
<td>85°C</td>
<td>94.85dB</td>
<td>94.85dB</td>
<td>94.85dB</td>
</tr>
<tr>
<td><strong>Gain</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Phase Margin</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>UGF</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>211.7MHz</td>
<td>183.3MHz</td>
<td>303.3MHz</td>
<td>244.5MHz</td>
</tr>
<tr>
<td>338.3MHz</td>
<td>354.5MHz</td>
<td>554.5MHz</td>
<td>338.3MHz</td>
</tr>
</tbody>
</table>

**PERFORMANCE VERSUS POWER SUPPLY VARIATION**

*Figure 24: Gain versus power supply voltage (±20%)*
Figure 24 and Figure 25 show the gain and phase of the amplifier versus power supply voltage. The table below summarizes the results and shows that the amplifier meets the requirements over all supply voltages.

<table>
<thead>
<tr>
<th></th>
<th>±2V Supply</th>
<th>±2.5V Supply</th>
<th>±3V Supply</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gain</td>
<td>96.7dB</td>
<td>100.1dB</td>
<td>101dB</td>
</tr>
<tr>
<td>Phase Margin</td>
<td>51.62°</td>
<td>50.46°</td>
<td>50.63°</td>
</tr>
<tr>
<td>UGF</td>
<td>182.4MHz</td>
<td>198.7MHz</td>
<td>204.3MHz</td>
</tr>
</tbody>
</table>

**CORNER PERFORMANCE**

In this section, the frequency response for the amplifier at the four corners of MOSFET operation are given. The simulation was performed in the same way as the other cases, expect the simulator was pointed to different sections of the model file.
Figure 26: AC response for NMOS and PMOS fast

Figure 27: AC response for NMOS and PMOS slow
Figure 28: AC response for NMOS fast and PMOS slow

Figure 29: AC response for NMOS slow and PMOS fast
These results are summarized in the table below.

<table>
<thead>
<tr>
<th>NMOS</th>
<th>PMOS</th>
<th>GAIN</th>
<th>UGF</th>
<th>PM</th>
<th>-3dB Point</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fast</td>
<td>Fast</td>
<td>99.36dB</td>
<td>197.6MHz</td>
<td>50.69°</td>
<td>1.62kHz</td>
</tr>
<tr>
<td>Fast</td>
<td>Slow</td>
<td>98.48dB</td>
<td>183.5MHz</td>
<td>51.43°</td>
<td>1.69kHz</td>
</tr>
<tr>
<td>Slow</td>
<td>Fast</td>
<td>100.6dB</td>
<td>194.7MHz</td>
<td>52.9°</td>
<td>1.33kHz</td>
</tr>
<tr>
<td>Slow</td>
<td>Slow</td>
<td>100.3dB</td>
<td>188.6MHz</td>
<td>52.37°</td>
<td>1.36kHz</td>
</tr>
</tbody>
</table>

Clearly, all of these measurements meet and exceed the specifications of the project.

**SLEW RATE, OVERSHOOT, AND SETTLING TIME**

Figure 30 shows the test bench used to measure the slew rate, overshoot, and settling time of the amplifier. The differential amplifier is connected in a unity inverting gain configuration. The outputs and inputs of the amplifier are buffered from the feedback network by using ideal voltage controlled voltage sources with a gain of 1.

![Figure 30: Test bench used to measure slew rate, overshoot, and settling time](image)

The $\beta$ of the feedback network is $\frac{1}{2}$ for this circuit, therefore this is not a test of the worst case phase margin. This is demonstrated in Figure 31. This figure shows that the transfer function for the feedback loop is the difference (in dB) of the closed loop transfer function and the constant line $20\log_{10}(1/\beta)$. This is because,

$$20\log_{10}(A_{DM}) - 20\log_{10}\left(\frac{1}{\beta}\right) = 20\log_{10}(A_{DM}\beta) = 20 \log_{10}(A_{LG})$$

Therefore, the 0dB point for the loop gain is the frequency at which $A_{DM}=20\log_{10}(1/\beta)$ or,

$$A_{DM} = 20\log_{10}\left(\frac{1}{\beta}\right) = 20 \log_{10}(2) \approx 6dB$$
Figure 31: Loop transfer function with a β feedback of f

Figure 32 shows the improvement in PM due to the bandwidth limiting effect of the feedback network. The UGF of the loop transfer function is 84.1MHz and the PM is 79.6°. Therefore, we can expect an over-damped transient response to a square wave input.

Figure 32: Closed loop AC response demonstrating the improved PM due to the feedback network
Figure 33 shows the rise time and fall time of the output response to an input pulse. The slew rates can be calculated as,

$$ Rising \ SR = \frac{911.7mV}{6.686ns} = 136.36 \frac{V}{\mu s} $$

and

$$ Falling \ SR = \frac{922.3mV}{7.112ns} = 129.68 \frac{V}{\mu s} $$

These values both exceed the 100V/µs requirement.

Figure 33: Transient response to a square-wave input displaying the rising and falling slew rates

Figure 34 shows that the positive overshoot on the falling edge was 29.15mV and the negative overshoot at the rising edge was 8mV. The circuit is critically damped so there is no overshoot at the rising edge or undershoot at the falling edge. This is much less than the 250mV (25%) specification given in the project definition.
Figure 34: Transient response to a square-wave input displaying the positive and negative overshoots

Figure 35 shows that the output signal has settled to within 80.29nV 50ns after the rising edge. The signal was measured to be within 110nV 50ns after the falling edge. This is clearly within the required 1mV.

Figure 35: Transient response to a square-wave input displaying the settling time after the rising and falling edges
The table below summarizes the results and compares them to the requirements given in the project definition. All of the requirements were exceeded.

<table>
<thead>
<tr>
<th></th>
<th>Rising</th>
<th>Falling</th>
</tr>
</thead>
<tbody>
<tr>
<td>Slew Rate</td>
<td>136.36V/µs &gt; 100V/µs</td>
<td>129.68V/µs &gt; 100V/µs</td>
</tr>
<tr>
<td>Overshoot</td>
<td>29.15mV &lt; 250mV</td>
<td>8mV &lt; 250mV</td>
</tr>
<tr>
<td>Settling after 50ns</td>
<td>80.29nV &lt; 1mV</td>
<td>110nV &lt; 1mV</td>
</tr>
</tbody>
</table>

**OUTPUT VOLTAGE SWING RANGE**

Figure 36 shows the test bench used for testing the output voltage swing range. The amplifier is connected in an inverting unity gain configuration. 1MΩ resistors are used so that the resistance at the output is large. A dc-voltage sweep was applied to the input and output was plotted versus the input.

![Diagram of amplifier configuration](image)

**Figure 36: Test bench used for testing output voltage swing range**

Figure 37 shows that that the output linear range is from -2.231V to 2.071V which meets the project requirement because,

\[-2.231V < -1.75V \text{ and } 1.75V < 2.071V\]
The output voltage swing range is limited by the CMFB circuit and large $V_{on}$ voltages for the input pair were used to increase this range.

**INPUT COMMON MODE RANGE**

Figure 38 shows the test bench used to measure the ICMR. A VCVS is used to buffer the output from the input and the amplifier itself is connected as a buffer. A DC sweep is applied at $V_{in+}$ and the CM input range over which the amplifier is still linear is shown by plotting the output of the buffer.

Figure 39 shows the simulation result and shows an ICMR of -2.068V to 1.203V. This meets the project requirement because,
\[ |ICMR| = 1.203V - (-2.068V) = 3.271V > 3V \]

and

\[ -2.068V < -1V \text{ and } 1V < 1.203V \]

Figure 39: Simulation result from the ICMR test

SYSTEMATIC OFFSET VOLTAGE

Figure 40 shows the circuit used to test the systematic offset voltage. The differential output voltage is held at a finite value and due to the high gain of the op-amp the differential input should be nearly 0V without any offset voltage. Because the circuit is completely symmetric, there is no systematic offset voltage and the differential input voltage of -79.91aV can be explained by the non-infinite gain of the amplifier and VCVS.

This zero offset voltage does not imply that the offset voltage after fabrication will also be zero. The amplifier will not be symmetric even with careful layout. There will be a \( V_t \) mismatch between paired transistors that would contribute to an offset voltage. This was minimized by the large area and high order gradient cancelation used for the differential input pair and the non-cascoded NMOS pull-down transistors in the first stage. Layout strategies are discussed in greater detail in a future section.
Figure 40: Test bench used to test the systematic offset voltage

OPEN LOOP DIFFERENTIAL MODE AC RESPONSE

Figure 41 shows the test bench used to measure the open loop differential mode AC response. This was tested to confirm open loop functionality. The AC response was exactly the same as the closed loop response and it is not shown here to avoid redundancy.

Figure 41: Test bench for measuring open loop differential mode AC response

OPEN LOOP COMMON MODE AC RESPONSE

Figure 42 shows the schematic used to test the CMFB circuit. The test was for the entire loop, so Vcmc in the schematic is connected to the $M_{SCM}$ as in normal operation. The loop is broken between the differential outputs and the CMFB circuit inputs. A VCVS is used to generate the DC voltage to balance the amplifier and a common mode AC-voltage source is connected in series.
An AC simulation was performed and the AC response was plotted and it is shown in Figure 43.

The CMFB loop gain is 84.35dB, -3dB point is at 1.177kHz, UGF at 14.43MHz, and the PM is 47.08°. It was very difficult to obtain a stable CMFB loop for the high UGF of the amplifier. Slight variations in circuit conditions would
drop the PM below 45° and make the loop unstable. Therefore, before fabrication, it would be good to lower the UGF of the amplifier to achieve a greater PM of the CMFB loop.

COMMON MODE REJECTION RATIO

Figure 44 shows the test bench used to measure CMRR. From this circuit the CM gain is plotted and the differential mode gain is plotted as presented previously. The calculator function in ADE is then used to plot,

\[
CMRR = \text{dB}20 \left( \frac{A_{DM}}{A_{CM}} \right)
\]

This plot is shown in Figure 45. The DC CMRR is \(\sim132\text{dB}\) which exceeds the 60dB project specification.
The differential power supply rejection ratio is impossible to measure before fabrication for a differential circuit unless transistor mismatches are simulated. This is because the amplifier is made to be perfectly symmetrical in the schematic and any changes at $V_{O+}$ due to power supply variations are directly reflected and then canceled out differentially by the changes at $V_{O-}$. An inverting unity gain configuration was used to measure PSRR. An AC source was placed in series with the DC supply and the gain was measure from the differential output to the supply. Figure 46 and Figure 47 show the positive and negative supply differential PSRR. The magnitude is on the order of 400dB, but is due to approximations made by Spectre.
A better indicator of PSRR is the PSRR of the current source. Figure 48 and Figure 49 show the positive and negative bias circuit PSRR, respectively. These plots indicate the gain from the differential voltage across the resistor (which determines bias current) to the positive and negative supplies. The DC PSRR in both cases is about 84dB which also meets the project requirement.

**INPUT REFERRED NOISE**

The model files for the AMI06 process set the flicker constant, \( K \), to zero. Therefore, the total noise in the circuit comes from the thermal noise of the transistors and the resistors. Figure 50 shows the output equivalent noise of the amplifier. The noise begins to drop by a magnitude of 10 every decade (20dB/decade) at the bandwidth of the amplifier. Figure 51 shows the input referred noise. The noise begins to increase at around 100MHz, but the amplifier has lost most of its gain at that point, so the contribution to the total output noise is negligible.
Figure 50: Output equivalent noise (V/√Hz)

Figure 51: Input referred noise (V/√Hz)

GAIN LINEARITY

Figure 52 shows the test bench used to measure the gain linearity over the output common mode range. A parametric sweep of the DC voltage in the source "/V0" was preformed and the maximum gain (DC gain) was plotted over the entire output common mode range.
Figure 52: Test bench used to measure the gain linearity over the output common mode range

Figure 53 shows the output plot. The maximum DC gain is centered at 0V as expected. Also, at the edges of the output common mode range (reported previously in this report) the gain drops dramatically.

Figure 53: DC gain versus output voltage over the output common mode range

AC RESPONSE LINEARITY

Figure 54 shows the FFT of the output sine wave of a unity inverting configuration op-amp with a 1V and 1 kHz input sine wave. The largest “spur” is 118.8dB, so the spurious free dynamic range (SFDR) is 118.8dB. Figure 55 shows the ADE window displaying the total harmonic distortion (THD) of the same signal. This was calculated using the ADE calculator GUI. The THD is -75.54dB.
Figure 54: FFT of a 1kHz 1V sine-wave output of an inverting unity gain configuration

Figure 55: Analog design environment showing the THD of a 1kHz 1V sine-wave output of an inverting unity gain configuration
CURRENT MIRRORS

It is important for each current source to be closely matched to the bias generator so that the relative current magnitudes are accurate. For this reason, each current mirror is made out of unit transistors. Multipliers are used to ratio the current between branches. Unit transistor current mirrors match well because short channel effects are equivalent and the “birds beak” phenomenon is the same for each transistor. For these reasons, each current mirror was created as a multiple of a unit transistor.

COMMON CENTROID

Two kinds of mismatch can occur when trying to match IC components. The first is random mismatch and can be reduced simply by increasing the area of the component pair to effectively average the random errors. The components should also be placed closely together because the random average can change with the position on the chip.

The second kind of mismatch is caused by gradient effects. To minimize these effects, common centroid layout techniques can be used. In class we talked about a technique to generate an $N^{th}$-order common centroid layout. It is illustrated in the table below.

<table>
<thead>
<tr>
<th>First Order</th>
<th>Second Order</th>
<th>Third Order</th>
<th>Fourth Order</th>
<th>Fifth Order</th>
</tr>
</thead>
<tbody>
<tr>
<td>ABBA</td>
<td>ABBABAAB</td>
<td>ABBABAABBBAABABBA</td>
<td>ABBABAABBBABABBA</td>
<td>ABBABAABBAABABBA</td>
</tr>
</tbody>
</table>

GUARD RINGS

Guard rings can be created by surrounding a component in a ring of well or substrate contacts. This electrically shields the component from the substrate and reduces the injection of substrate noise. In this project, guard rings are used around the critical components such as the PMOS differential input pair and the miller capacitor.

LAYOUT FLOORPLAN

Figure 56 shows the layout floor plan for the amplifier. An axis of symmetry was used for the first and second stages of the amplifier. High order common centroid layout is used for the transistors in the first stage because the mismatches due to these transistors are amplified to the output (as discussed in the equations section). The diodes from the bias circuit are also connected in a common centroid configuration so that their delta voltage is matched properly.
In the following sections, a discussion is given on the layout of individual pieces of the amplifier layout.

**INPUT DIFFERENTIAL PAIR LAYOUT**

The differential input pair contributes more than any other transistor to the offset voltage of the amplifier as shown in a previous section. In order to minimize the offset of the amplifier, it is important that the pair be large to decrease random mismatch errors and have a high order common centroid to cancel gradient errors. Therefore a fifth order common centroid was used for the PMOS input pair in this project. Using the algorithm presented in class, the following layout plan was designed:

```
ABBA BAABBAAB ABBA
BAAB ABBAABBA BAAB
BAAB ABBAABBA BAAB
ABBA BAABBAAB ABBA
```

![Layout floor plan](image)
where A and B as are transistors M1 and M2. Because M1 and M2 share a source, it was possible to use 8 blocks of M=4 transistors and 4 blocks of M=8 for a total of 64 transistors (M=32 for each transistor).

This differential pair is surrounded by a ring of well contacts tied Vdd. This is to shield the input pair from substrate noise as discussed previously.

**FIRST STAGE LAYOUT**

Figure 58 shows the layout of the first stage amplifier. The first thing to note is that M_{3,4}, M_{3c,4c}, and M_{1c,2c} have a 3rd-order common centroid layout. M_{3,4} can be seen at the bottom of the layout. A guard ring was used around these transistors because the noise and $V_t$ mismatch contribution from this pair is only canceled by the ratio of $g_{m3,4}$ to $g_{m1,2}$. Therefore these are the second most important transistors in the layout. The guard ring consists of substrate contacts and is tied to ground.

An axis of symmetry was used for the entire first stage to maintain the symmetry of the amplifier. A symmetric first stage can be connected differentially to mirrored second stages to maintain the symmetry of the interconnects and parasitics. This helps to exploit the benefits of the symmetry of the differential amplifier like even-order harmonic cancelation and a large differential power supply rejection ratio. If symmetry is lost in layout, then these benefits are diminished due to the imbalance of the parasitics.
DIODE LAYOUT

A diode can be created in a MOSFET process by forward biasing the junction between the source/drain diffusion and N-well of a PMOS transistor. For this project, a diode was created using a 5µ x 5µ PMOS transistor with the drain connected to the source and the gate connected to the substrate. The drain source node is the anode of the diode and the gate substrate node is the cathode.

The diodes in this project were used in the bias circuit to create a delta voltage across a resistor to generate a PTAT current. The accuracy of this voltage is dependent on the matching of the area and the saturation current. This is because,

$$\Delta V_{Diode} = V_T \ln \left( \frac{I_{S1}}{I_{S2}} \right) = V_T \ln \left( \frac{A_1 k_1}{A_2 k_2} \right)$$

where

$$k \propto \frac{1}{N_A} + \frac{1}{N_D}$$
Therefore, the area ratio needs to be closely matched, as well as the average doping concentration. This is done by making the diodes out of a unit diode and eight identical diodes surrounding it. This gives a common centroid configuration and good area matching. The results in

\[ \Delta V_{Diode} = V_T \ln \left( \frac{I_{S1}}{I_{S2}} \right) = V_T \ln(8) \]

pretty well independent of process variations. This layout is shown in Figure 59.

![Figure 59: Common centroid diode layout](image)

RESISTOR LAYOUT

There are three resistors used in this design: two resistors in the compensation network and one in the dc bias circuit. The accuracy of these resistances cannot be calculated because we do not have access to the process files for the AMI06 process. The accuracy of a resistance is usually around 15%, though. This number is worse if the area is small, there is a small length to width ratio (low number of squares), or the width of the resistive material is small. Therefore, for this project poly was used to create the resistors and a width of 3 times \( W_{MIN} \) was used (1.8µm).
The diodes and the resistor of the bias circuit were laid out as discussed in the previous two sections. The remaining transistors were laid out and Figure 60 shows the final layout.

Before fabrication, the empty substrate space should be used to create a large bypass capacitor to stabilize the DC voltage of the bias circuit. This was not included at this time due to time constraints.

The matching of the second stage transistors is not as important as the first stage since the \( V_T \) mismatch is rejected by the gain for the first stage when referred to the input. The critical components in the second stage are the compensation resistors and capacitors. The resistor was laid out using the technique discussed in the previous section.
CAPACITOR LAYOUT

The capacitor was made by using the overlap capacitance of the poly1 and poly2 layers. The parasitic fringe capacitance was extracted and accounted for in the layout design. The poly1 plate of the capacitor faces the substrate and has a parasitic capacitance associated with it. Therefore, the top plate (poly2) was connected to the output of the first stage of the amplifier. Therefore, only the capacitance of the poly layers is miller multiplied and the parasitic poly-substrate capacitance is not added to the capacitor $C_1$ which limits the frequency of the second pole. A guard ring was placed around the capacitor to shield it from substrate noise. Also, the edges of the top and bottom plates were surrounded by metal1 contacts and a metal ring. This is to help assure even charge distribution across the high resistance of the poly gates.

CMFB LAYOUT

The layout for the common mode feedback circuit can be seen in Figure 62. The circuit was made to be symmetric across the vertical axis. Before fabrication, it would be good to cross couple the CMFB input transistors to improve their matching.
The final layout is shown in Figure 63. This layout was LVS checked to match against the final schematic. The LVS match is included in appendix A.
With the layout completed, post layout simulation can be performed to gauge the impact of the parasitic capacitance on the AC response of the amplifier.
POST-LAYOUT SIMULATION RESULTS

In this section, the test results for the post-layout amplifier are presented and discussed. The test methods and test benches are the same as the pre-layout simulations and are not included again here.

DIFFERENTIAL MODE GAIN AND STABILITY

Figure 64 shows the post layout AC response. The DC gain is 100.1dB, the bandwidth is 1.388kHz, the UGF is 209.4MHz and the PM is 47.29°.

Although this meets the specifications, the phase margin has decreased by 3°. This is because the $p_2$ and $z_1$ decreased in frequency. This can be seen in Figure 65. Now when the capacitive load is decreased from 2pF, the zero stays in the same location, but the pole moves to higher frequencies.
This effect causes a bump in the transfer function just before the unity gain frequency, greatly increasing the UGF and diminishing phase margin. This is discussed in greater detail in the next section.

**PERFORMANCE VERSUS TEMPERATURE (VARIOUS CAPACITIVE LOADS)**

The AC responses for the amplifier versus temperature and capacitive loads are included in this section. Figure 66 shows the AC response versus temperature from -40°C to 85°C for a 2pF capacitive load.
Figure 66: Post layout AC response versus temperature ($C_L = 2\text{pF}$)

Figure 67 and Figure 68 show the AC responses versus temperature for a $1\text{pF}$ and $0\text{pF}$ capacitive load, respectively.
Figure 68: Post layout AC response versus temperature (C_L=0pF)

The table below summarizes the results. Although, the circuit meets the specifications for the 2pF load, the circuit becomes unstable for smaller capacitive loads. Typically, the maximum capacitive load leads to the worst case PM and stability because it reduces the location of the second pole. For this amplifier, though, the pole was canceling the first zero and as the load capacitor decreases, the pole increases leaving the zero just below the UGF. This causes a bump in the transfer function and greatly increases the UGF (822.5MHz for CL=0pF and Temp=-40°C). At these high UGFs, the amplifier does not have sufficient phase margin and is therefore unstable.

From this I have learned that pole zero cancelation can only be used if the capacitive load is known before hand and is constant. Therefore, it is a good strategy for application specific IC applications, but not for generic amplifiers.

<table>
<thead>
<tr>
<th>Temperature</th>
<th>CL=2pF</th>
<th>CL=1pF</th>
<th>CL=0pF</th>
</tr>
</thead>
<tbody>
<tr>
<td>-40°C</td>
<td>104.3dB</td>
<td>104.3dB</td>
<td>104.3dB</td>
</tr>
<tr>
<td>85°C</td>
<td>95dB</td>
<td>225.4 MHz</td>
<td>279.7 MHz</td>
</tr>
<tr>
<td>Phase Margin</td>
<td>193.3MHz</td>
<td>337 MHz</td>
<td>822.5 MHz</td>
</tr>
<tr>
<td>UGF</td>
<td>46.4°</td>
<td>32.6°</td>
<td>-31°</td>
</tr>
</tbody>
</table>

In the next section, the AC response versus power supply voltage is presented.
PERFORMANCE VERSUS POWER SUPPLY VOLTAGE

Figure 69 shows the AC response of the amplifier versus power supply voltage. For a ±2V supply, the first pole increased while the DC gain decreased keeping the UGF constant. This likely indicates a decrease in the gain of the second stage of the amplifier, which decreases the magnitude of the capacitance due to the compensation capacitor increasing the location of pole 1. This would also clearly decrease the gain.

![Figure 69: Post-layout AC response versus power supply voltage](image)

The table below summarizes the performance of the amplifier versus power supply voltage. It can be seen from the plot in Figure 69 that the amplifier meets the specifications for voltages as low as ±2.25V.

<table>
<thead>
<tr>
<th></th>
<th>±2V Supply</th>
<th>±2.5V Supply</th>
<th>±3V Supply</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Gain</strong></td>
<td>81.93dB</td>
<td>100.1dB</td>
<td>101dB</td>
</tr>
<tr>
<td><strong>Phase Margin</strong></td>
<td>58.12°</td>
<td>47.29°</td>
<td>50.37°</td>
</tr>
<tr>
<td><strong>UGF</strong></td>
<td>182MHz</td>
<td>209.4MHz</td>
<td>207.8MHz</td>
</tr>
</tbody>
</table>

CORNER PERFORMANCE

The plots for the four corners of MOSFET operation are included in this section as Figure 70, Figure 71, Figure 72, and Figure 73.
Figure 70: Post-layout AC response for NMOS fast and PMOS fast

Figure 71: Post-layout AC response for NMOS fast and PMOS slow
The table below summarizes the results from these simulations. It is clear that the project specifications have been met for all corners.

<table>
<thead>
<tr>
<th></th>
<th></th>
<th>GAIN</th>
<th>UGF</th>
<th>PM</th>
<th>-3dB Point</th>
</tr>
</thead>
<tbody>
<tr>
<td>NMOS</td>
<td>PMOS</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Fast</td>
<td>Fast</td>
<td>99.37dB</td>
<td>210.3MHz</td>
<td>48.53°</td>
<td>1.575kHz</td>
</tr>
<tr>
<td>Fast</td>
<td>Slow</td>
<td>99.49dB</td>
<td>196.1MHz</td>
<td>49.42°</td>
<td>1.644kHz</td>
</tr>
<tr>
<td>Slow</td>
<td>Fast</td>
<td>100.6dB</td>
<td>210 MHz</td>
<td>49.82°</td>
<td>1.292kHz</td>
</tr>
<tr>
<td>Slow</td>
<td>Slow</td>
<td>100.3dB</td>
<td>202.7 MHz</td>
<td>49.78°</td>
<td>1.33kHz</td>
</tr>
</tbody>
</table>
In this section, a transient response is analyzed to obtain the slew rate, overshoot, and settling time of the amplifier. Figure 74 shows the positive and negative slew rates which can be calculated to be 131.37 V/µs and 128.67 V/µs, respectively (see below).

\[
\text{Positive SR} = \frac{889.9mV}{6.774ns} = 131.37 \frac{V}{\mu s}
\]

\[
\text{Negative SR} = \frac{871.6mV}{6.774ns} = 128.67 \frac{V}{\mu s}
\]

Figure 75 shows the post layout simulation results for overshoot. As mentioned in the pre-layout simulation results, there is a β of \( \frac{1}{2} \) in the test bench, greatly increasing the phase margin. This is why the positive overshoot at the falling edge is only 28.59mV and the negative overshoot at the rising edge is only 12mV.
Figure 76 shows the settling voltages after 50ns. The output has settled to with 4.93\(\mu\)V 50ns after the rising edge and has settled to 33\(\mu\)V 50ns after the falling edge, which clearly meets the project requirements.
Figure 76: Post layout settling after 50ns

The table below summarizes the results from these simulations and compares them to the project requirements. Clearly all of the specifications have been met.

<table>
<thead>
<tr>
<th></th>
<th>Rising</th>
<th>Falling</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Slew Rate</strong></td>
<td>131.37 V/µs &gt; 100 V/µs</td>
<td>128.67 V/µs &gt; 100 V/µs</td>
</tr>
<tr>
<td><strong>Overshoot</strong></td>
<td>12mV &lt; 250mV</td>
<td>28.6mV &lt; 250mV</td>
</tr>
<tr>
<td><strong>Settling after 50ns</strong></td>
<td>4.83µV &lt; 1mV</td>
<td>33µV &lt; 1mV</td>
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</table>
Figure 77 shows the post layout common mode rejection ratio. It is very similar to the pre-layout CMRR and the DC value (132.4dB) greatly exceeds the project requirement of 60dB.
Figure 78 and Figure 79 show the positive and negative power supply rejection ratios, respectively. Because this is a post layout simulation, the circuit is no longer entirely symmetric so the differential PSRR is not infinite. At extremely low frequencies, both the positive and negative differential PSRR exceeds 200dB. This frequency is $10^6$ Hz, though, which corresponds to a sine-wave with a period of,

$$T = \frac{1}{f} = 10^6 \text{ seconds} = 10^6 \text{s} \cdot \frac{1 \text{ hr}}{3600 \text{s}} \cdot \frac{1 \text{ day}}{24 \text{ hr}} = 11.57 \text{ days}$$

which is unrealistic. It is more realistic to consider the PSRR in the range of $10^1$Hz or 1Hz. For these frequencies, the positive and negative PSRRs are around 110dB which exceeds the project requirement of 60dB.
Figure 80 and Figure 81 show the post layout output noise and the input referred noise. These results are very alike the pre-layout simulations. The noise is bandwidth limited to the output of the amplifier and flicker noise is not observed because the AMI06 BSIM3 model parameters for flicker noise are set to zero in the model file.

Figure 80: Post layout output equivalent noise (V/√Hz)

Figure 81: Post layout input referred noise (V/√Hz)
**GAIN LINEARITY**

Figure 82 shows the post layout DC gain of the amplifier versus output voltage as an indicator of gain linearity. The gain was plotted versus the output common mode voltage range. The peak gain is again at 0V as expected.

![Post layout gain linearity versus output voltage](image)

**AC RESPONSE LINEARITY**

Figure 83 shows the FFT of a 1 kHz 1V sine wave at the output of the amplifier connected in a unity inverting gain configuration. The spurious free dynamic range is 109.2dB as compared to the 118.8dB pre-layout SFDR. This indicates a slight decrease in linearity. Figure 84 shows the ADE window output of the THD of the same signal. The THD is -67.86dB as compared to the -75.54dB pre-layout THD. This again indicates a slight decrease in linearity in the post-layout simulation.
Although, this schematic has been thoroughly designed, there are a few improvements that should be made before it is ready for fabrication. First, the UGF should be lowered to increase the stability of the CMFB loop and the stability of the amplifier. Also, the zero should be placed beyond the UGF so that the circuit is stable for all capacitive loads in post layout simulations.
The compensation capacitor and resistor should be laid out in a common centroid pattern to balance the differential circuit. Also, the circuit should be made to work for 15% variation in $R_Z$ or a trimming circuit should be incorporated.

It would also be helpful to incorporate a bandgap current reference circuit so that current is constant versus temperature.

ESD protection circuitry would need to be added so that it could be tested without damaging the amplifier. Off chip drivers would be necessary to drive the capacitance of the package and impedance matching would be necessary for high frequency measurements.

**CONCLUSIONS AND LESSONS LEARNED**

A fully differential amplifier with 100dB of gain, 200MHz UGF, and 50° of phase margin has been designed. The circuit remained stable and met every design specification in pre-layout simulations and corner tests. The layout was created and an LVS was obtained. The layout was designed to minimize the offset voltage and imbalance of the amplifier.

Post layout simulation was successful for all specifications and at all corners for a 2pF capacitive load. For lower loads, the second pole increased in frequency and the first zero dominated the transfer function near the UGF. This greatly increased the UGF and diminished the phase margin, making the circuit unstable. Future work has been identified before fabrication would be viable.

I learned many things during the design of this amplifier. First and foremost, I learned how difficult it can be to maintain stability while trying to maximize the frequency operation of a differential amplifier. The common mode feedback loop is often less stable than the differential mode loop of the amplifier. The amplifier often needs to be modified to stabilize the CMFB loop. I also learned that pole zero cancelation cannot be done for a generic amplifier. It is possible to make use of this technique if the load capacitance is controllable and known before hand.

Finally, I learned that the parasitic capacitances of the layout can adversely affect the performance of the amplifier. This is something that I knew going into the project, but had not experienced firsthand until I performed post layout simulation. The increased capacitance at the $C_1$ node was enough to cause the circuit to be unstable for low load capacitances even though it was stable in pre-layout simulations.

I will probably not fabricate this circuit choosing instead to work to get the second project in a state ready for fabrication.
APPENDIX

A: LVS MATCH OUTPUT FILE

Command line: /usr/local/cadence/IC5141/tools.lnx86/dfII/bin/32bit/LVS.exe -dir
/home/boesch/Classes/Masters/Fall/EE501/Labs/LVS -l -s -t
/home/boesch/Classes/Masters/Fall/EE501/Labs/LVS/layout
/home/boesch/Classes/Masters/Fall/EE501/Labs/LVS/schematic

Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.

Net-list summary for /home/boesch/Classes/Masters/Fall/EE501/Labs/LVS/layout/netlist

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<tr>
<th>count</th>
<th>nets</th>
<th>terminals</th>
<th>res</th>
<th>cap</th>
<th>pmos</th>
<th>nmos</th>
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<td>3</td>
<td>2</td>
<td>157</td>
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Net-list summary for /home/boesch/Classes/Masters/Fall/EE501/Labs/LVS/schematic/netlist

<table>
<thead>
<tr>
<th>count</th>
<th>nets</th>
<th>terminals</th>
<th>res</th>
<th>cap</th>
<th>pmos</th>
<th>nmos</th>
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</thead>
<tbody>
<tr>
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<td>3</td>
<td>2</td>
<td>23</td>
<td>23</td>
<td></td>
</tr>
</tbody>
</table>

Terminal correspondence points
N42    N38    Vcm
N20    N16    Vdd
N40    N35    Vin+
N39    N34    Vin-
N13    N7     Vo+
N34    N25    Vo-
N41    N36    Vss

Devices in the rules but not in the netlist:
  nfet pfet nmos4 pmos4

The net-lists match.

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