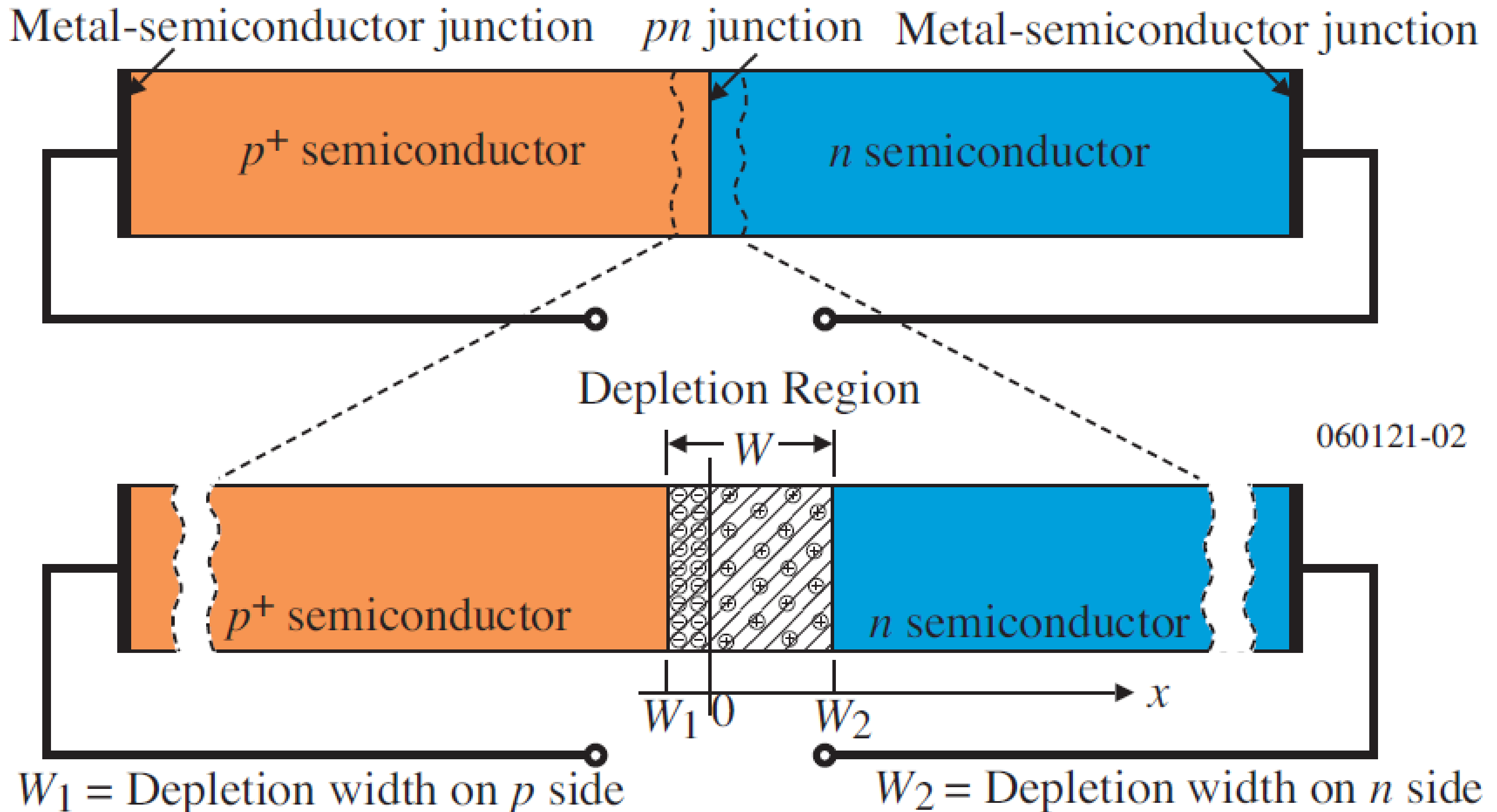
CMOS Devices

- PN junctions and diodes
- NMOS and PMOS transistors
- Resistors
- Capacitors
- Inductors
- Bipolar transistors

PN Junctions

- Diffusion causes depletion region
- D.R. is insulator and establishes barrier
- This leads to 1-directional current flow
- Forms junction capacitor
  - Capacitance highly voltage dependent
  - Can be nuisance or benefits

PN Junctions



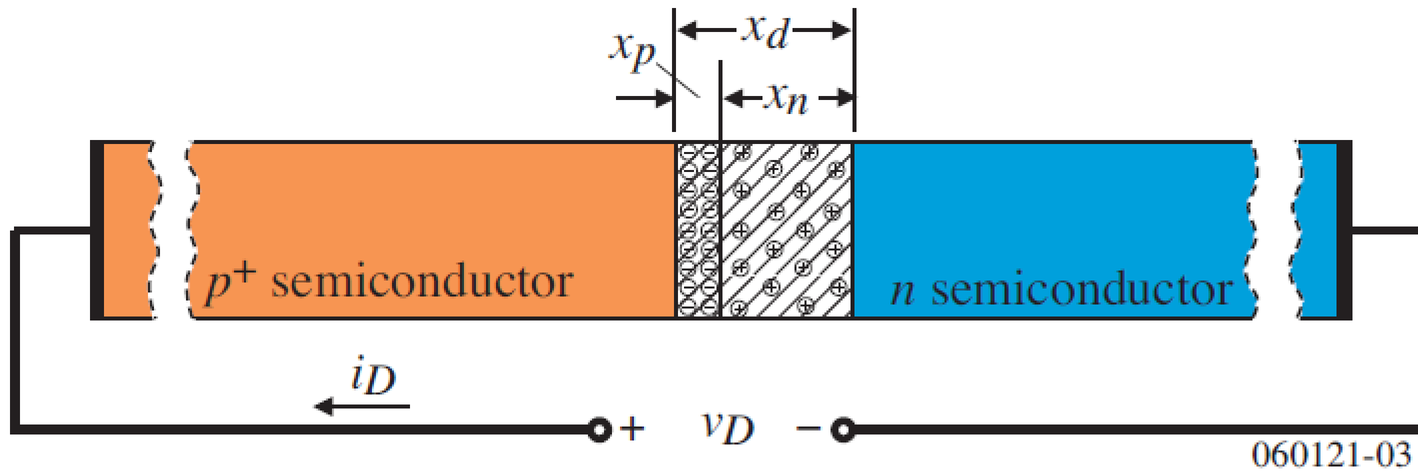
pn junction

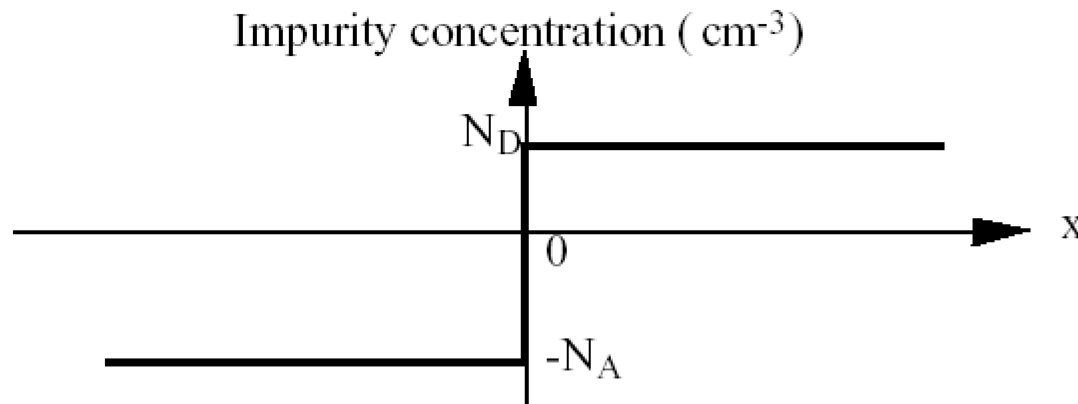
1. Doped atoms near the metallurgical junction lose their free carriers by diffusion.
2. As these fixed atoms lose their free carriers, they build up an electric field, which opposes the diffusion mechanism.
3. Equilibrium conditions are reached when:

Current due to diffusion = Current due to electric field

PN Junctions

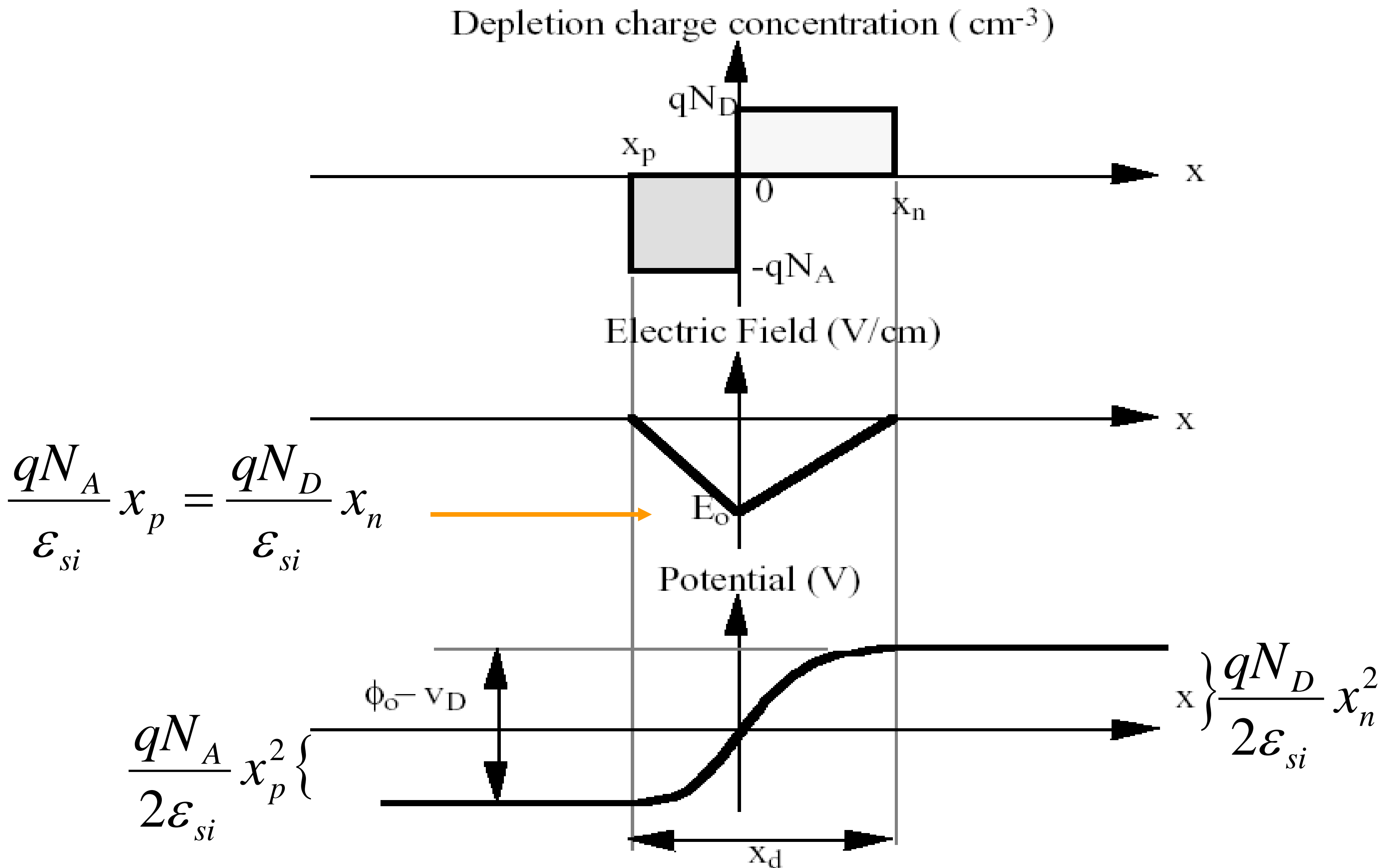
Cross-section of an ideal pn junction:





Initial impurity concentration

PN Junctions



PN Junctions

$$\phi_o - v_D = \frac{q}{2\varepsilon_{si}}(N_A x_p^2 + N_D x_n^2) = \frac{qN_A x_p^2}{2\varepsilon_{si}}(1 + \frac{N_A}{N_D})$$

Depletion region widths:

$$x_n = \left(\frac{2\varepsilon_{si}(\phi_0 - v_D)N_A}{qN_D(N_A + N_D)} \right)^{1/2}$$

$$x_p = -\left(\frac{2\varepsilon_{si}(\phi_0 - v_D)N_D}{qN_A(N_A + N_D)} \right)^{1/2}$$

$$x_d \propto \sqrt{\frac{1}{N}}$$

$$\left| x_n / x_p \right| = N_A / N_D$$

Built-in potential:

$$\varphi_o = \frac{kT}{q}\ln(\frac{N_A N_D}{n_i^2}) = V_t \ln(\frac{N_A N_D}{n_i^2})$$

Example

- NA=10^15 atoms/cm^3, ND=10^16, vD=-10
- Ni=2.25*10^20
- Phi_o=26ln(10^15*10^16/2.25/10^20)=638 mV
- xp= - 3.5 μm
- xn= 0.35 μm
- Max field = q*NA*xp/ε = -5.4*10^4 V/cm

Note the large magnitude of the field

Excercise

- Suppose that $v_D = 0$, $\psi_o = 0.637V$ and $N_D = 10^{17}$ *atoms/cm3.*
- If $N_A = 10^{15}$ *atoms/cm3*

    p-side depletion width = ??

    n-side depletion width = ??

- *If* $N_A = 10^{19}$ *atoms/cm3:*

    p-side depletion width = ??

    n-side depletion width = ??

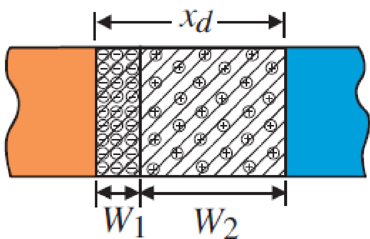
PN Junctions

The depletion charge

$$Q_j = \left|AqN_A x_p\right| = AqN_D x_n = A\left(\frac{2\varepsilon_{si} qN_A N_D}{N_A + N_D}\right)^{1/2} (\phi_0 - v_D)^{1/2}$$

The junction capacitance

$$C_j = \frac{dQ_j}{dv_D} = A\left(\frac{2\varepsilon_{si} qN_A N_D}{N_A + N_D}\right)^{1/2} \frac{1}{(\phi_0 - v_D)^{1/2}} = \frac{C_{j0}}{(1 - v_D/\phi_0)^m}$$



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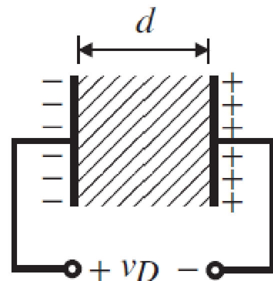
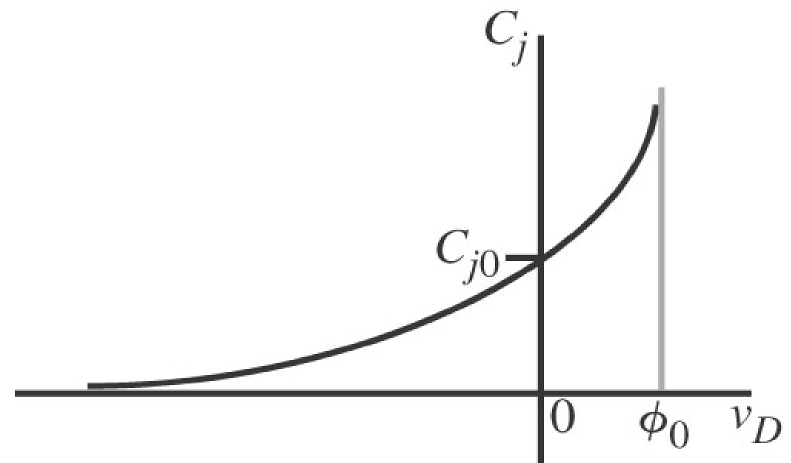
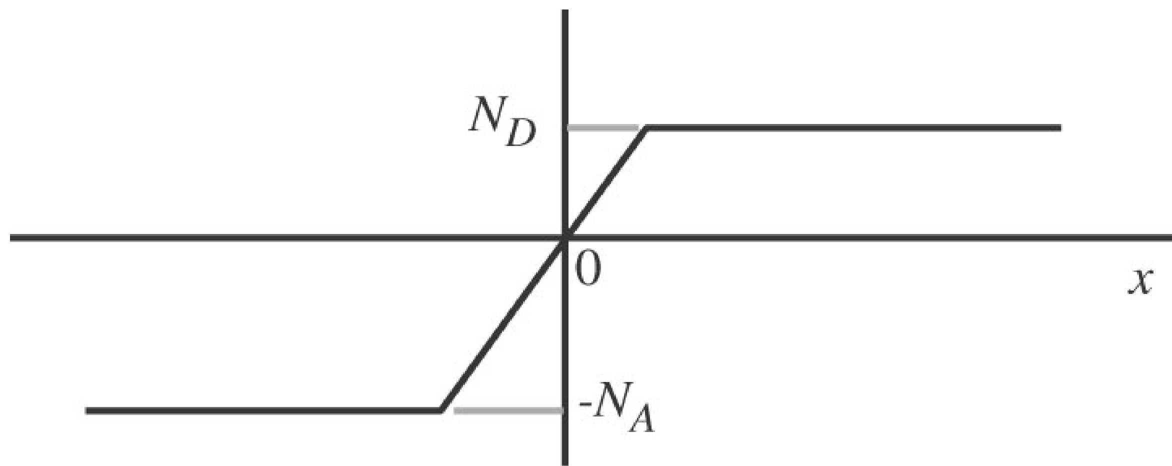
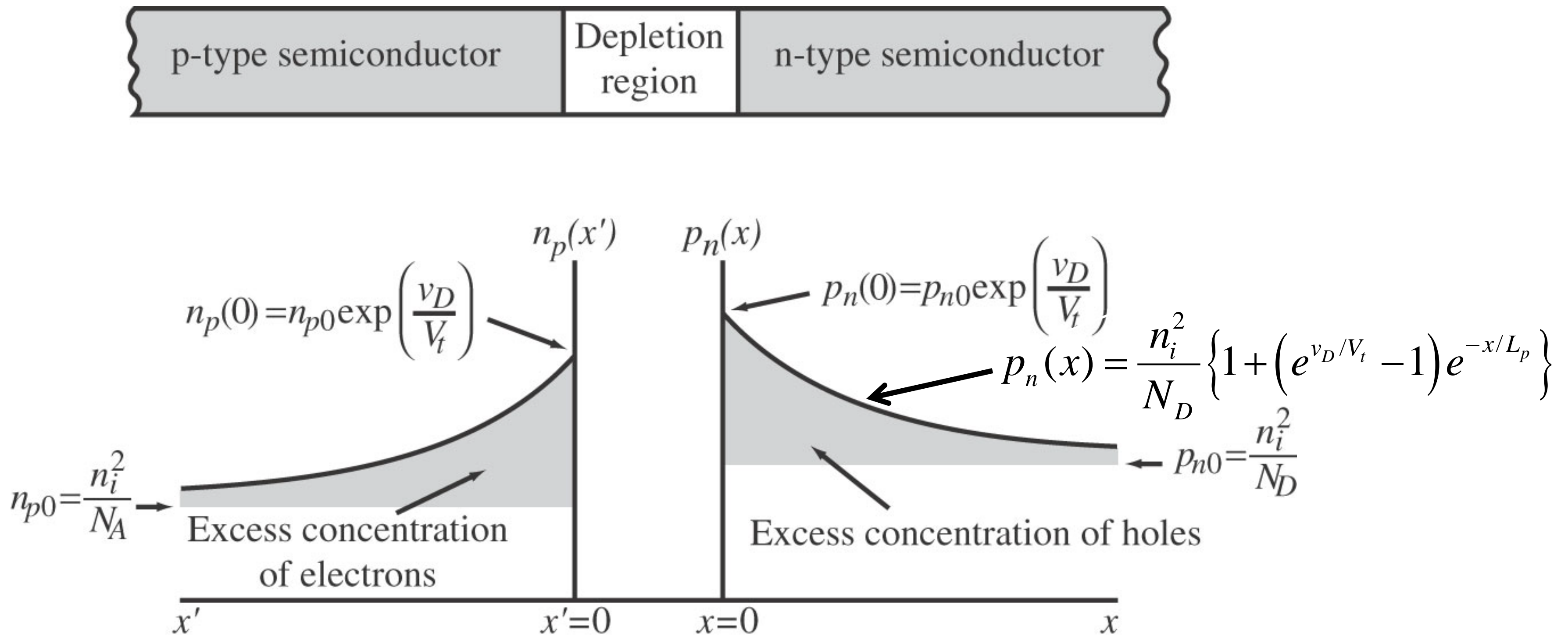




- Can be used as voltage controlled capacitor
- Here m = 1/2 for the step change in impurity concentration.
- For gradual concentration change, m = 1/3.



Impurity concentration profile for diffused pn junction



Current density at boundary due to wholes:

$$J_p(x) = -qD_p \left. \frac{dp_n(x)}{dx} \right|_{x=0}$$

$$J_p(0) = \frac{qD_p n_i^2}{N_D L_p} \left\{ e^{v_D/V_t} - 1 \right\}$$

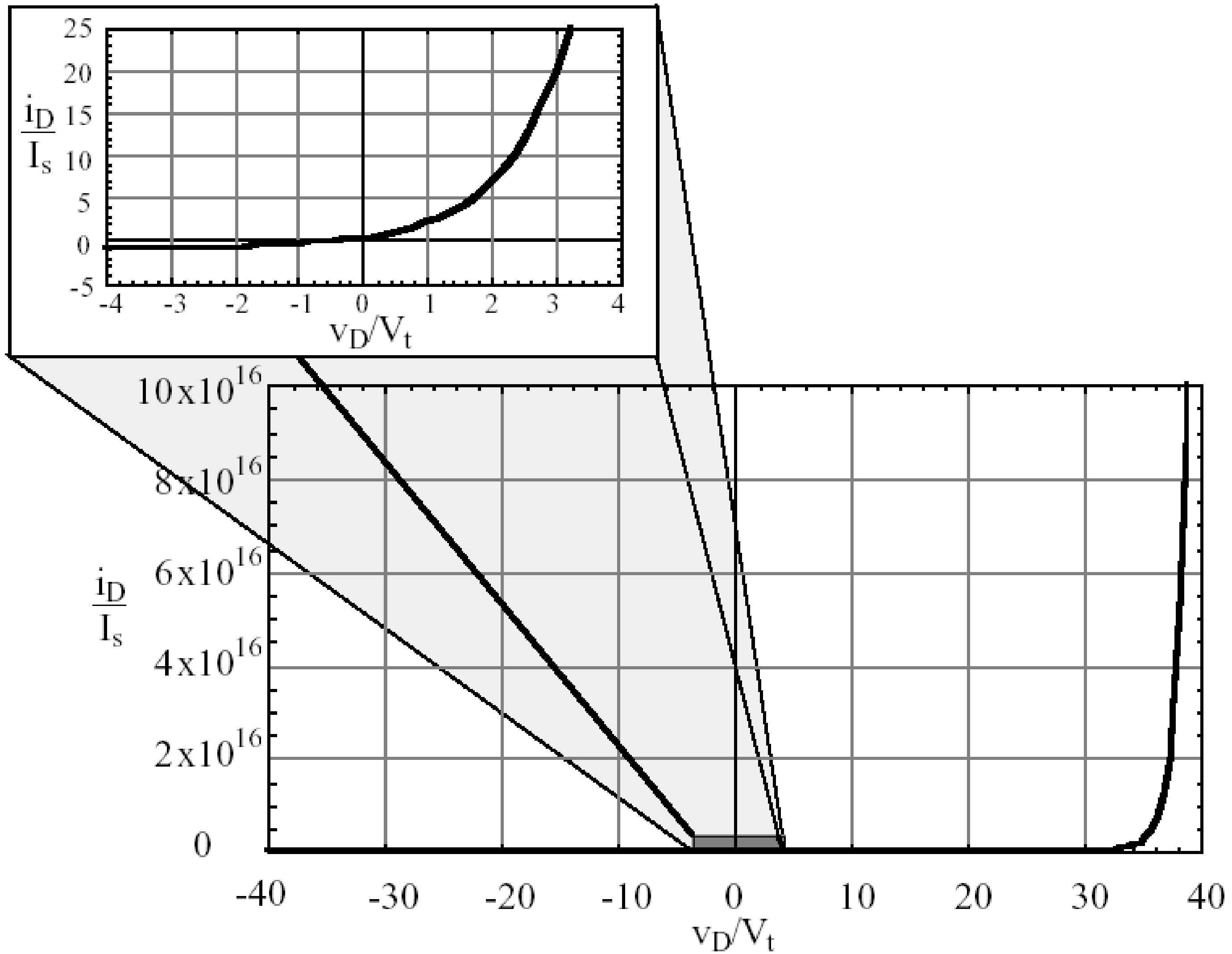
Total:

$$J(0) = J_p(0) + J_n(0) = qn_i^2 \left(\frac{D_p}{N_D L_p} + \frac{D_n}{N_A L_n} \right) \left\{ e^{v_D/V_t} - 1 \right\}$$

Diode current:

$$i_D = AJ(0) = qn_i^2 A \left(\frac{D_p}{N_D L_p} + \frac{D_n}{N_A L_n} \right) \left\{ e^{v_D/V_t} - 1 \right\} = I_S \left\{ e^{v_D/V_t} - 1 \right\}$$

$$i_D = I_S \left\{ e^{v_D/V_t} - 1 \right\}$$



Reverse-Biased *PN* Junctions

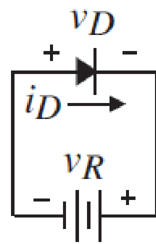
Depletion region:

$$x_d = x_p + x_n = W_1 + W_2$$

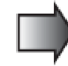
$$x_p = W_1 \propto \sqrt{v_R}$$

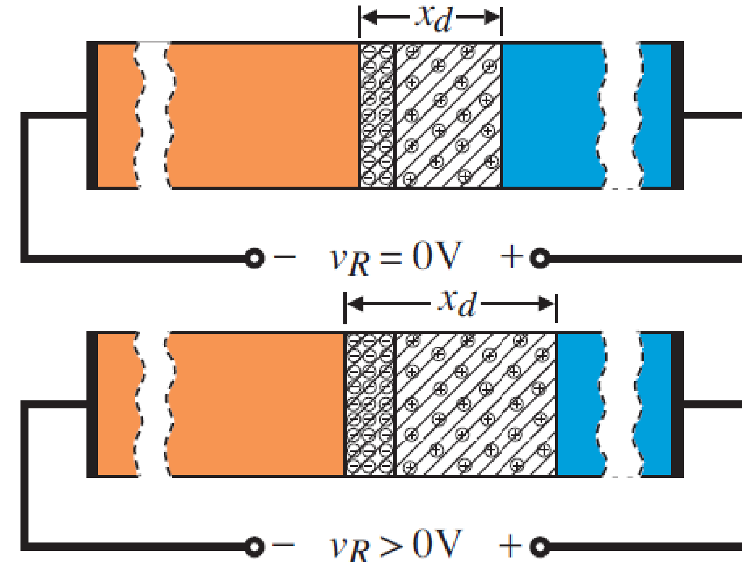
and

$$x_n = W_2 \propto \sqrt{v_R}$$



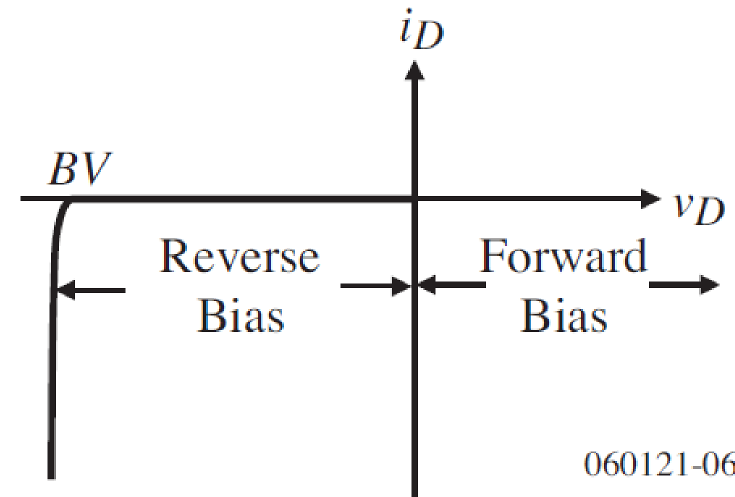
Influence of v_R on depletion region width





Breakdown voltage (*BV*):

If $v_R > BV$, avalanche multiplication will occur resulting in a high conduction state as illustrated.



Breakdown Voltage

Our book shows that

$$BV \approx \frac{\varepsilon_{si}(N_A + N_D)}{2qN_AN_D} E_{max}^2$$

where $E_{max} = 3\text{x}10^5$ V/cm for silicon.

An example:

Assume that $N_D = 10^{17}$ atoms/cm^3.

Find BV if $N_A = 10^{15}$ atoms/cm^3 and if $N_A = 10^{19}$ atoms/cm^3:

$N_A = 10^{15}$ atoms/cm^3:

$$\text{If } N_A << N_D, \text{ then } BV \approx \frac{\varepsilon_{si}}{2qN_A} E_{max}^2 = \frac{1.04\text{x}10^{-12} \cdot 9\text{x}10^{10}}{2 \cdot 1.6\text{x}10^{-19} \cdot 10^{15}} = 291\text{V}$$

$N_A = 10^{19}$ atoms/cm^3:

$$\text{If } N_A >> N_D, \text{ then } BV \approx \frac{\varepsilon_{si}}{2qN_D} E_{max}^2 = \frac{1.04\text{x}10^{-12} \cdot 9\text{x}10^{10}}{2 \cdot 1.6\text{x}10^{-19} \cdot 10^{17}} = 2.91\text{V}$$

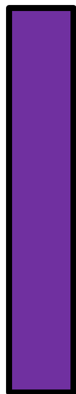
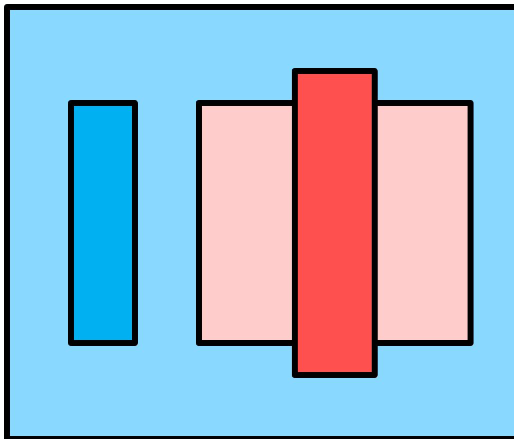
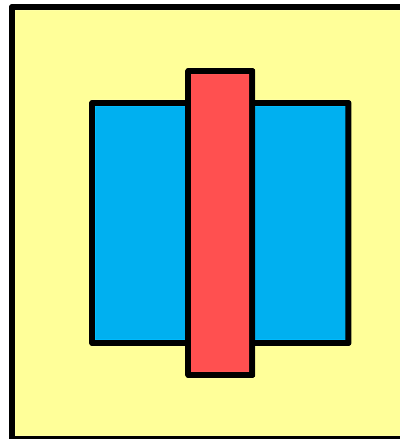
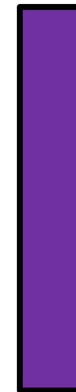
Metal-Semiconductor Junctions

- Ohmic Junctions:
  - A pn junction formed by a highly doped semiconductor and metal
  - Behaves like resistor
- Schottky Junctions:
  - A pn junction formed by a lightly doped semiconductor and metal
  - Behaves like a diode

The MOS Transistors

Substrate Salicide
Substrate Salicide
Well Salicide
W
W
n^+
p^+
p^+
L
n^+
n^+
L
Shallow Trench Isolation
n-well
Shallow Trench Isolation
Substrate
070322-02

Gate Ox	Oxide	*p*+	*p*	*p*-	*n*-	*n*	*n*+	Poly	Salicide	Polycide	Metal

Capacitors

- Two conductor plates separated by an insulator form a capacitor
- Intentional capacitors vs parasitic capacitors
- Linear vs nonlinear capacitors

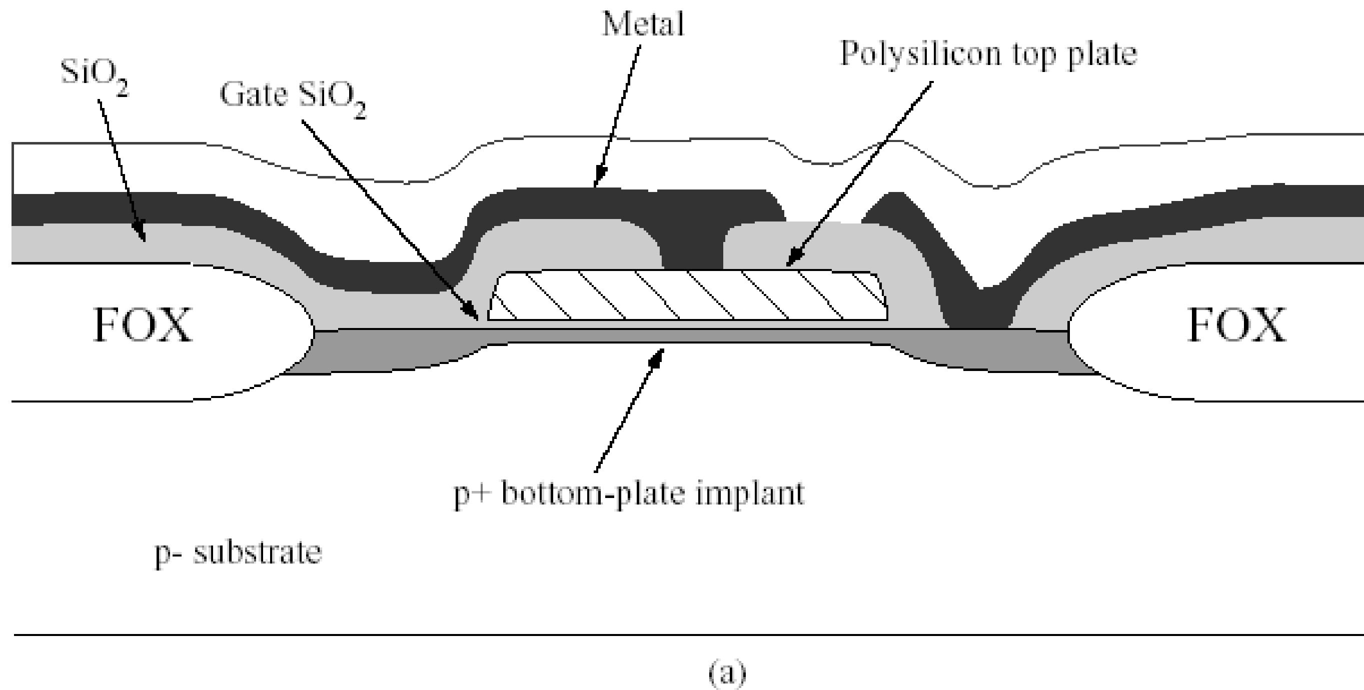
Linear capacitors:

$$C = \frac{\varepsilon_{ox} A}{t_{ox}} = C_d A$$

Capacitor specifications

1. Dissipation (quality factor) of a capacitor
2. Parasitic capacitors to ground from each node of the capacitor.
3. The density of the capacitor in Farads/area.
4. The absolute and relative accuracies of the capacitor.
5. The *Cmax/Cmin ratio which is the largest value of capacitance to the smallest when* the capacitor is used as a variable capacitor (*varactor).*
6. The variation of a variable capacitance with the control voltage (is it linear).
7. Linearity, $q = Cv$.

PMOS on Substrate Gate Capacitors

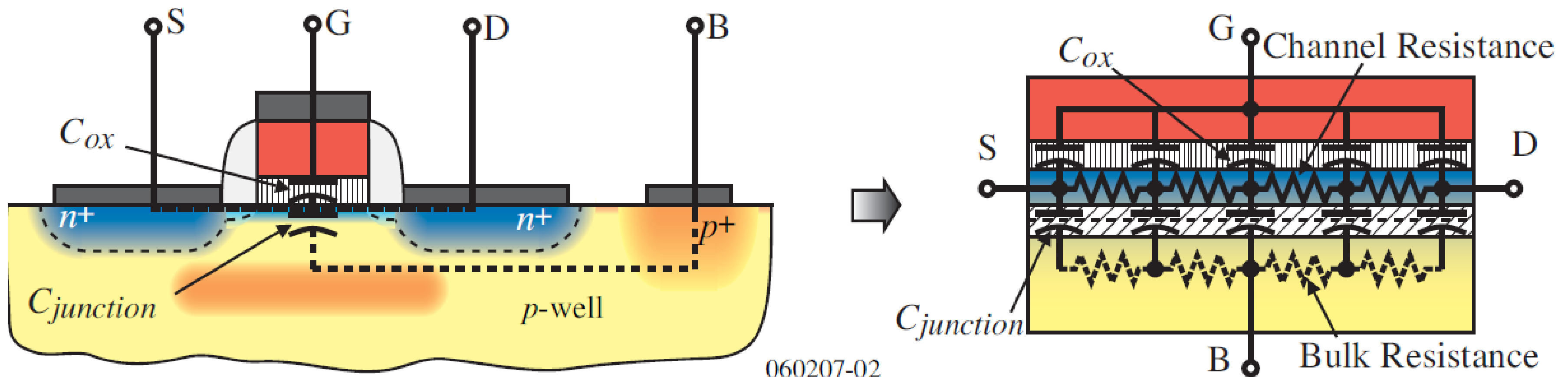


(a) Polysilicon-oxide-channel

High density, good matching, but nonlinear

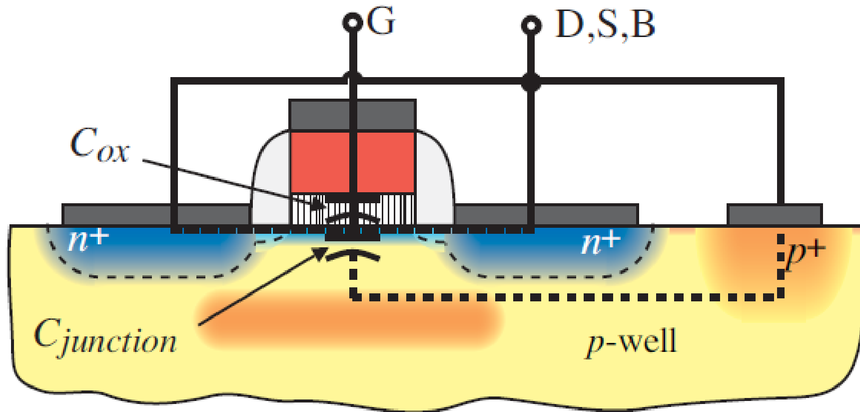
NMOS in p-well Gate Capacitor

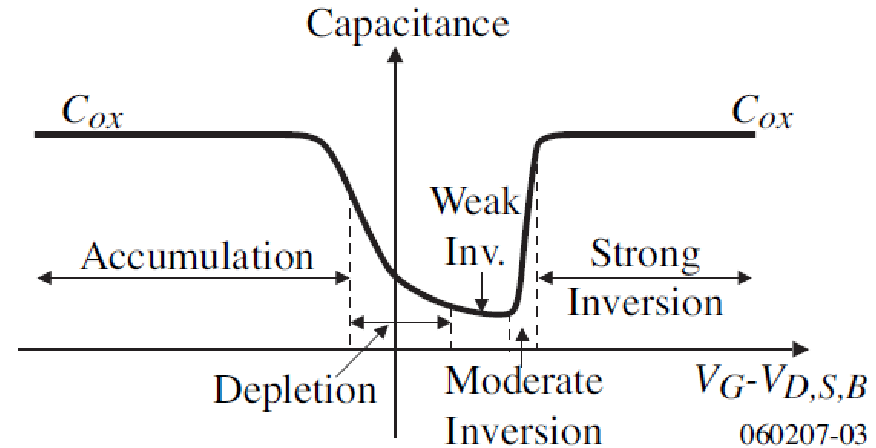
- Gate as one terminal of the capacitor
- Some combination of the source, drain, and bulk as the other terminal



$$C_{\text{gate}} = \frac{1}{\dfrac{1}{C_{ox}} + \dfrac{1}{C_j}}$$

Gate Capacitor vs V_{GS} *with D=S=B*





Operation:

In this configuration, the MOSFET gate capacitor has 5 regions of operation as V_{GS} is varied. They are:

1.) Accumulation
2.) Depletion
3.) Weak inversion
4.) Moderate inversion
5.) Strong inversion

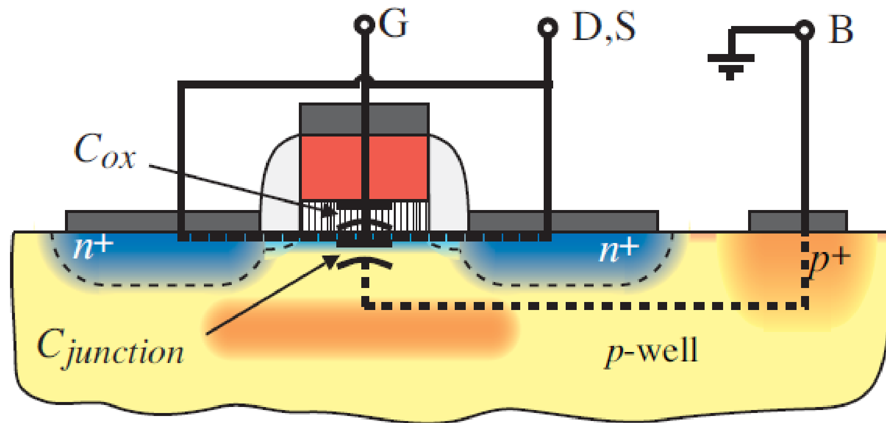
For the first four regions, the gate capacitance is the series combination of C_{ox} and C_j given as,

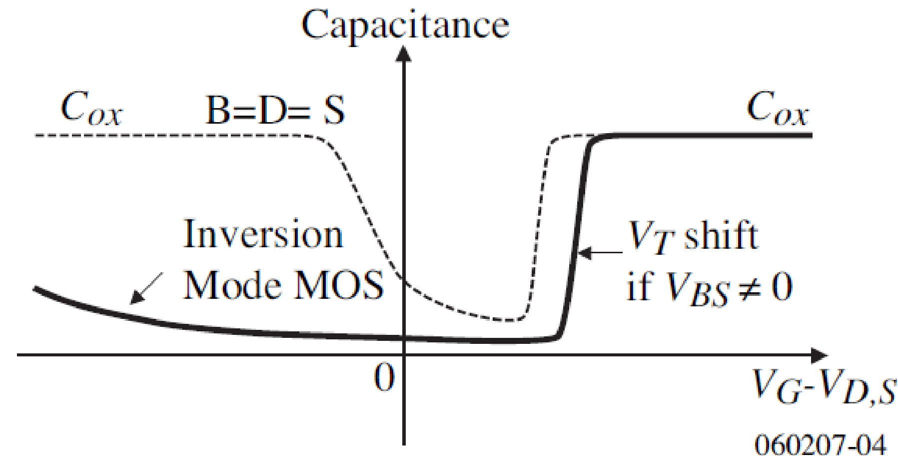
$$C_{\text{gate}} = \frac{1}{\frac{1}{C_{ox}} + \frac{1}{C_j}}$$

3-seg Approximation

Region	Channel R	C_{ox} and C_j	C_{gate}	3-Segment Model
Accumulation	Large	In series and $C_j > C_{ox}$	$C_{gate} \approx C_{ox}$	G, C_{ox}, S, D, C_j, B; $\approx C_{ox}$; S, D, B; 070218-01
Depletion	Large	In series and $C_j \approx C_{ox}$	$C_{gate} \approx 0.5C_{ox} \approx 0.5C_j$	G, C_{ox}, S, D, C_j, B; $\approx \frac{C_{ox}}{2}$; S, D, B; 070218-02
Weak Inversion	Large	In series and $C_j < C_{ox}$	$C_{gate} \approx C_j$	G, C_{ox}, S, D, C_j, B; $\approx C_j$; S, D, B; 070218-03
Moderate Inversion	Moderate	In series and $C_j < C_{ox}$	$C_j < C_{gate} < C_{ox}$	G, C_{ox}, S, D, C_j, B; $\approx C_j // C_{ox}$; S, D, B; 070218-04
Strong Inversion	Small	In parallel and $C_j < C_{ox}$	$C_{gate} \approx C_{ox}$	G, C_{ox}, S, D, C_j, B; $\approx C_{ox}$; S, D, B; 070218-05

Gate Capacitor *in Inversion Mode*





Conditions:

- D = S, B = V_{SS}
- Accumulation region removed by connecting bulk to V_{DD}
- Nonlinear
- Channel resistance:

$$R_{on} = \frac{L}{12K_P'(V_{BG}-|V_T|)}$$

- LDD transistors will give lower Q because of the increased series resistance

Inversion Mode NMOS Capacitor

Best results are obtained when the drain-source are connected to ac ground.

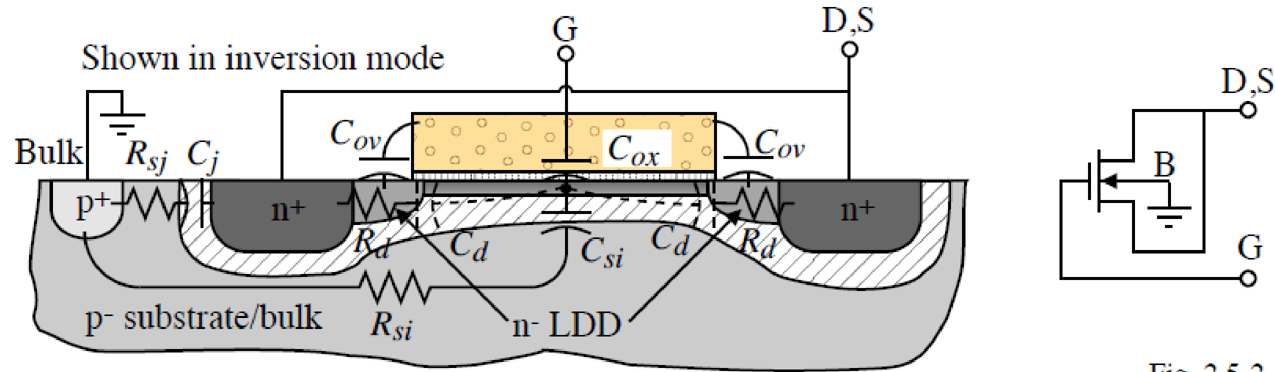


Fig. 2.5-2

Experimental Results (Q at 2GHz, 0.5μm CMOS)†:

C_{max} C_{min} Q_{max} Q_{min}

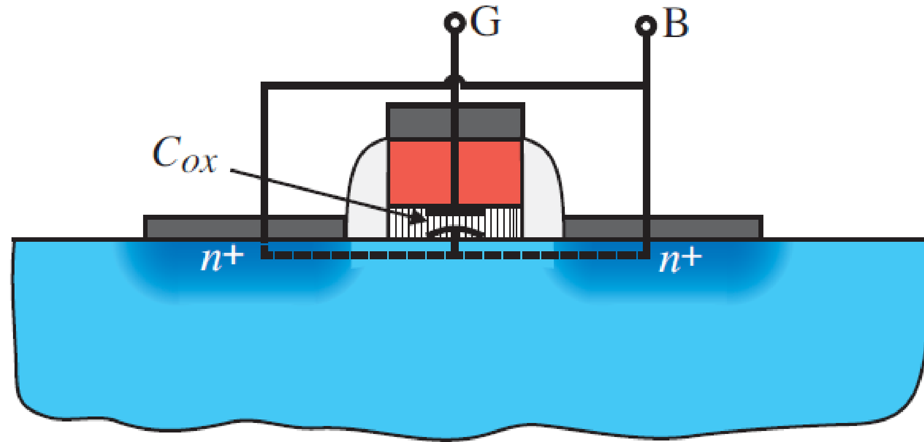
C_{Gate} (pF) / Q_{Gate} vs. Drain/Source Voltage (V); V_G = 2.1V, V_G = 1.8V, V_G = 1.5V; RX Meter, V_G, $V_{D,S}$

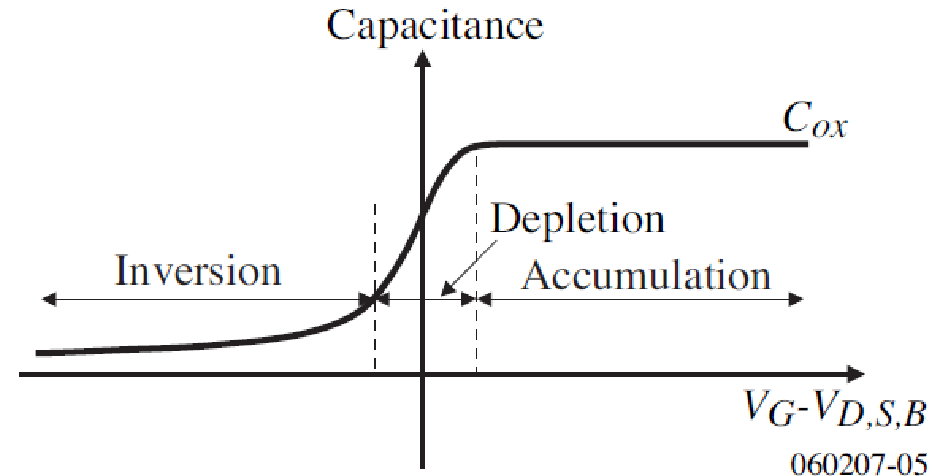
070617-06

V_G =1.8V: C_{max}/C_{min} ratio = 2.15 (1.91), Q_{max} = 34.3 (5.4), and Q_{min} = 25.8(4.9)

† E. Pedersen, "RF CMOS Varactors for 2GHz Applications," *Analog Integrated Circuits and Signal Processing, vol. 26, pp. 27-36, Jan. 2001.*

Accumulation NMOS Gate Cap in n-well





Conditions:

- Remove p^+ drain and source and put n^+ bulk contacts instead.
- Implements a variable capacitor with a larger transition region between the maximum and minimum values.
- Reasonably linear capacitor for values of $V_{GB} > 0$

Accumulation Mode NMOS Gate Cap

Best results are obtained when the drain-source are on ac ground.

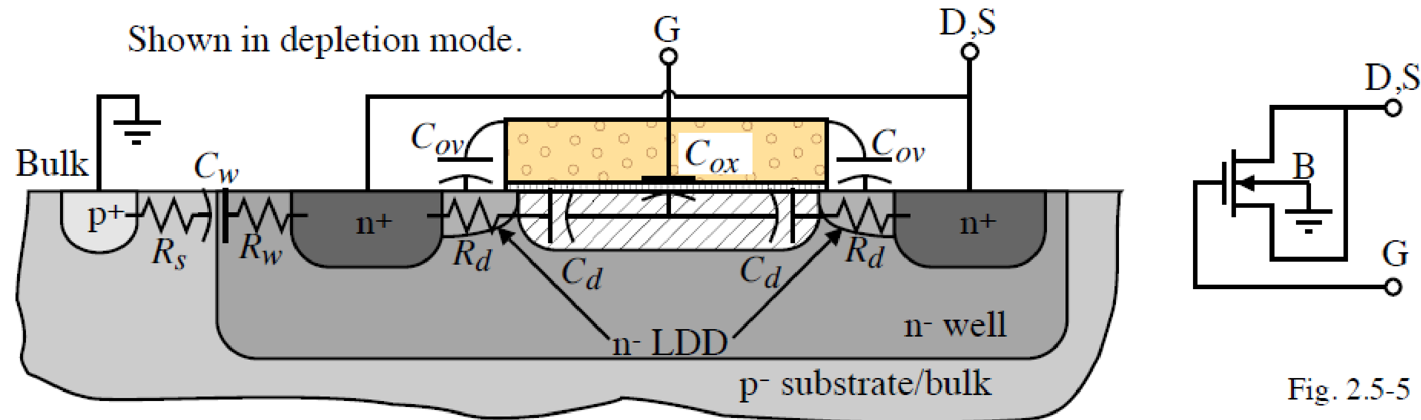
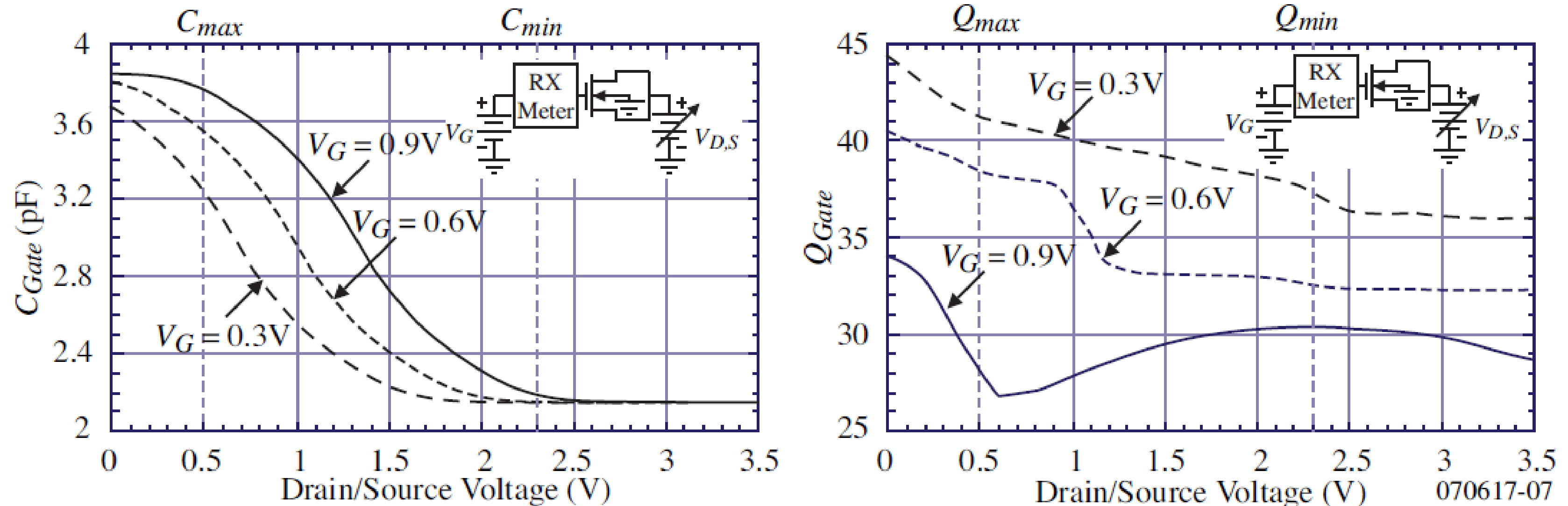


Fig. 2.5-5

Experimental Results (Q at 2GHz, 0.5μm CMOS)[†]:

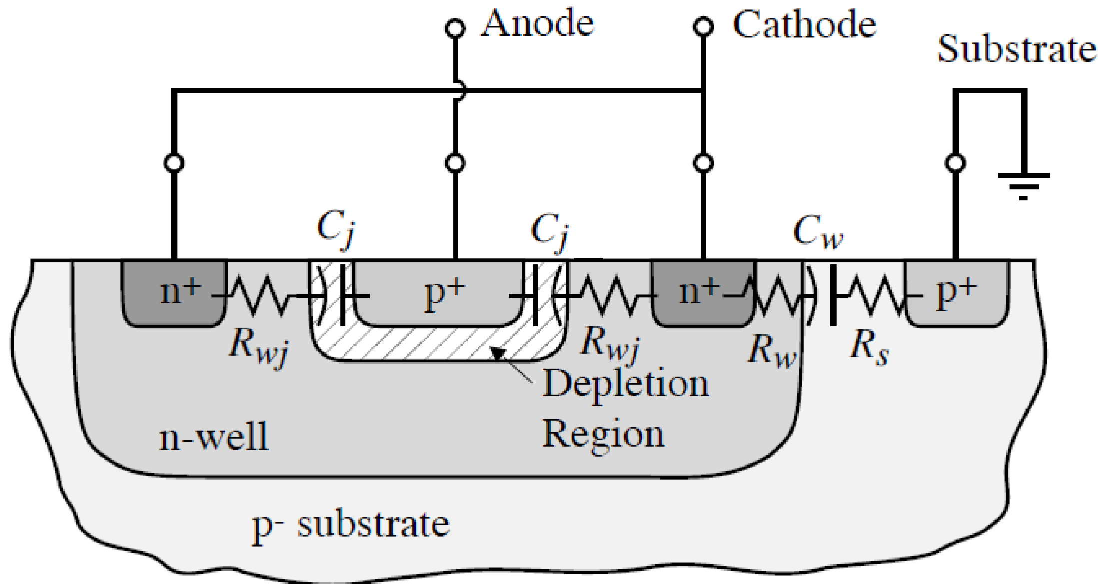


$V_G = 0.6$V: C_{max}/C_{min} ratio = 1.69 (1.61), Q_{max} = 38.3 (15.0), and Q_{min} = 33.2(13.6)

E. Pedersen, "RF CMOS Varactors for 2GHz Applications," *Analog Integrated Circuits and Signal Processing, vol. 26, pp. 27-36, Jan. 2001.*

PN Junction Capacitors in a Well

Generally made by diffusion into the well.



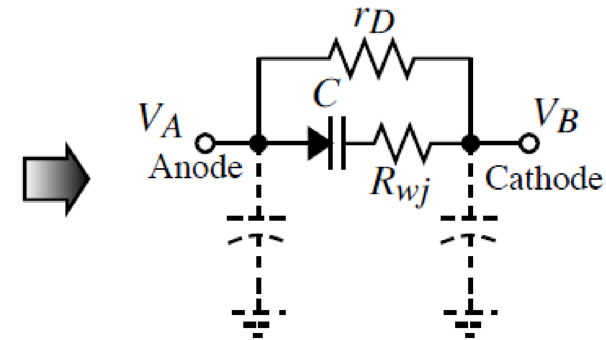


Fig. 2.5-011

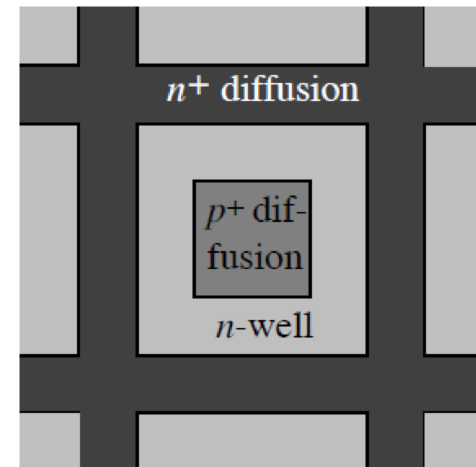
Layout:

Minimize the distance between the $p+$ and $n+$ diffusions.

Two different versions have been tested.

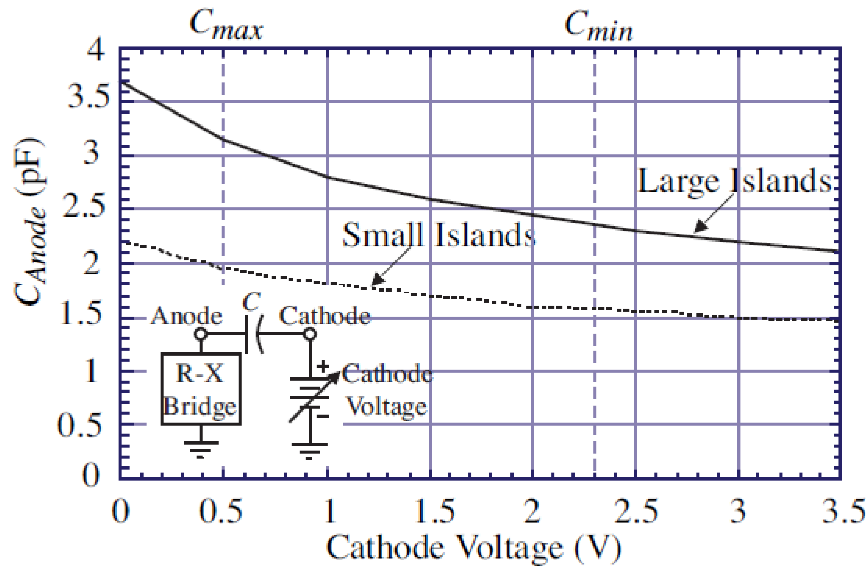
1.) Large islands – 9μm on a side

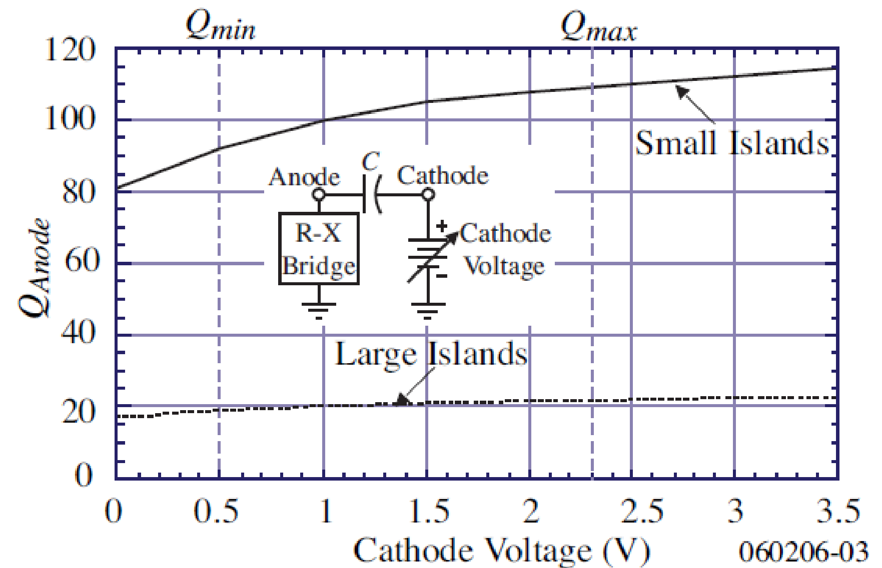
2.) Small islands – 1.2μm on a side



PN-Junction Capacitors

The anode should be the floating node and the cathode must be connected to ac ground.
Experimental data (Q at 2GHz, 0.5μm CMOS)†:



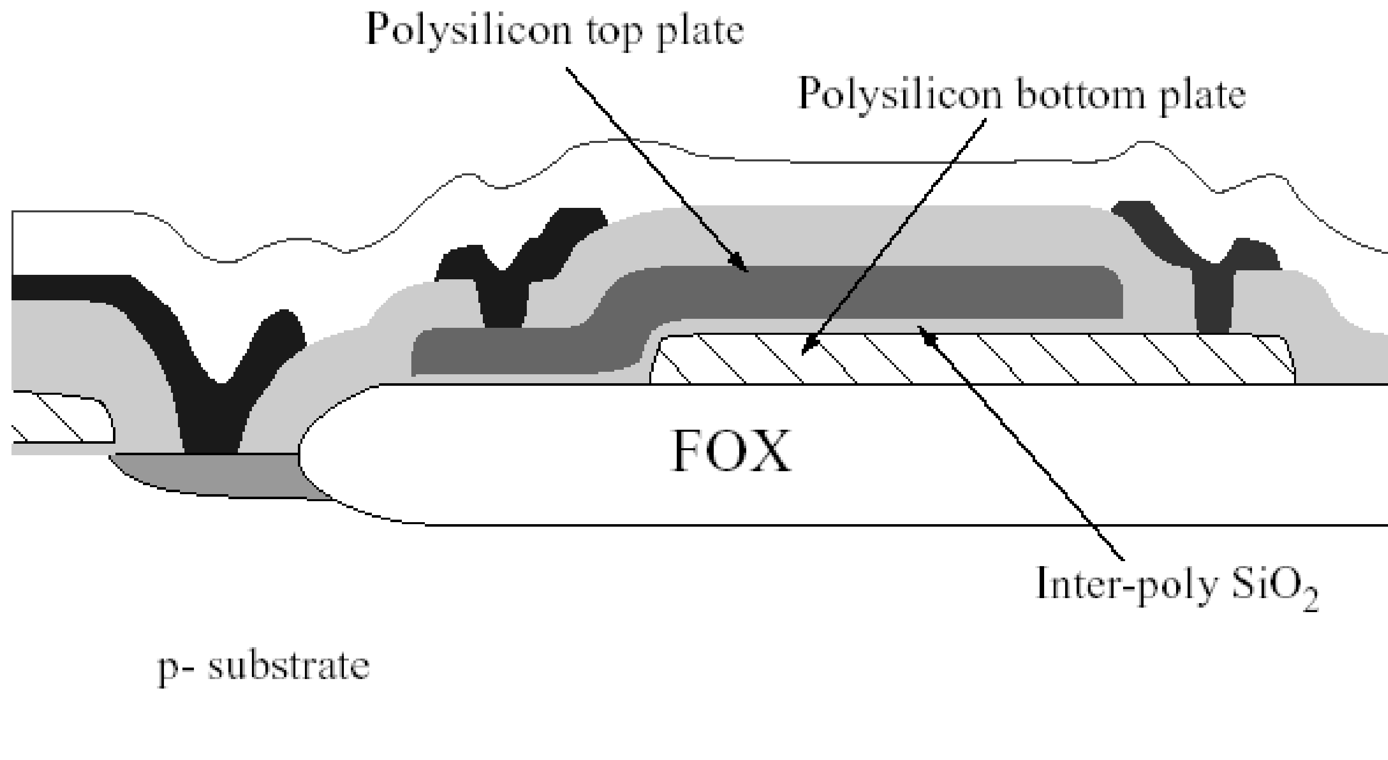


Terminal Under Test	Small Islands (598 1.2μm x1.2μm)			Large Islands (42 9μm x 9μm)		
	C_{max}/C_{min}	Q_{min}	Q_{max}	C_{max}/C_{min}	Q_{min}	Q_{max}
Anode	1.23	94.5	109	1.32	19	22.6
Cathode	1.21	8.4	9.2	1.29	8.6	9.5

Electrons as majority carriers lead to higher Q because of their higher mobility.
The resistance, R_{wj}, is reduced in small islands compared with large islands $\Rightarrow$ higher Q

E. Pedersen, "RF CMOS Varactors for 2GHz Applications," *Analog Integrated Circuits and Signal Processing, vol. 26, pp. 27-36, Jan. 2001.*

Poly-poly cap on FOX

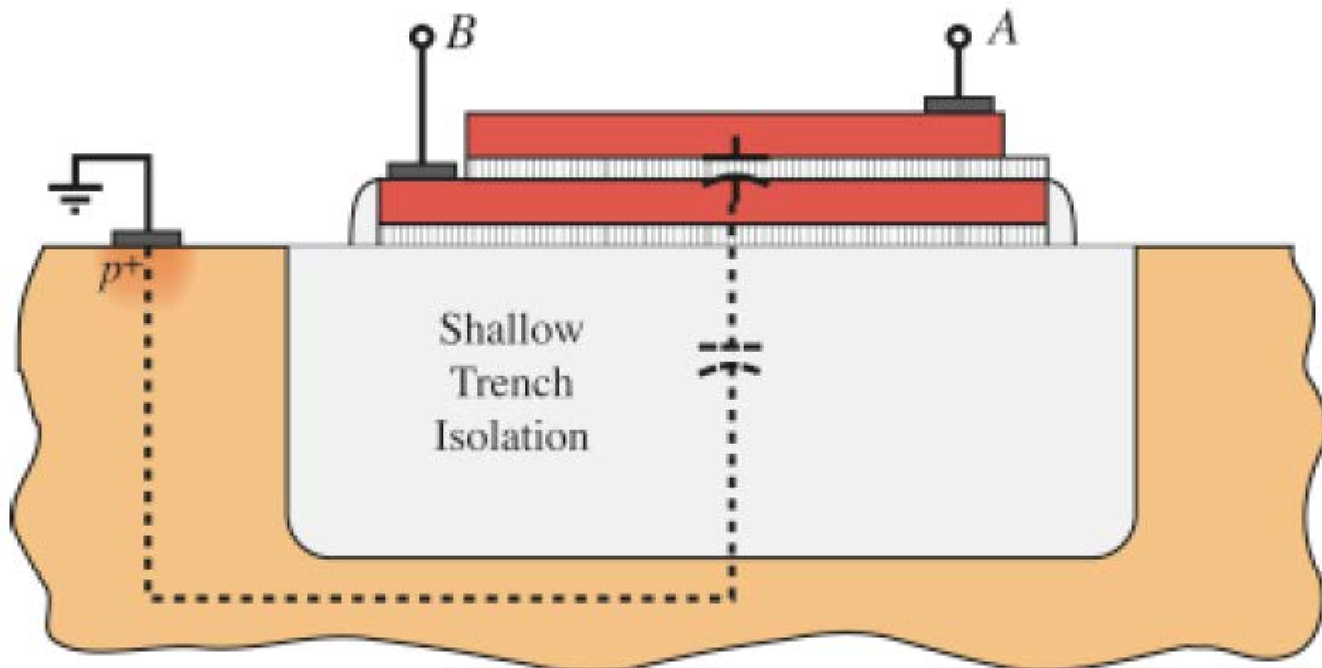


(b) Polysilicon-oxide-polysilicon

High density, good matching, good linearity, but require two-poly processes

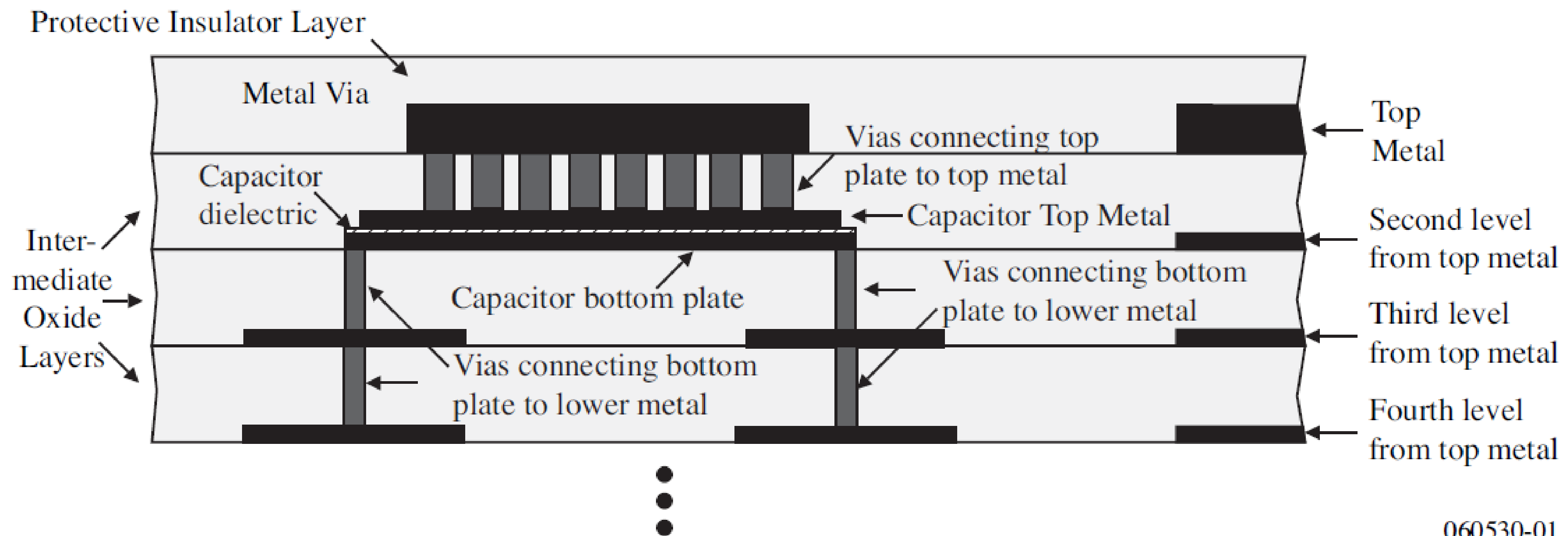
Poly-poly cap on STI

- Very linear
- Small bottom plate parasitics



Metal-insulator-metal cap

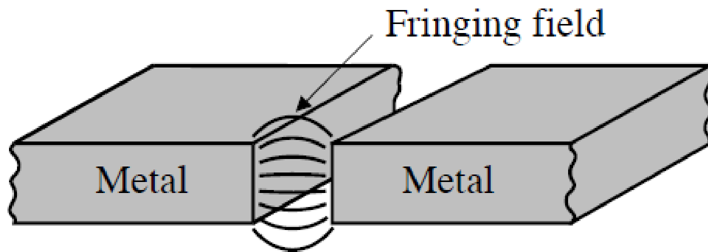
In some processes, there is a thin dielectric between a metal layer and a special metal layer called "capacitor top metal". Typically the capacitance is around $1\text{fF}/\mu\text{m}^2$ and is at the level below top metal.



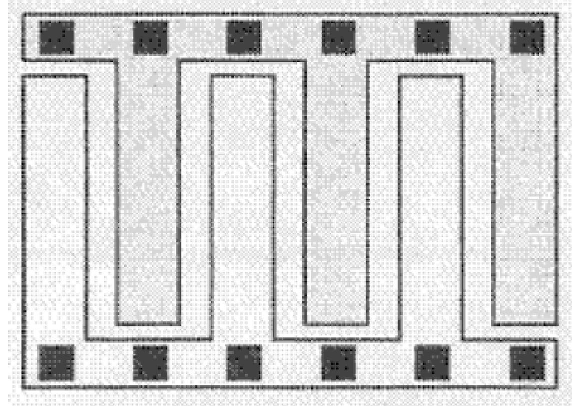
Good matching is possible with low parasitics.

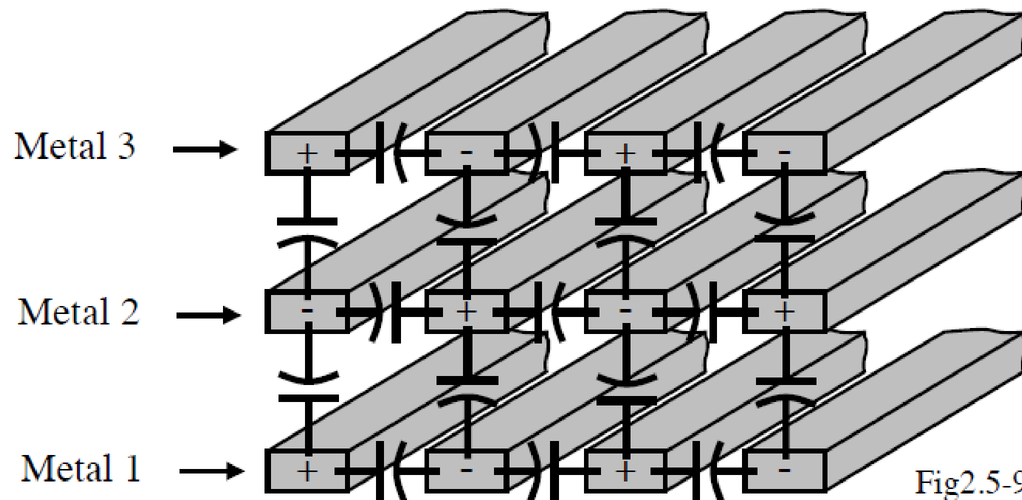
Fringe Capacitors

Capacitance between conductors on the same level and use lateral flux.

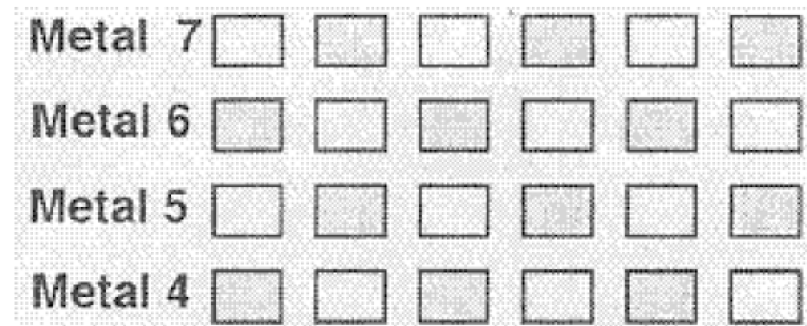


Top view:



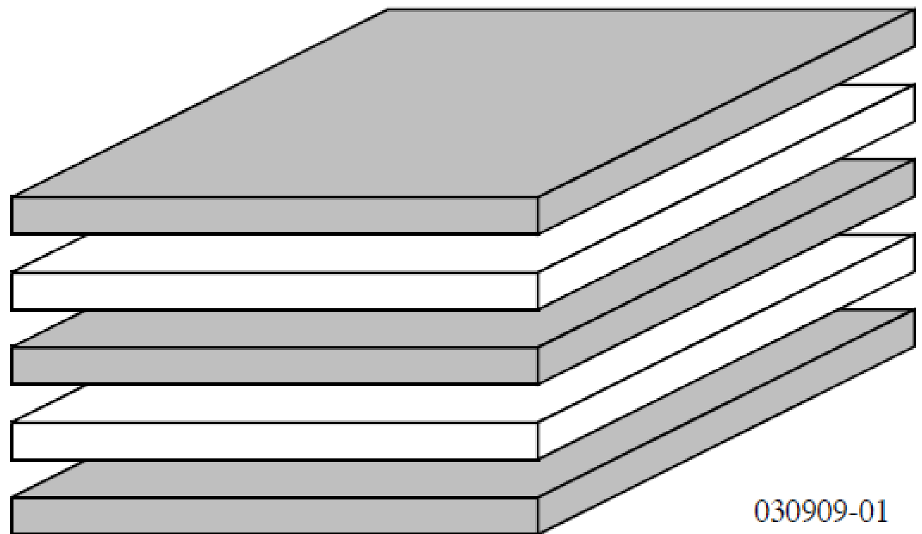


Side view:

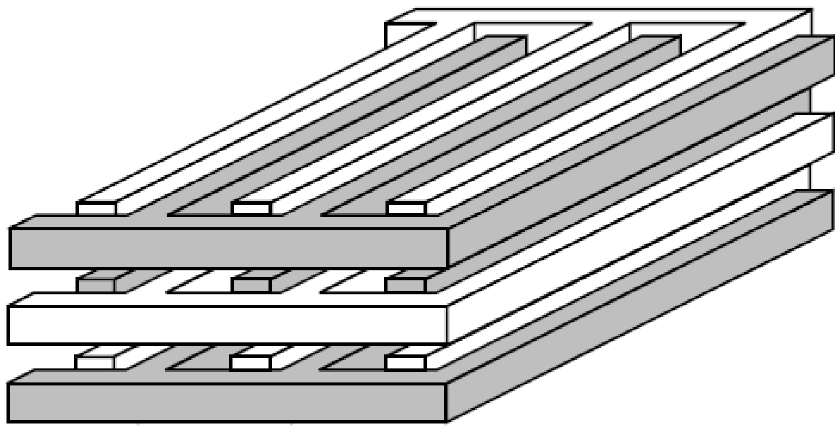


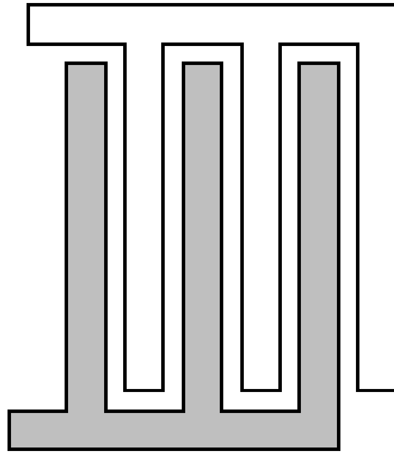
These capacitors are sometimes called fractal capacitors because the fractal patterns are structures that enclose a finite area with a near-infinite perimeter.
The capacitor/area can be increased by a factor of 10 over vertical flux capacitors.

1.) Horizontal parallel plate (HPP).



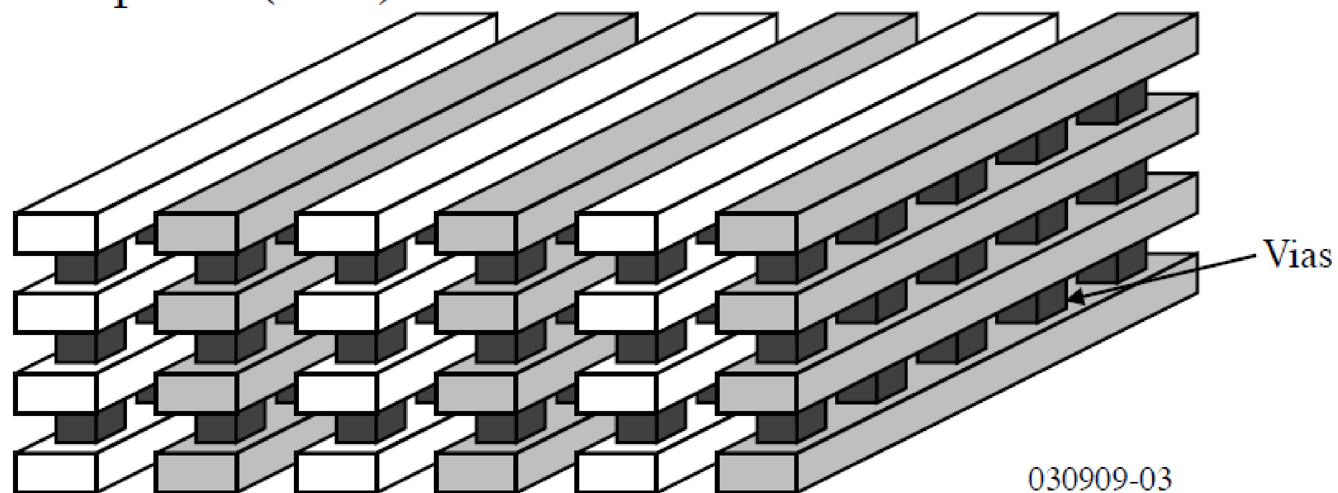
2.) Parallel wires (PW):



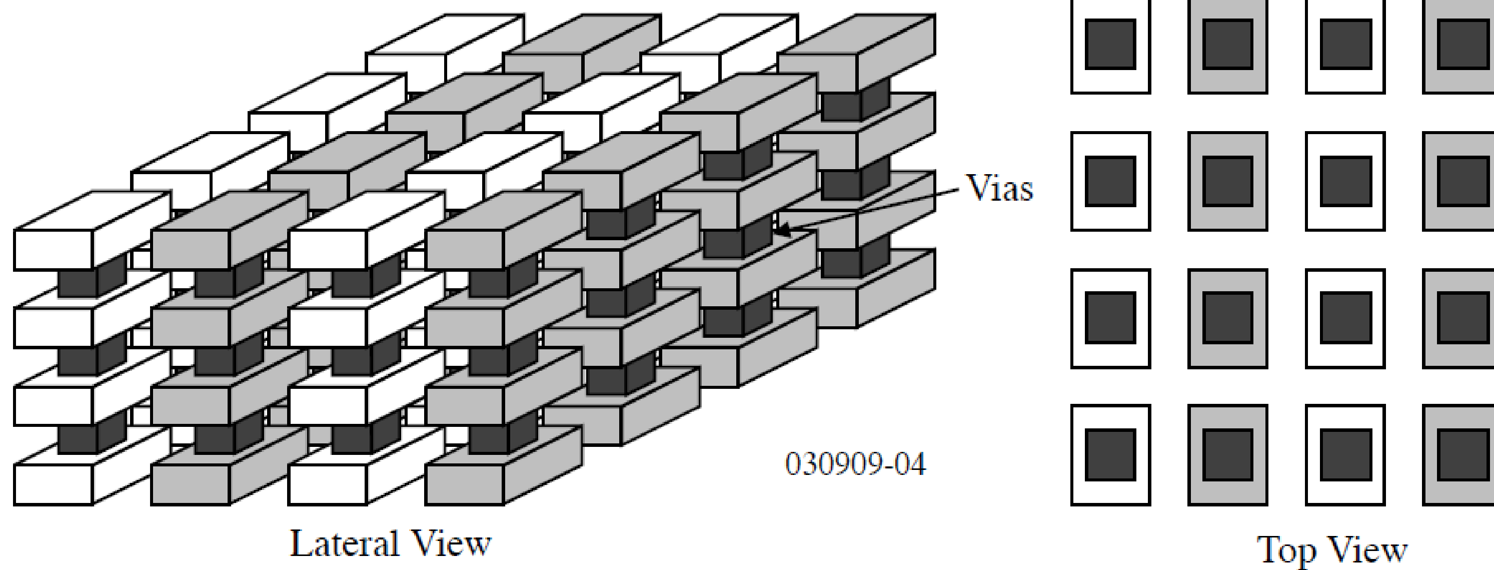


R. Aparicio and A. Hajimiri, "Capacity Limits and Matching Properties of Integrated Capacitors," *IEEE J. of Solid-State Circuits, vol. 37, no. 3, March* 2002, pp. 384-393.

3.) Vertical parallel plates (VPP):



4.) Vertical bars (VB):



Comparison

Experimental results for a CMOS process with 3 layers of metal, L_{min} =0.5μm, t_{ox} = 0.95μm and t_{metal} = 0.63μm for the bottom 2 layers of metal.

Structure	Cap. Density ($aF/\mu m^2$)	$C_{aver.}$ (pF)	Std. Dev. (fF)	$\frac{\sigma}{C_{aver.}}$	$f_{res.}$ (GHz)	Q @ 1 GHz	R_s (Ω)	Break-down (V)
VPP	158.3	18.99	103	0.0054	3.65	14.5	0.57	355
PW	101.5	33.5	315	0.0094	1.1	8.6	0.55	380
HPP	35.8	6.94	427	0.0615	6.0	21	1.1	690

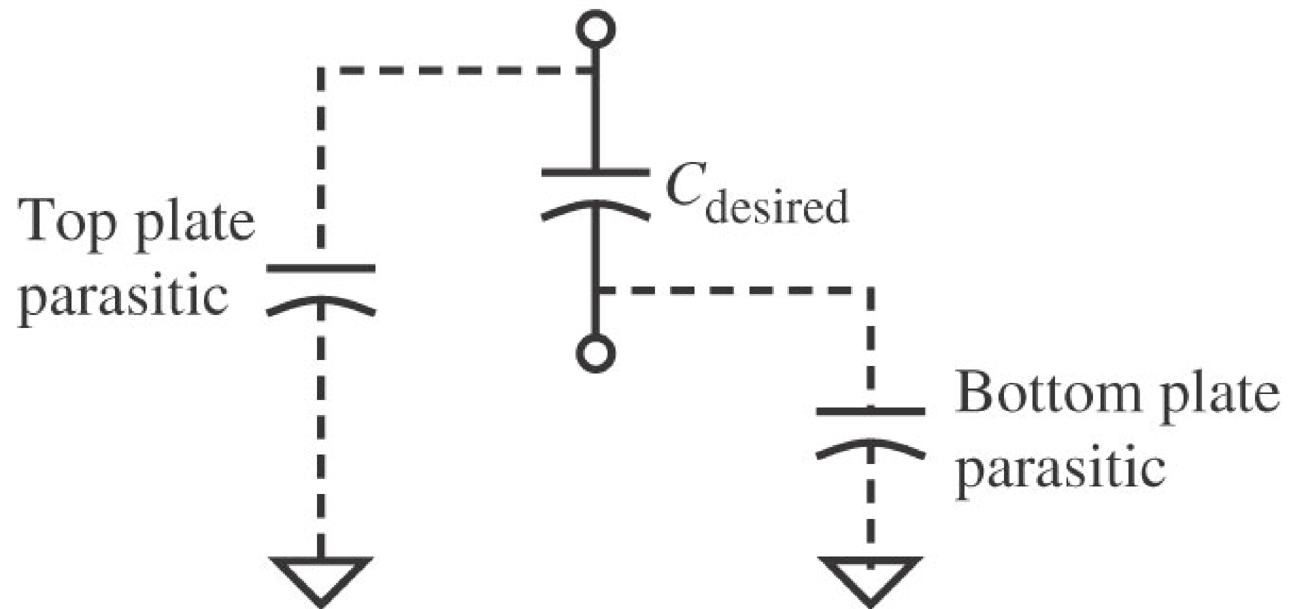
Experimental results for a digital CMOS process with 7 layers of metal, L_{min} =0.24μm, t_{ox} = 0.7μm and t_{metal} = 0.53μm for the bottom 5 layers of metal. All capacitors = 1pF.

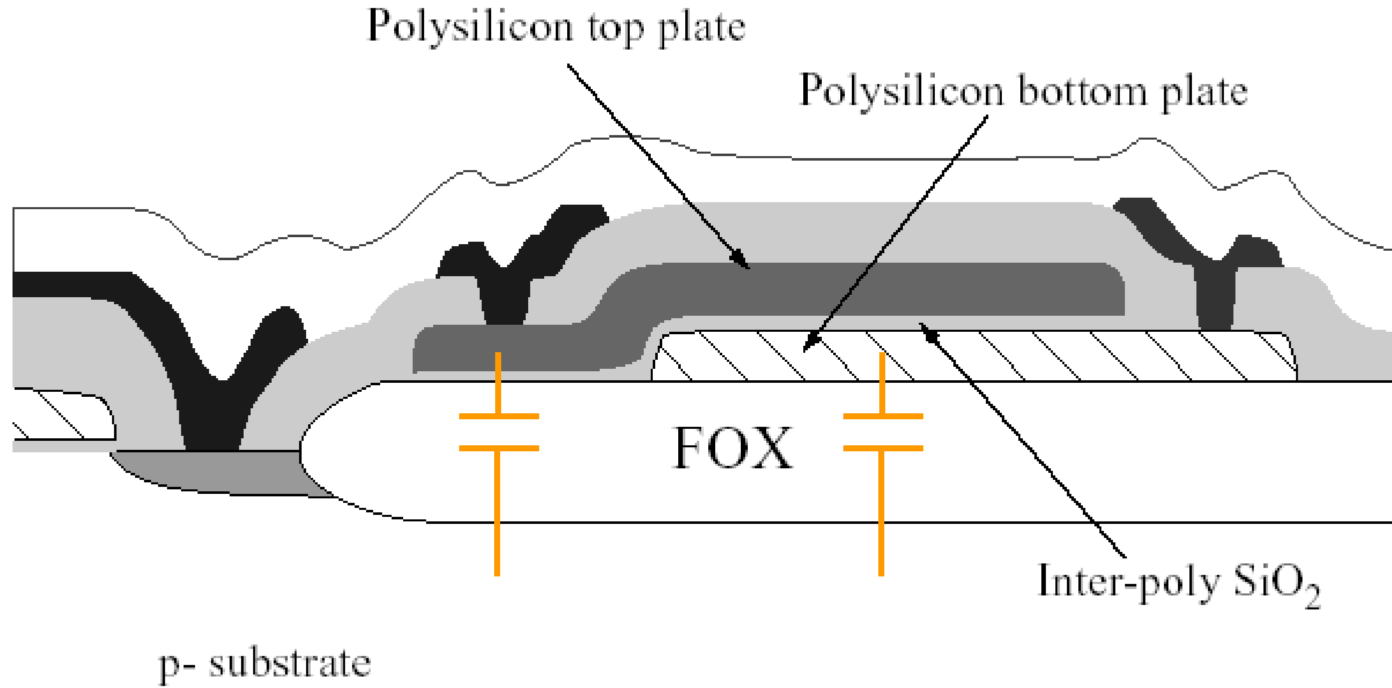
Structure (1 pF)	Cap. Density ($aF/\mu m^2$)	$C_{aver.}$ (pF)	Area (μm^2)	Cap. Enhancement	Std. Dev. (fF)	$\frac{\sigma}{C_{aver.}}$	$f_{res.}$ (GHz)	Q @ 1 GHz	Break-down (V)
VPP	1512.2	1.01	670	7.4	5.06	0.0050	> 40	83.2	128
VB	1281.3	1.07	839.7	6.3	14.19	0.0132	37.1	48.7	124
HPP	203.6	1.09	5378	1.0	26.11	0.0239	21	63.8	500
MIM	1100	1.05	960.9	5.4	-	-	11	95	-

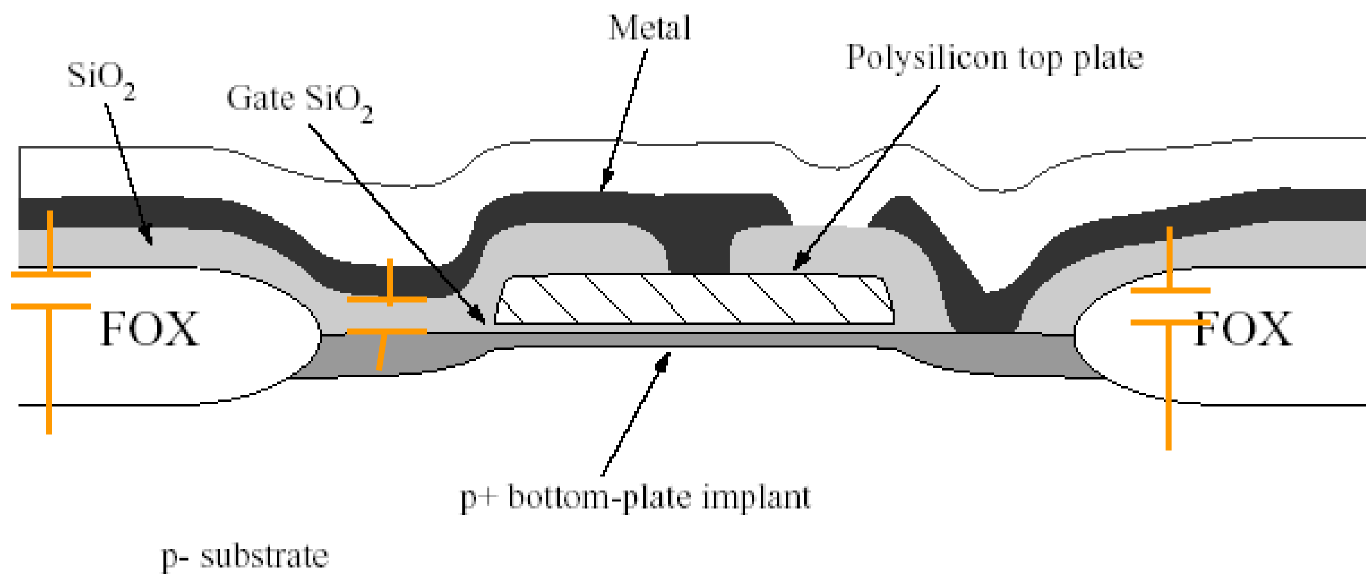
Non-ideal Behavior

- Dielectric gradients
- Edge effects
- Process biases
- Parasitics
- Voltage dependence
- Temperature dependence

Parasitic Capacitors

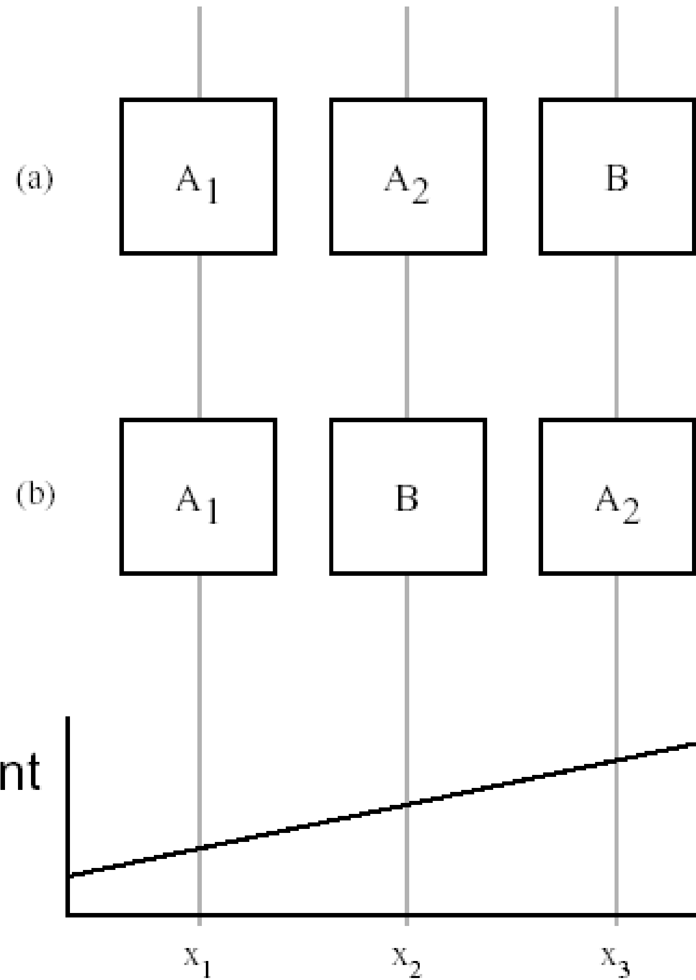



Polysilicon top plate
Polysilicon bottom plate
FOX
Inter-poly SiO_2
p- substrate

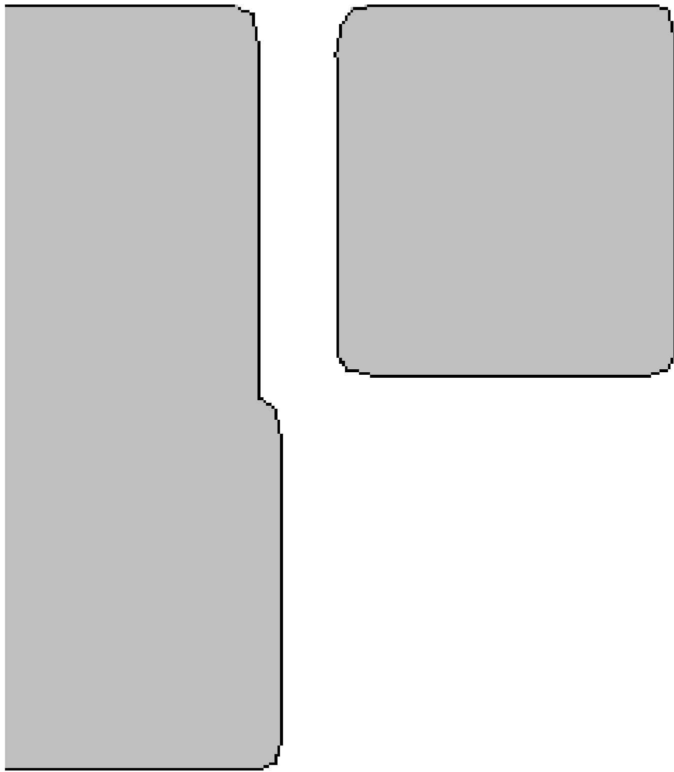

Metal
Polysilicon top plate
SiO_2
Gate SiO_2
FOX
FOX
p+ bottom-plate implant
p- substrate

Proper layout of capacitors

For achieving $C_A = 2C_B$, which one is better?

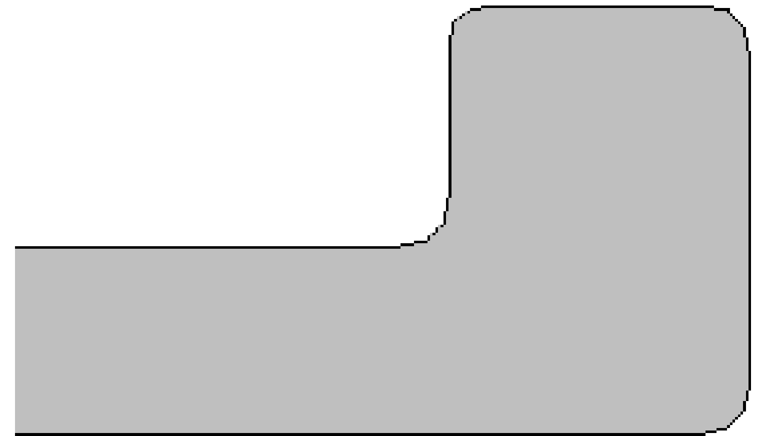


Various Capacitor Errors

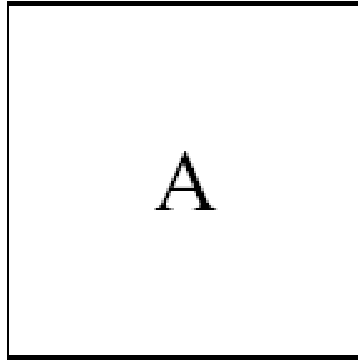


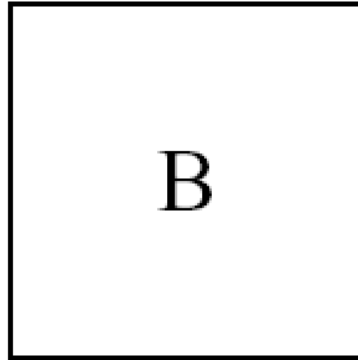
Large-scale distortion

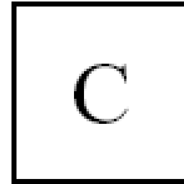
Random edge distortion



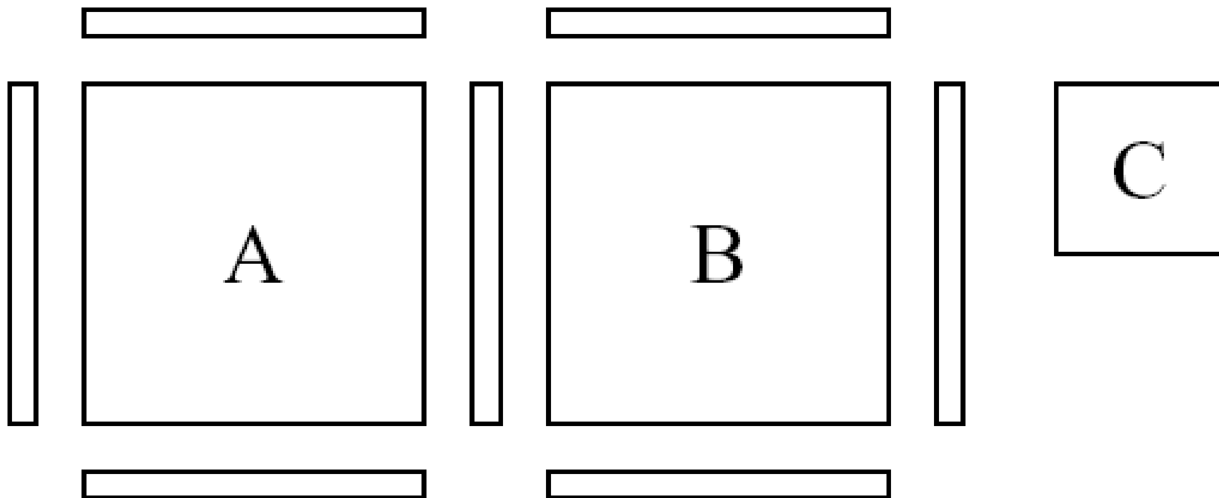
Corner-rounding distortion







Are A and B the same?



Temperature and Voltage Dependence

- MOSFET Gate Capacitors:
  - Absolute accuracy ≈ ±10%
  - Relative accuracy ≈ ±0.2%
  - Temperature coefficient ≈ +25 ppm/C°
  - Voltage coefficient ≈ -50ppm/V
- Polysilicon-Oxide-Polysilicon Capacitors:
  - Absolute accuracy ≈ ±10%
  - Relative accuracy ≈ ±0.2%
  - Temperature coefficient ≈ +25 ppm/C°
  - Voltage coefficient ≈ -20ppm/V
- Metal-Dielectric-Metal Capacitors:
  - Absolute accuracy ≈ ±10%
  - Relative accuracy ≈ ±0.6%
  - Temperature coefficient ≈ +40 ppm/C°
  - Voltage coefficient ≈ -20ppm/V, 5ppm/V2
- Accuracies depend upon the size of the capacitors.

Improving Cap Matching

- Divide each cap into even # of unit caps
- Each unit cap is square, has identical construction, has identical vicinity, has identical routing
- The unit caps for matching critical caps are laid out with inter-digitation, common centroid, or other advanced techniques.

- Same comments apply to resistors and transistors

Resistors in CMOS

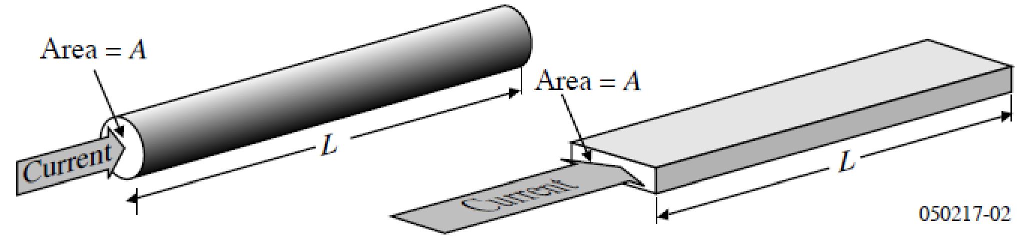
- Diffusion resistor
- polysilicon resistor
- well resistor
- metal layer resistor
- contact resistor

Resistor specs

1.) Value

$$R = \frac{\rho L}{A}$$

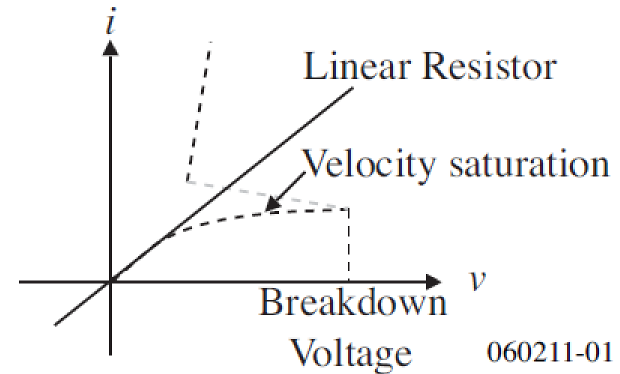
AC and DC resistance



2.) Linearity

Does $V = IR$?

Velocity saturation of carriers

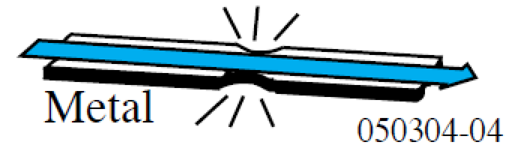


3.) Power

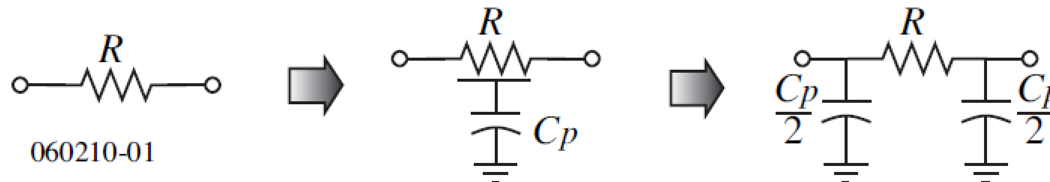
$$P = VI = I^2R$$

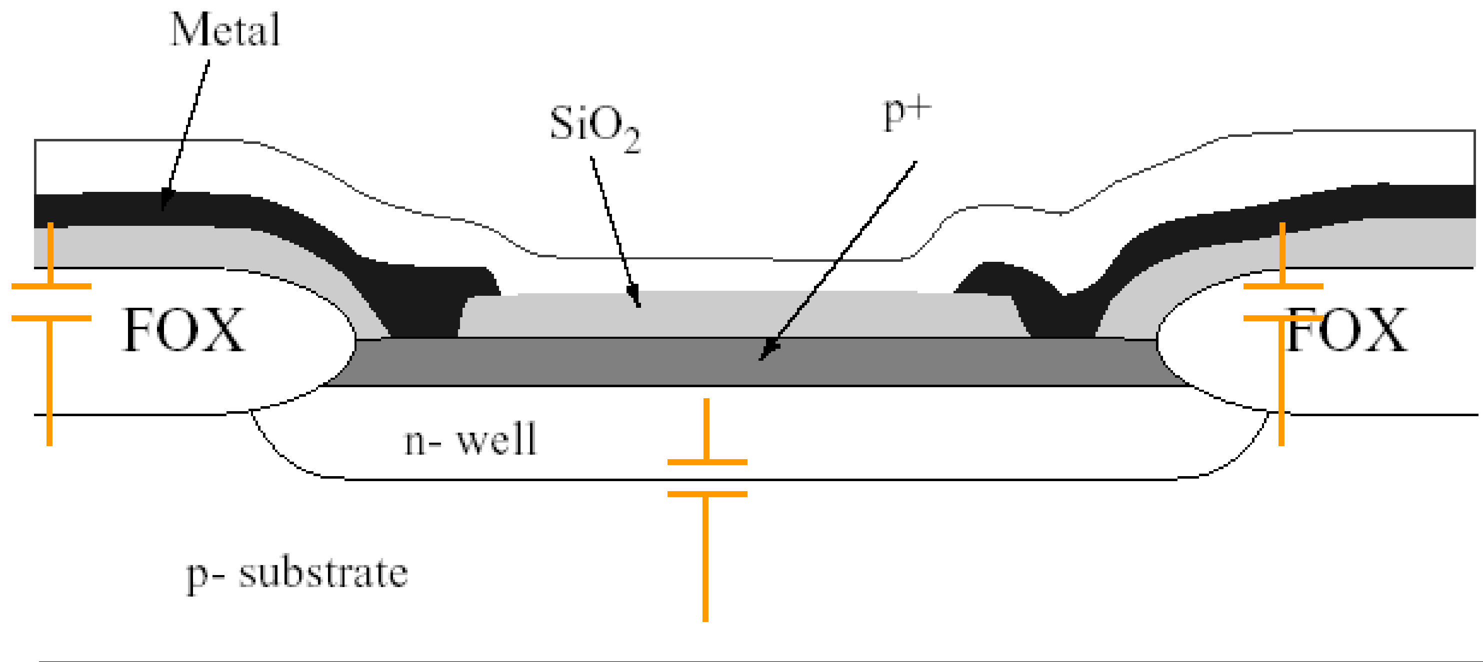
4.) Current

Electromigration



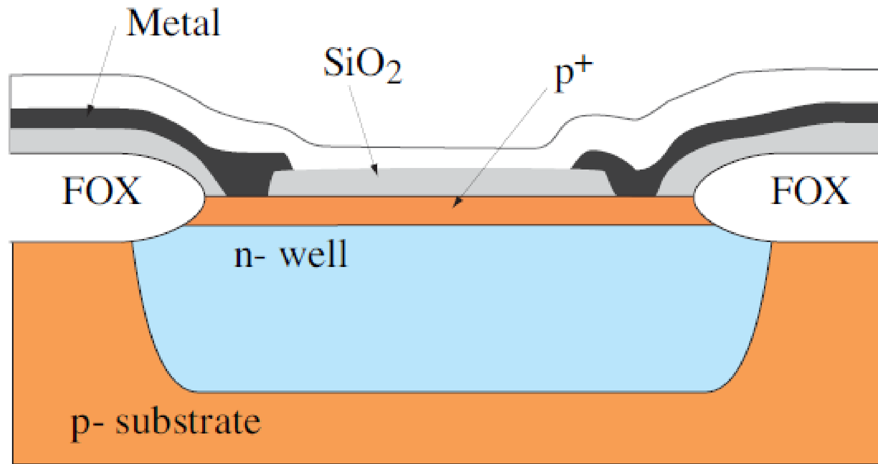
5.) Parasitics



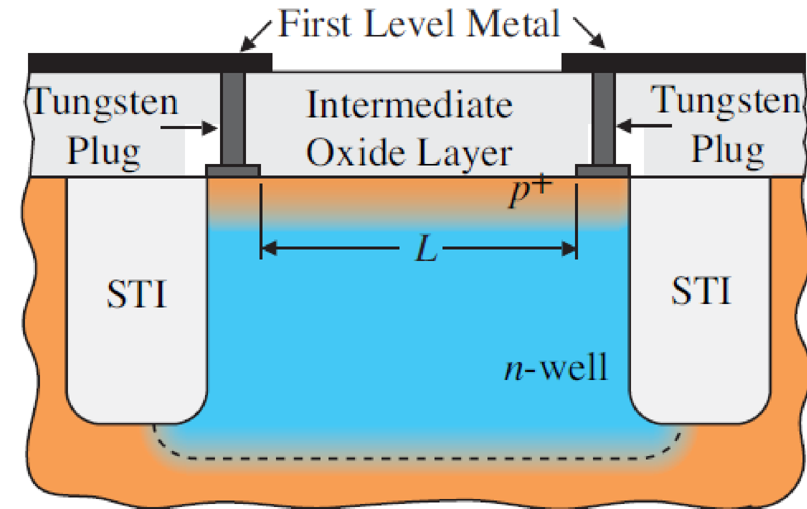


Diffusion resistor in n-well

Source/Drain Resistor



Older LOCOS Technology



Diffusion:

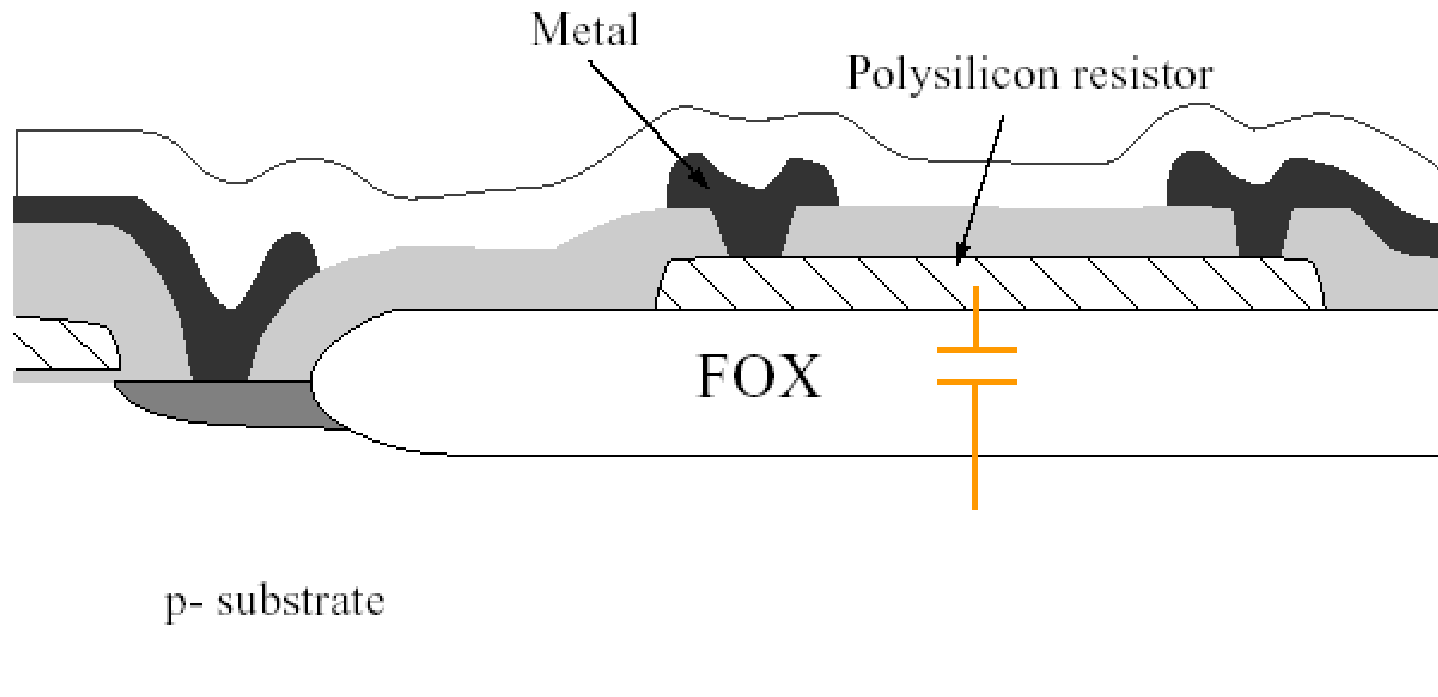
10-100 ohms/square
Absolute accuracy = ±35%
Relative accuracy=2% (5μm), 0.2% (50μm)
Temperature coefficient = +1500 ppm/°C
Voltage coefficient ≈ 200 ppm/V

Ion Implanted:

500-2000 ohms/square
Absolute accuracy = ±15%
Relative accuracy=2% (5μm), 0.15% (50μm)
Temperature coefficient = +400 ppm/°C
Voltage coefficient ≈ 800 ppm/V

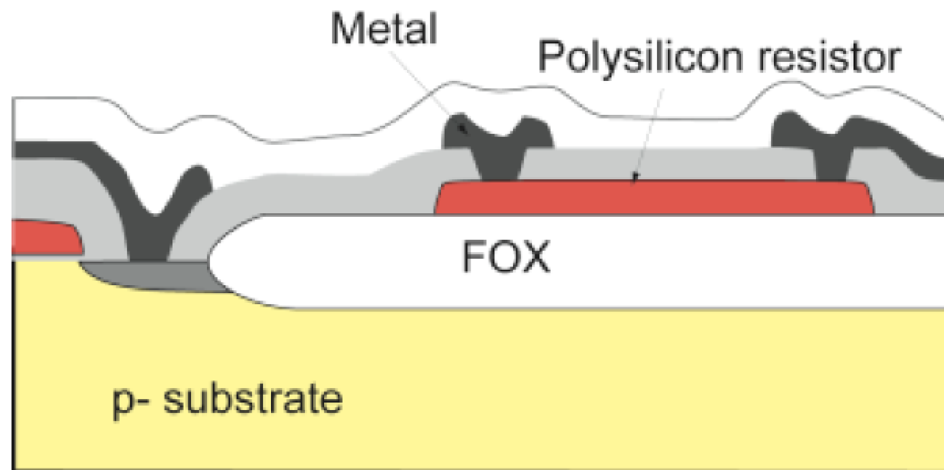
Comments:

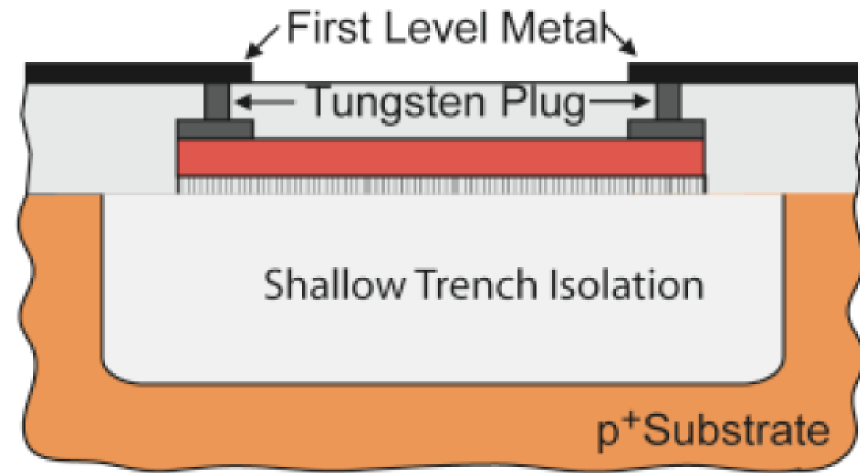
- Parasitic capacitance to substrate is voltage dependent.
- Piezoresistance effects occur due to chip strain from mounting.



Polysilicon resistor on FOX

Polysilicon Resistor





30-100 ohms/square (unshielded)
100-500 ohms/square (shielded)
Absolute accuracy = ±3 0%
Relative accuracy = 2% (5 μm)
Temperature coefficient = 500-1000 ppm/°C
Voltage coefficient ≈ 100 ppm/V

Comments:

- Used for fuzzes and laser trimming
- Good general resistor with low parasitics

Metal

n+

FOX

FOX

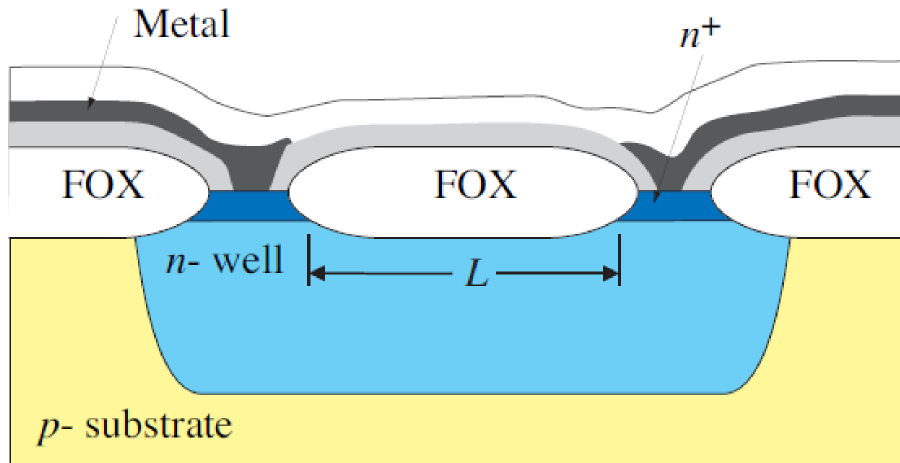
FOX

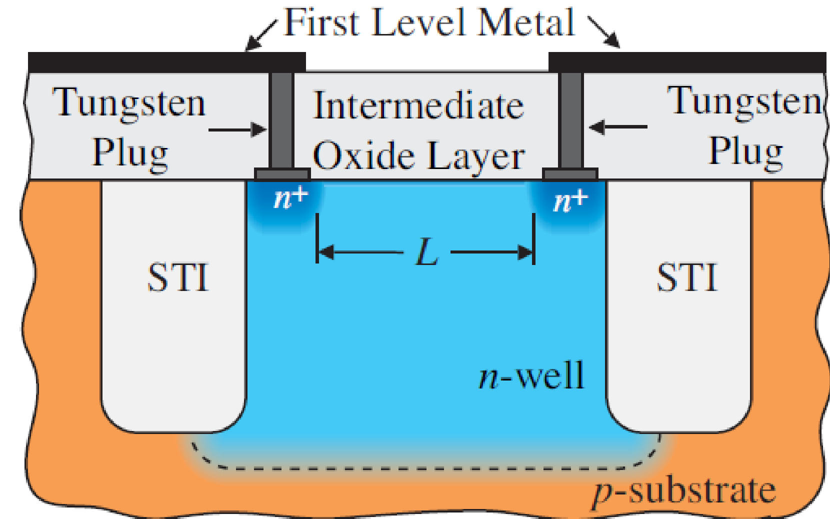
n- well

p- substrate

n-well resistor on p-substrate

N-well Resistor





1000-5000 ohms/square

Absolute accuracy = ±40%

Relative accuracy ≈ 5%

Temperature coefficient = 4000 ppm/°C

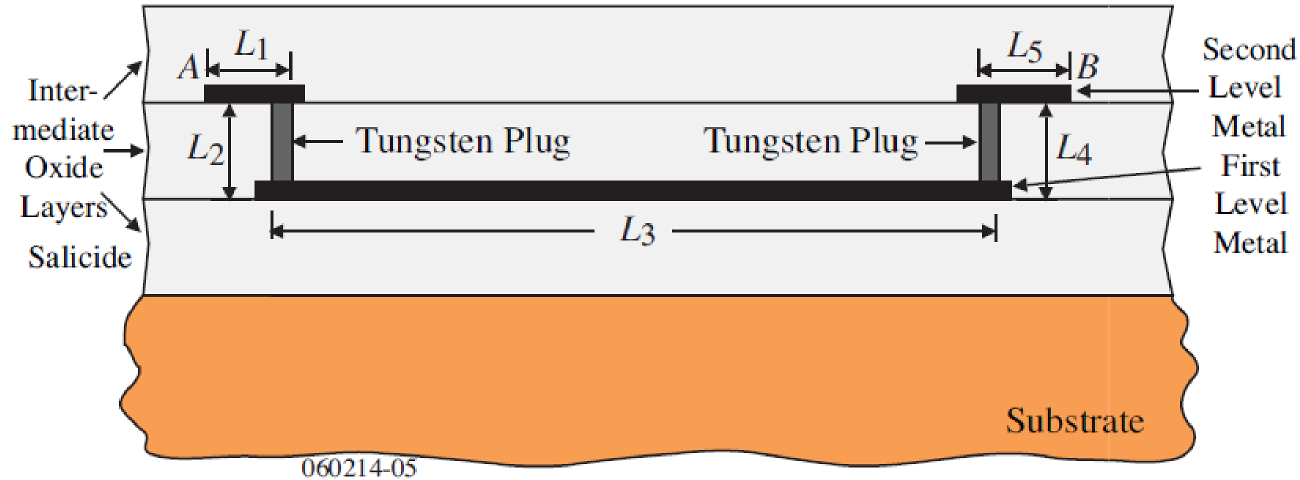
Voltage coefficient is large ≈ 8000 ppm/V

Comments:

- Good when large values of resistance are needed.
- Parasitics are large and resistance is voltage dependent
- Could put a p^+ diffusion into the well to form a pinched resistor

Metal Resistor

Illustration:



Resistance from A to B = Resistance of segments L_1, L_2, L_3, L_4, and L_5 with some correction subtracted because of corners.

Sheet resistance:

50-70 m$\Omega/\square$ ± 30% for lower or middle levels of metal

30-40 m$\Omega/\square$ ± 15% for top level metal

Watch out for the current limit for metal resistors.

Contact resistance varies from 5Ω to 10Ω.

Tempco ≈ +4000 ppm/°C

Need to derate the current at higher temperatures:

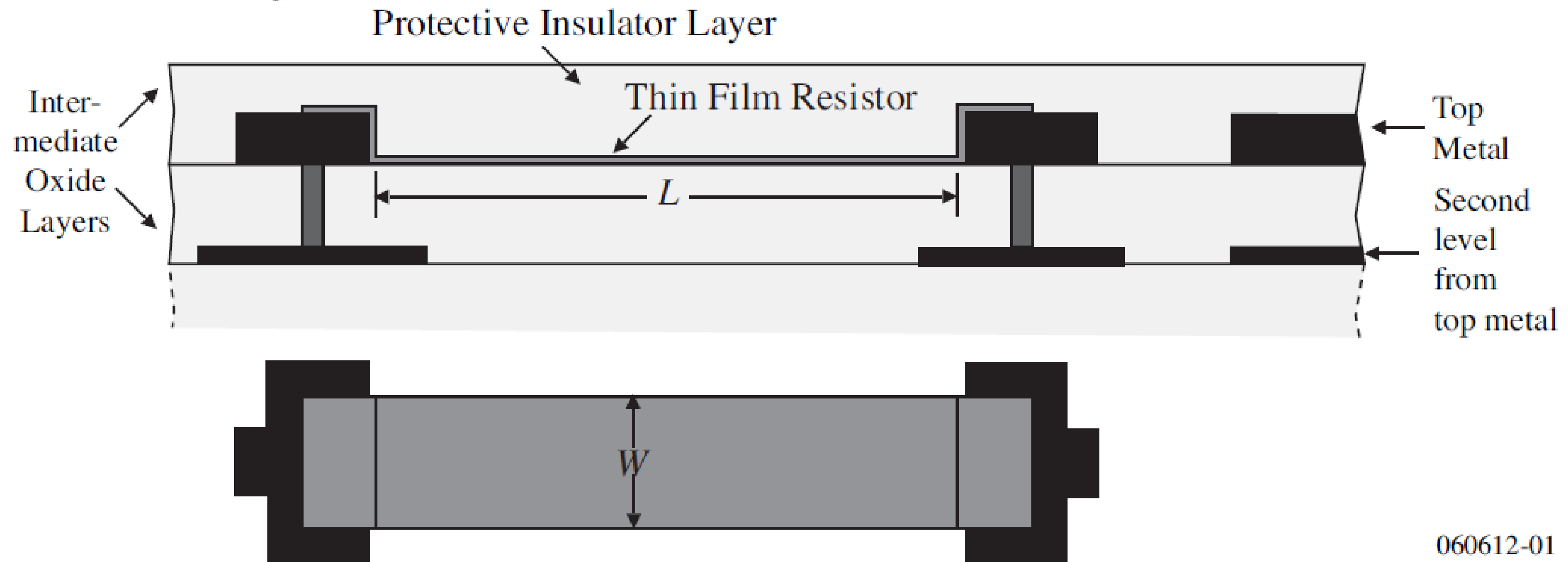
$$I_{DC}(T_j) = D_t \cdot I_{DC}(T_r)$$

T_j(°C)	T_r(°C)	D_t
<85	85	1
100	85	0.63
110	85	0.48
125	85	0.32
150	85	0.18

Thin Film Resistors

A high-quality resistor fabricated from a thin nickel-chromium alloy or a silicon-chromium mixture.

Uppermost metal layer:



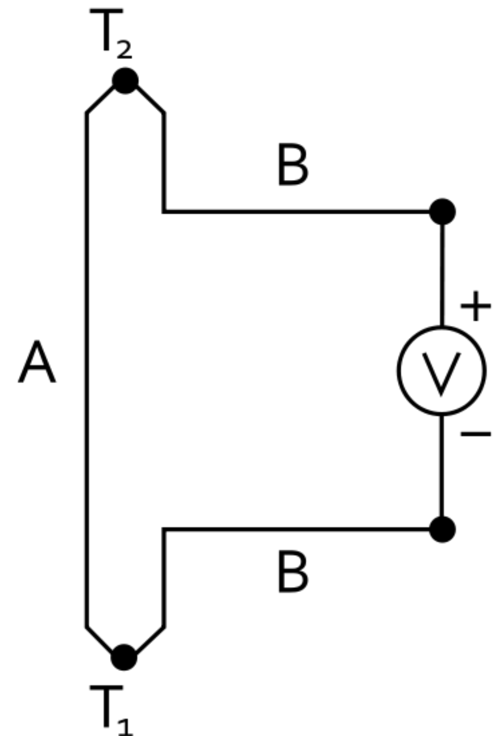
Performance:

- Sheet resistivity is approximately 5-10 ohms/square
- Temperature coefficients of less than 100 ppm/°C
- Absolute tolerance of better than ±0.1% using laser trimming
- Selectivity of the metal etch must be sufficient to ensure the integrity of the thin-film resistor beneath the areas where metal is etched away.

Thermoelectric (Seebeck) Effects

- When two materials form a junction, a voltage difference is generated, which depends on the temperature
- But a single junction voltage cannot be measured
- It needs at least two junctions
- The voltage difference is:

$$\begin{aligned} \boldsymbol{V} &= (\boldsymbol{S_B} - \boldsymbol{S_A})\boldsymbol{T_2} - (\boldsymbol{S_B} - \boldsymbol{S_A})\boldsymbol{T_1} \\ &= (\boldsymbol{S_B} - \boldsymbol{S_A})(\boldsymbol{T_2} - \boldsymbol{T_1}) \end{aligned}$$



Seebeck Coefficients

- S_A and S_B are called Seebeck coefficients of material A and material B
- Roughly speaking S is inversely related to the conductivity of the material
- Metals have low S, semiconductors have high S
- High resistivity materials (with light doping) pose serious thermoelectric problems

Table 1. Seebeck Coefficients for Some Metals and Alloys, Compared to Platinum

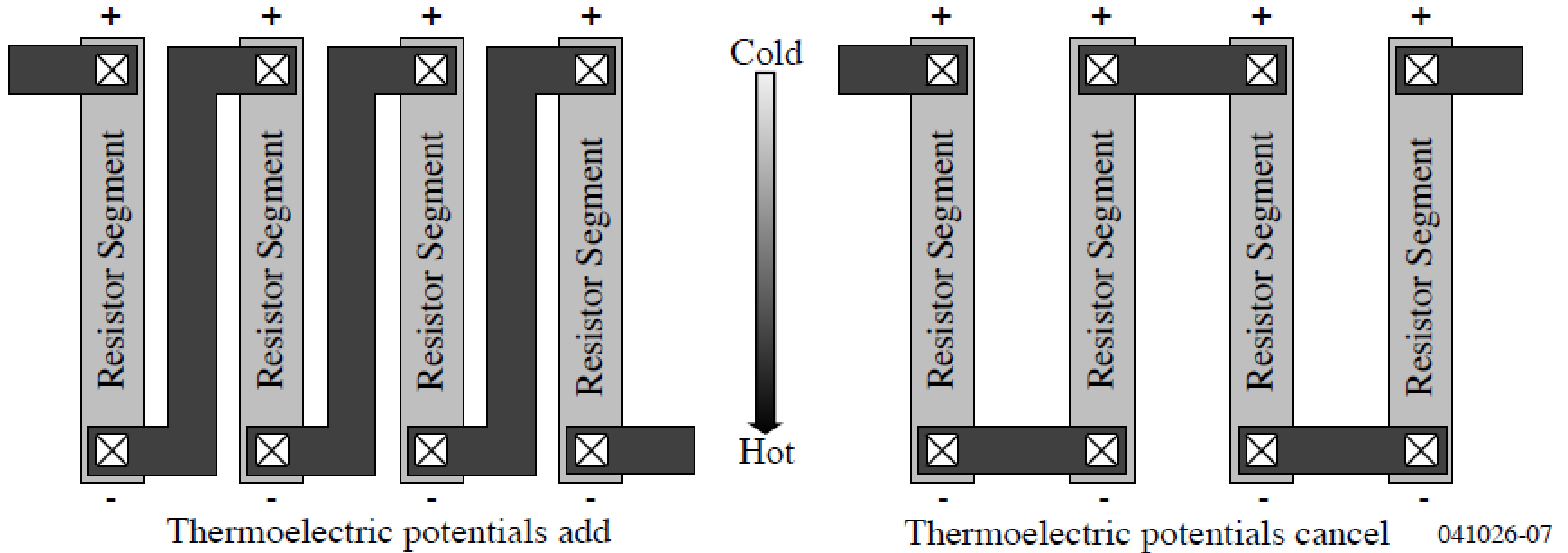
Metals	Seebeck Coefficient
	μV/K
Antimony	47
Nichrome	25
Molybdenum	10
Cadmium	7.5
Tungsten	7.5
Gold	6.5
Silver	6.5
Copper	6.5
Rhodium	6.0
Tantalum	4.5
Lead	4.0
Aluminum	3.5
Carbon	3.0
Mercury	0.6
Platinum	0
Sodium	-2.0
Potassium	-9.0
Nickel	-15
Constantan	-35
Bismuth	-72

Table 2. Seebeck Coefficients for Some Semiconductors

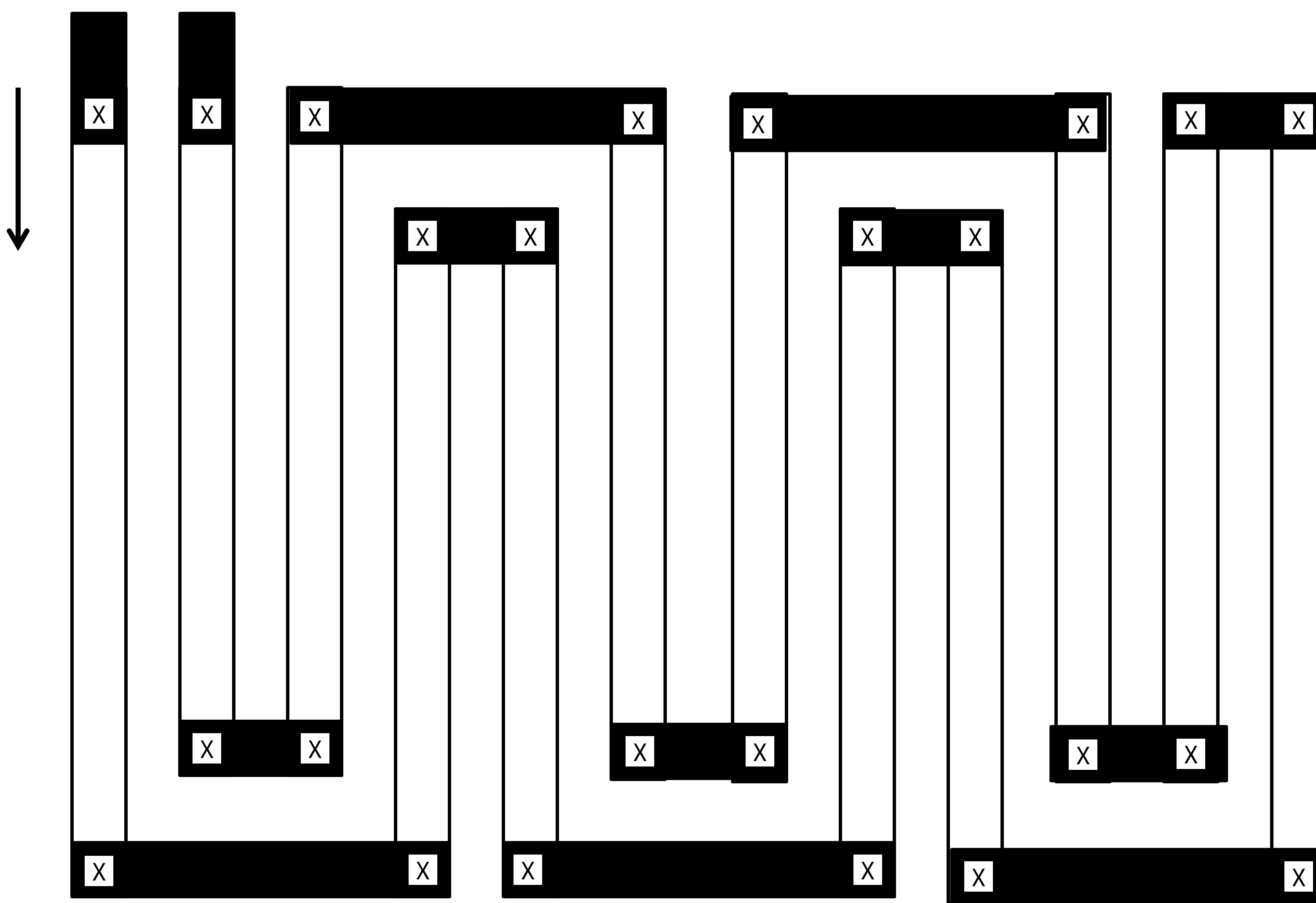
Semiconductors	Seebeck Coefficient
	μV/K
Se	900
Te	500
Si	440
Ge	300
n-type Bi_2Te_3	-230
p-type $Bi_{2-x}Sb_xTe_3$	300
p-type Sb_2Te_3	185
PbTe	-180
$Pb_{03}Ge_{39}Se_{58}$	1670
$Pb_{06}Ge_{36}Se_{58}$	1410
$Pb_{09}Ge_{33}Se_{58}$	-1360
$Pb_{13}Ge_{29}Se_{58}$	-1710
$Pb_{15}Ge_{37}Se_{58}$	-1990
$SnSb_4Te_7$	25
$SnBi_4Te_7$	120
$SnBi_3Sb_1Te_7$	151
$SnBi_{2.5}Sb_{1.5}Te_7$	110
$SnBi_2Sb_2Te_7$	90
$PbBi_4Te_7$	-53

Moffat, R., "Notes on Using Thermocouples", ElectronicsCooling, Vol. 3, No. 1, 1997

Resistor Layout



- But what about horizontal temperature gradient?
- Use "antiparallel" layout



HW1: Prove that if following the arrow, all the metal to poly contacts have the same centroid as all the poly to metal contacts, then the thermo-electric effect due to linear thermo gradient is cancelled.

HW2: Generalize HW1 to design a layout pattern so that thermo-electric effects due to both linear and nonlinear thermo gradients are cancelled.

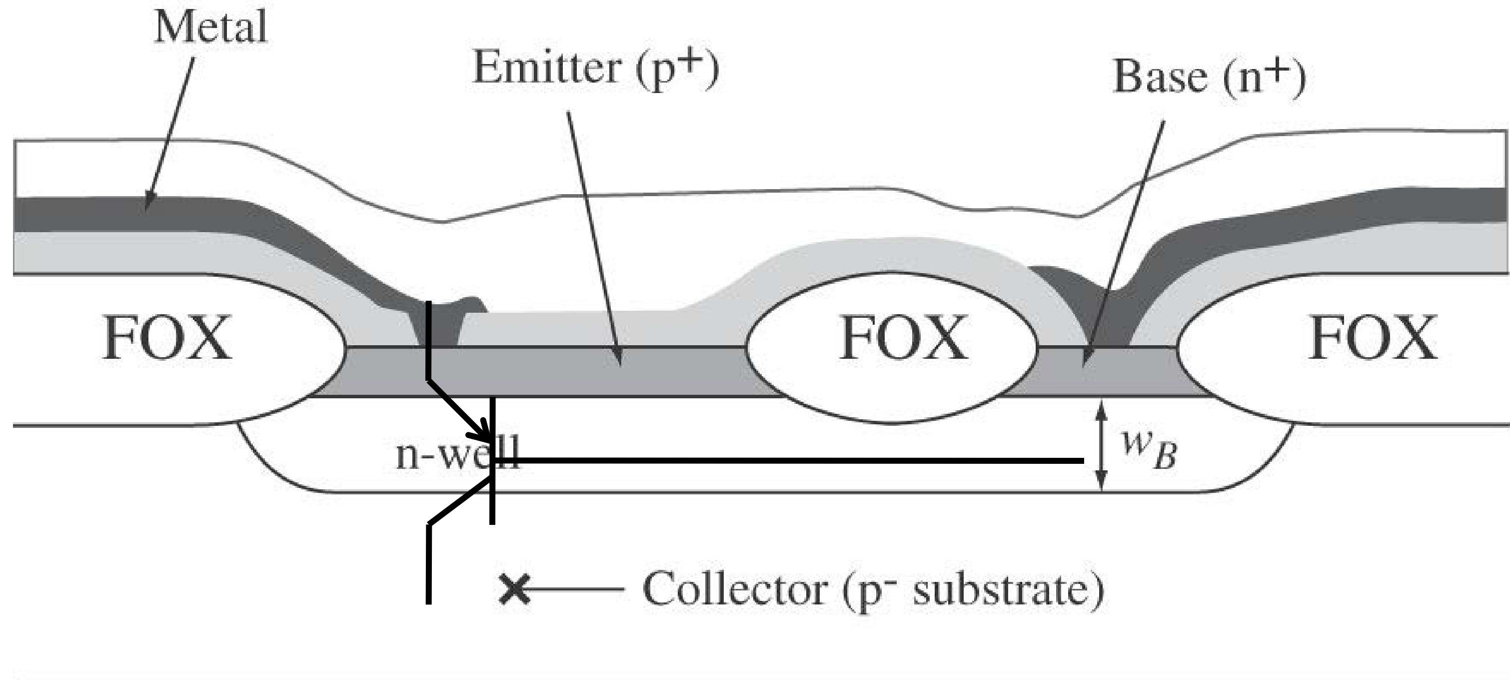
Suggestions

- Use larger area (increase both W and L) to improve accuracy
- Use metal to make "turns", i.e., use straight strips only
- Use unit resistors
- Use dummies
- Use identical structures and vivinities
- Interdigitate, common centroid, and other techniques for good matching

Passive RC Performance

Component Type	Range of Values	Absolute Accuracy	Relative Accuracy	Temperature Coefficient	Voltage Coefficient
MOSFET gate Cap.	6-7 $fF/\mu m^2$	10%	0.1%	20ppm/°C	±20ppm/V
Poly-Poly Capacitor	0.3-0.4 $fF/\mu m^2$	20%	0.1%	25ppm/°C	±50ppm/V
Metal-Metal Capacitor	0.1-1$fF/\mu m^2$	10%	0.6%	??	??
Diffused Resistor	10-100 Ω/sq.	35%	2%	1500ppm/°C	200ppm/V
Ion Implanted Resistor	0.5-2 kΩ/sq.	15%	2%	400ppm/°C	800ppm/V
Poly Resistor	30-200 Ω/sq.	30%	2%	1500ppm/°C	100ppm/V
n-well Resistor	1-10 kΩ/sq.	40%	5%	8000ppm/°C	10kppm/V
Top Metal Resistor	30 mΩ/sq.	15%	2%	4000ppm/°C	??
Lower Metal Resistor	70 mΩ/sq.	28%	3%	4000ppm/°C	??

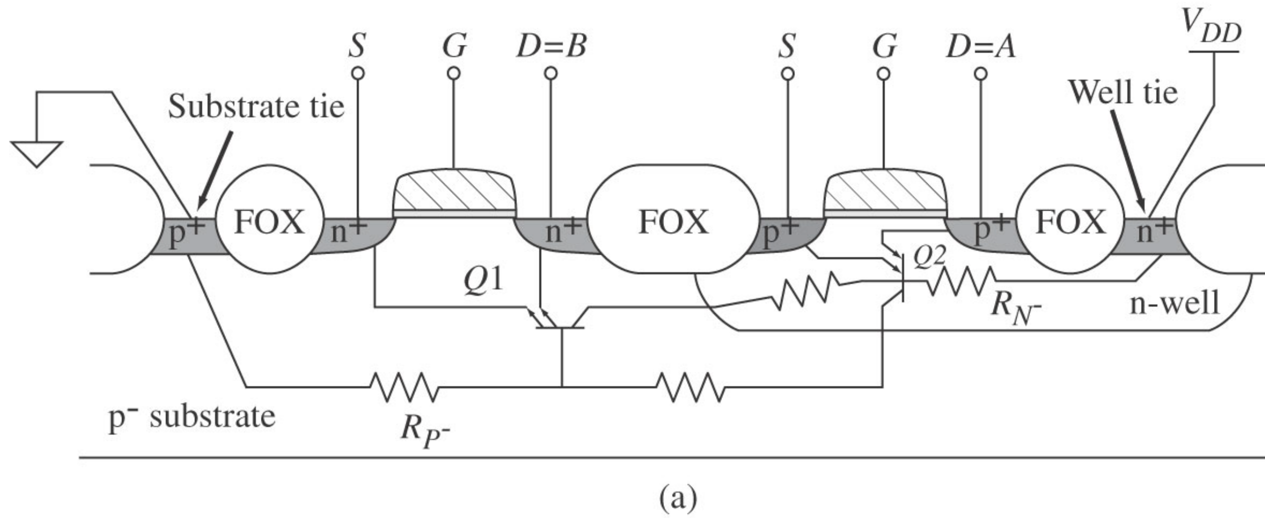
Parasitic Bipolar in CMOS



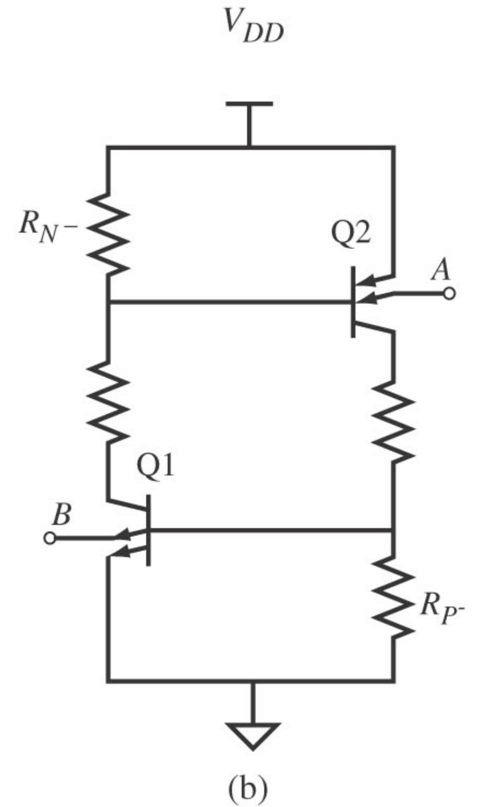
Vertical PNP

Horizontal NPN

Latch-up problem



(a)



(b)

Preventing Latch-up

p-channel transistor

n-channel transistor

n^+ guard bars

p^+ guard bars

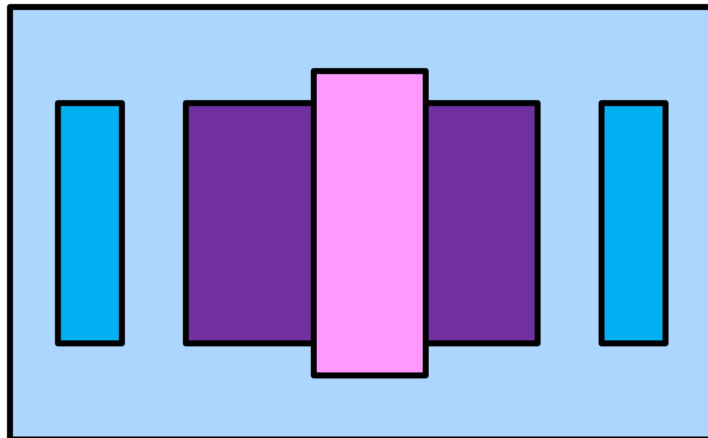
V_{DD}

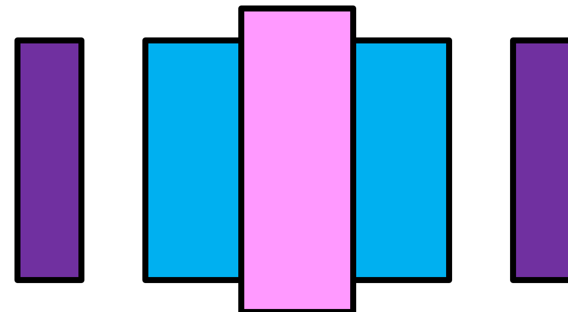
V_{SS}

FOX

n-well

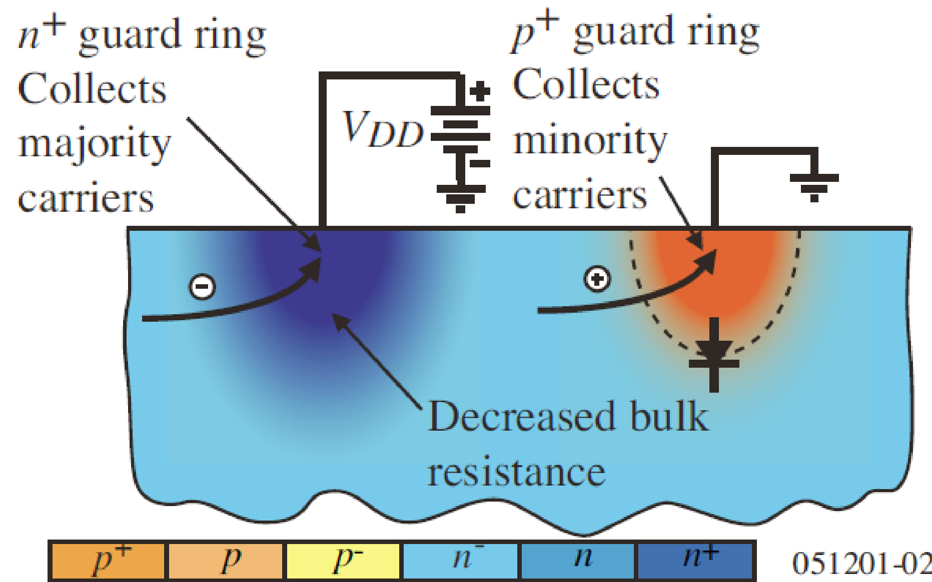
p^- substrate

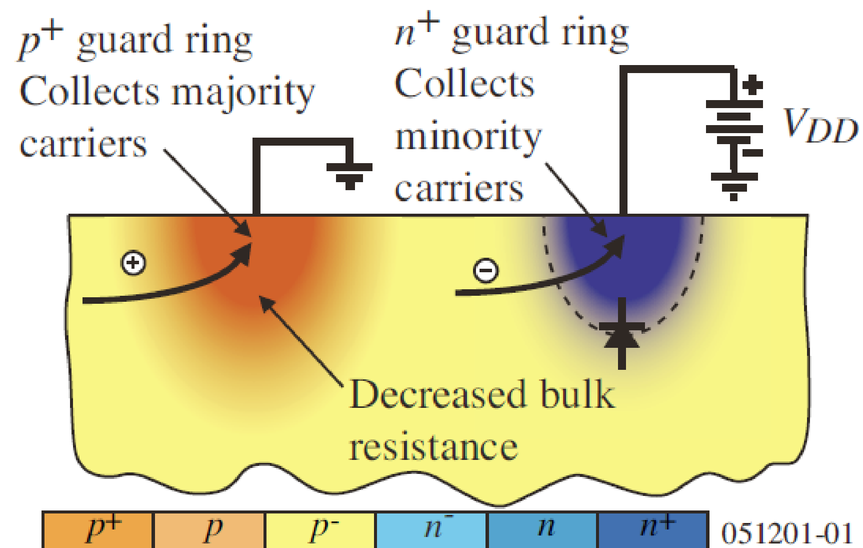




Guard Rings

- Collect carriers flowing in the silicon
- Bypass unwanted currents to VDD or VSS
- Isolate sensitive circuits from noise and/or interferences

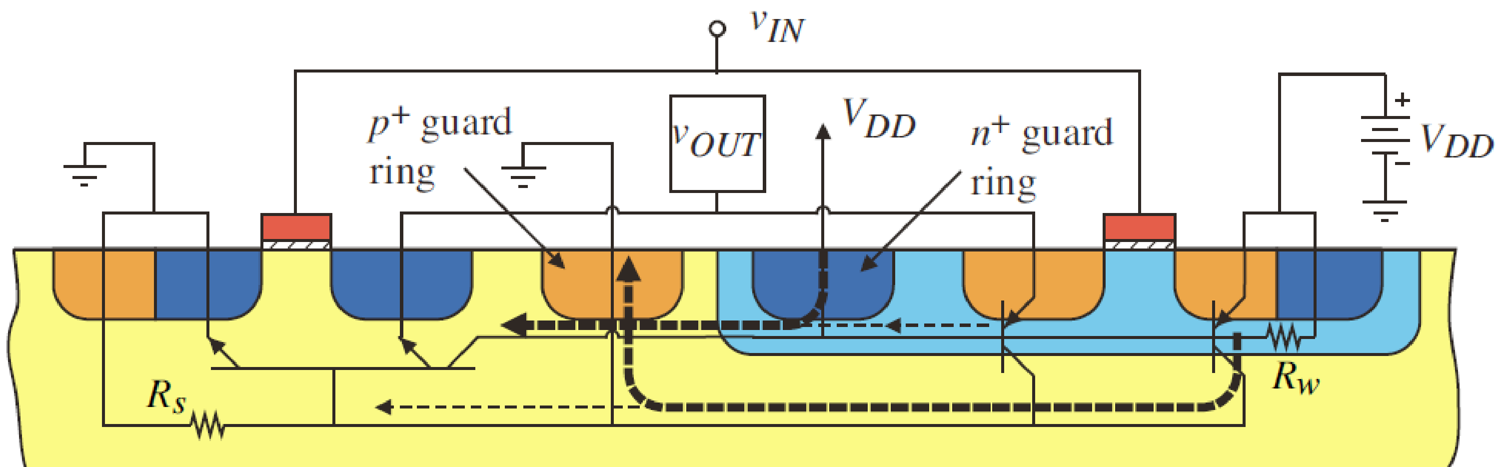




Butted Contacts and Guard Rings

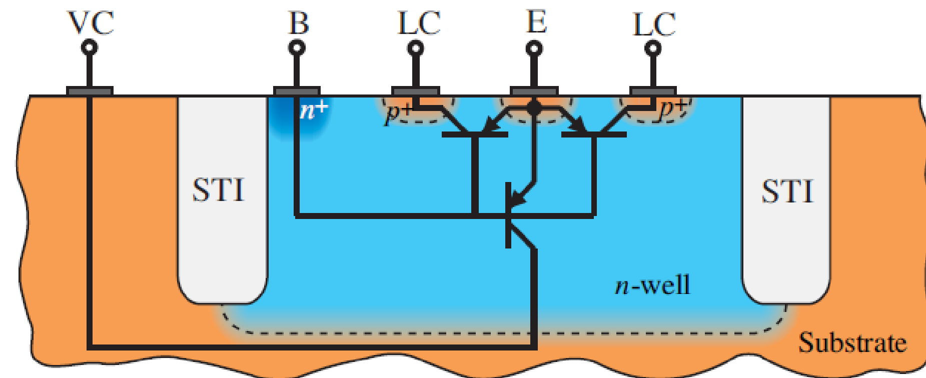
- To reduce sensitivity
- To prevent latch up

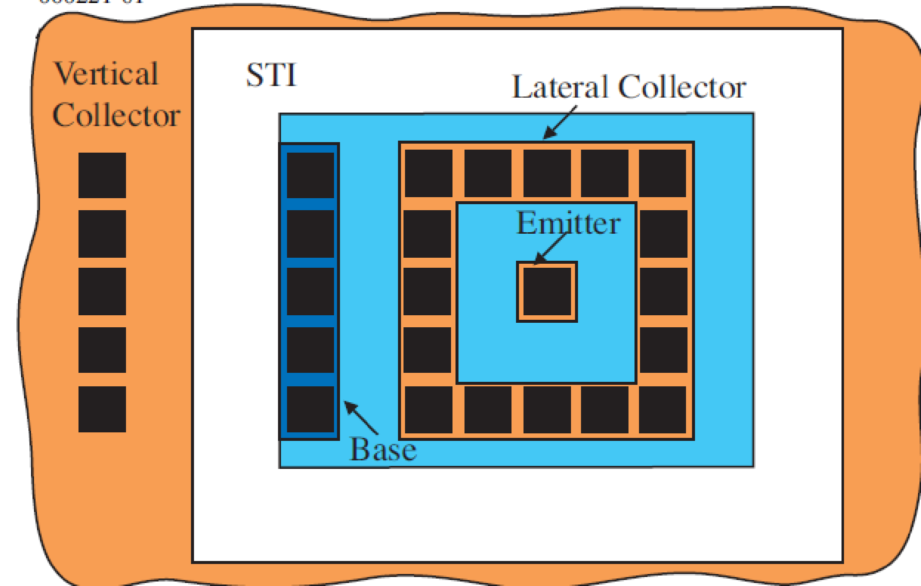
v_{IN}
p^+ guard ring
v_{OUT}
V_{DD}
n^+ guard ring
V_{DD}
R_W
R_S
Note increased separation



Intentional Bipolar

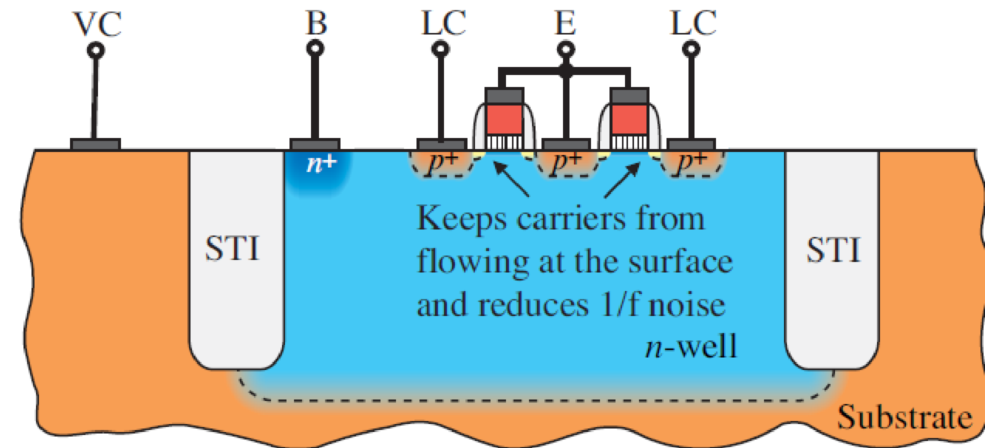
- It is desirable to have the lateral collector current much larger than the vertical collector current.
- Lateral BJT generally has good matching.
- The lateral BJT can be used as a photodetector with reasonably good efficiency.
- Triple well technology allows the current of the vertical collector to avoid the substrate.

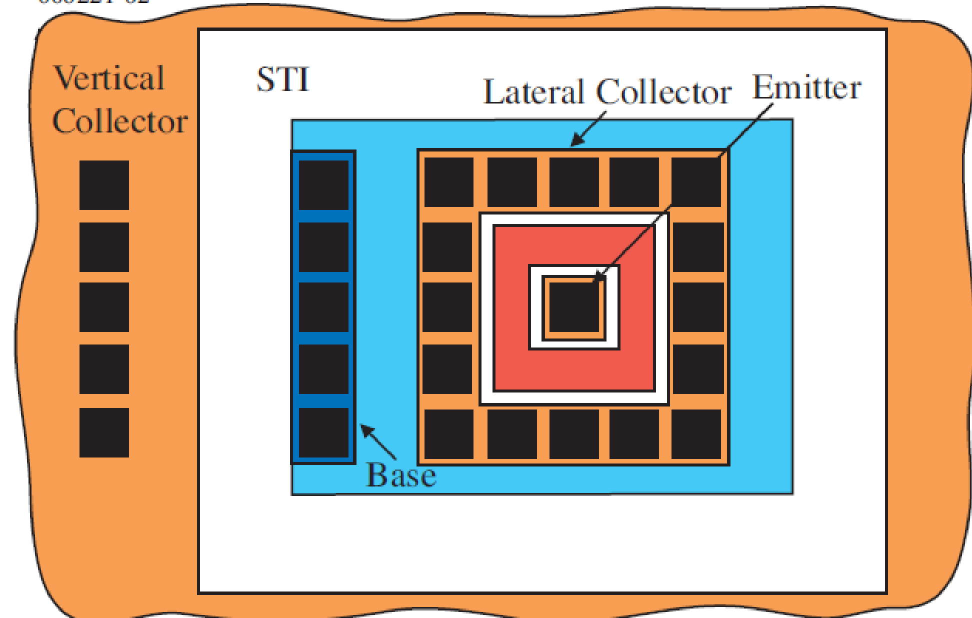




Donut PMOS as bipolar

- A Field-Aided Lateral BJT
  - Use minimum channel length
  - enhance beta to 50 to 100





- Can be done in ON0.5 or TSMC0.18
  - No STI

ESD protection

- A very serious problem
- Not enough theoretical study
- Many trade secrets
- Learn from experienced designers