EE 330 Midterm Exam #01

Name:_____Score_____

Instructions:

- The exam is for individual work, with closed-book, closed-notes, no electronic devices.
- One sheet of formulas of US letter size is allowed. No other papers allowed.
- Write brief solutions in the space provided on this exam. If necessary, you can write on the backside but clearly mark the question numbers.
- Do not erase. Just cross out unwanted writing, and write correct answers in clean space.
- Specific parameters are given in the problem statements. Extra process and device parameters are attached at the end of the exam.

- Here are some additional parameters in case you need them: $\mu_n C_{OX}=300\mu A/V^2$, $\mu_p C_{OX}=100\mu A/V^2$, $V_{TNO}=0.5V$, $V_{TPO}= -0.5V$, $C_{OX}=8fF/\mu^2$, no Vds effect ($\lambda=0$), diode $J_S=10^{-17}A/\mu^2$, k/q= 8.61E-5 V/K, kT/q=26mV.
- If you need any other parameters, clearly make an assumption and proceed.

1. Use two words (phrases) to briefly answer the following questions: (2 pts each)
    a. Name the largest chip fabrication foundry in the world, and give the main reason why we focus on it.

    b. Name the largest two semiconductor companies in the world.

    c. Name one famous CEO who graduated from ISU and the corresponding large semiconductor company.

    d. State why a barrier metal layer is used when creating copper interconnects, and reason why copper is better than aluminum.

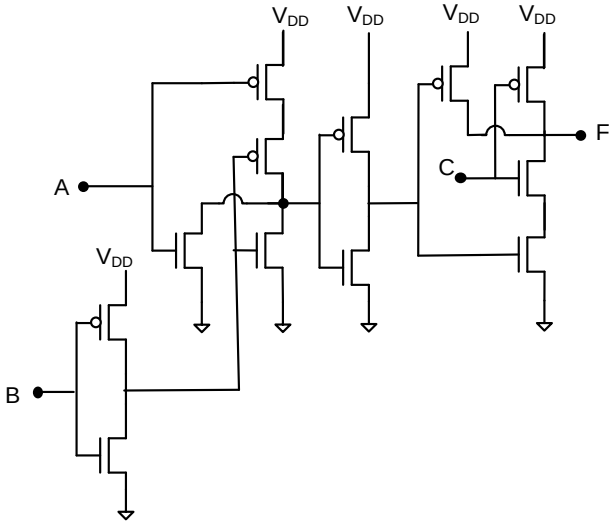
    e. Name two drawbacks of Pass Transistor Logic.

2. Circle the best choice or draw the best matches. (3 pts each)
    a. On a given wafer, as the die area increase, match parameter and the trend:
        - Die area cost — a) constant as area increase
        - Defect density — b) increase linearly as area increase
        - Yield of good die — c) increase exponentially
        - Cost of good die — d) decrease exponentially
    b. Circle the most important goal when designing a chip product:
        - Smaller die area
        - Higher yield
        - Better performance
        - Selling more chips
        - Other:_____
    c. A chip has 5 components, each has 10% chance being bad. The chance the whole chip is bad is close to: a) 10%, b) 40%, c) 50%, d) 60%, e)90%
    d. Match each process step with how they add or subtract materials:
        - Photolithography
        - Etching — Add
        - Chemical vapor deposition — Subtract
        - Oxidation — Neither
        - Chemical mechanical polishing (CMP)
    e. Rank the following layers in conductivity from highest (1) to lowest (5):
        - Poly____, Substrate____, Top metal____, N-well____, Metal 1____

3. (15 pts) Layout a minimum sized 400KΩ resistor in a 0.25μ CMOS process. It has a High Resistivity Poly which has $R_{\square}$=1000Ω. Assume the minimum width of HR Poly is 4λ and the minimum spacing is 2λ. Use metal layers to connect between poly strips. Minimum metal width is 4λ. Ignore metal resistance. The total resistor area should have rectangular shape with aspect ratio close to 1:2.

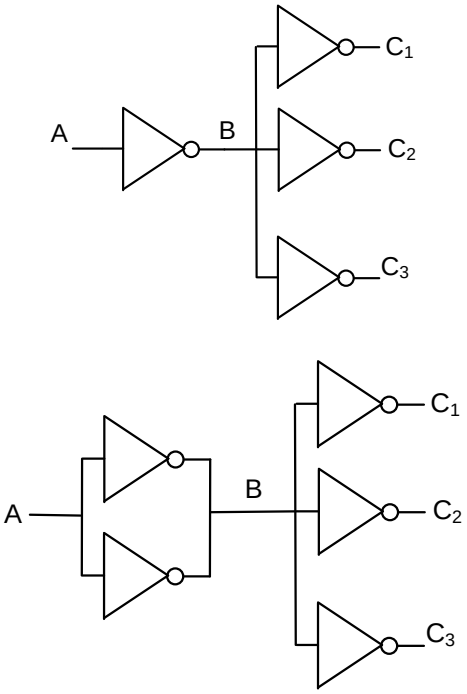
4. (15 pts) For the previous resistor, what is the total layout area? What is the poly resistor area? Suppose the foundry provides random variation A numbers, $A_{\Delta R/R}$=2%μm. What is the σ value of ΔR/R? If we need the 3σ to be ≤0.1% to achieve our yield target, how should we modify our design?

5. (15 pts) The transistor level implementation of a logic block with inputs A, B, and C and an output F is shown below.
    a. Given a Boolean expression for F in terms of the inputs A, B, and C .
    b. Implement the same Boolean function using the compound gate logic approach at the transistor level. Assume the inputs that are available are A, B, and C.



6. (15 pts) Assume 300mm wafers after processing cost $3140 per wafer. If the defect density on these wafers is 1.1/cm^2, determine the cost per good die if the die is square with a side dimension of 3 mm. Assume the soft yield is 100%. Use $e^{\varepsilon} \approx 1+\varepsilon$.

7. (15 pts) Two circuits are shown below that ideally implement the same Boolean function. Though the lower circuit has the outputs of two inverters that are tied together, since the inputs are the same, this is an allowed and actually widely used circuit. Assume the Boolean logic levels for these circuits are 0V and 5V and all transistors are minimum sized. Specify the model you use for the inverters when solving this problem.
   a) If the input A changes from V_{DD} to 0 at time t=0, the output B will subsequently change from low to high. Determine the time it takes for the B output to change states for the upper circuit.
   b) Repeat part a) for the lower circuit.



MOSIS WAFER ACCEPTANCE TESTS

RUN: T4BK (MM_NON-EPI_THK-MTL) VENDOR: TSMC
TECHNOLOGY: SCN018 FEATURE SIZE: 0.18 microns

INTRODUCTION: This report contains the lot average results obtained by MOSIS from measurements of MOSIS test structures on each wafer of this fabrication lot. SPICE parameters obtained from similar measurements on a selected wafer are also attached.

COMMENTS: DSCN6M018_TSMC

TRANSISTOR PARAMETERS	W/L	N-CHANNEL	P-CHANNEL	UNITS
MINIMUM	0.27/0.18			
Vth		0.50	-0.53	volts
SHORT	20.0/0.18			
Idss		571	-266	uA/um
Vth		0.51	-0.53	volts
Vpt		4.7	-5.5	volts
WIDE	20.0/0.18			
Ids0		22.0	-5.6	pA/um
LARGE	50/50			
Vth		0.42	-0.41	volts
Vjbkd		3.1	-4.1	volts
Ijlk		<50.0	<50.0	pA
K' (Uo*Cox/2)		171.8	-36.3	uA/V^2
Low-field Mobility		398.02	84.10	cm^2/V*s

COMMENTS: Poly bias varies with design technology. To account for mask bias use the appropriate value for the parameters XL and XW in your SPICE model card.

Design Technology	XL (um)	XW (um)
SCN6M_DEEP (lambda=0.09)	0.00	-0.01
thick oxide	0.00	-0.01
SCN6M_SUBM (lambda=0.10)	-0.02	0.00
thick oxide	-0.02	0.00

FOX TRANSISTORS	GATE	N+ACTIVE	P+ACTIVE	UNITS
Vth	Poly	>6.6	<-6.6	volts

PROCESS PARAMETERS	N+	P+	POLY	N+BLK	PLY+BLK	M1	M2	UNITS
Sheet Resistance	6.6	7.5	7.7	61.0	317.1	0.08	0.08	ohms/sq
Contact Resistance	10.1	10.6	9.3				4.18	ohms
Gate Oxide Thickness	40							angstrom

PROCESS PARAMETERS	M3	POLY_HRI	M4	M5	M6	N_W	UNITS
Sheet Resistance	0.08	991.5	0.08	0.08	0.01	941	ohms/sq
Contact Resistance	8.97		14.09	18.84	21.44		ohms

COMMENTS: BLK is silicide block.

CAPACITANCE PARAMETERS

	N+	P+	POLY	M1	M2	M3	M4	M5	M6	R_W	D_N_W	M5P	N_W	UNITS
Area (substrate)	998	1152	103	39	19	13	9	8	3		129		127	aF/um^2
Area (N+active)			8566	54	21	14	11	10	9					aF/um^2
Area (P+active)			8324											aF/um^2
Area (poly)				64	18	10	7	6	5					aF/um^2
Area (metal1)					44	16	10	7	5					aF/um^2
Area (metal2)						38	15	9	7					aF/um^2
Area (metal3)							40	15	9					aF/um^2
Area (metal4)								37	14					aF/um^2
Area (metal5)									36			1003		aF/um^2
Area (r well)	987													aF/um^2
Area (d well)										574				aF/um^2
Area (no well)	139													aF/um^2
Fringe (substrate)	244	201		18	61	55	43	25						aF/um
Fringe (poly)				69	39	29	24	21	19					aF/um
Fringe (metal1)					61	35		23	21					aF/um
Fringe (metal2)						54	37	27	24					aF/um
Fringe (metal3)							56	34	31					aF/um
Fringe (metal4)								58	40					aF/um
Fringe (metal5)									61					aF/um
Overlap (P+active)			652											aF/um

CIRCUIT PARAMETERS			UNITS
Inverters	K		
Vinv	1.0	0.74	volts
Vinv	1.5	0.78	volts
Vol (100 uA)	2.0	0.08	volts
Voh (100 uA)	2.0	1.63	volts
Vinv	2.0	0.82	volts
Gain	2.0	-23.33	
Ring Oscillator Freq.			
D1024_THK (31-stg,3.3V)		338.22	MHz
DIV1024 (31-stg,1.8V)		402.84	MHz
Ring Oscillator Power			
D1024_THK (31-stg,3.3V)		0.07	uW/MHz/gate
DIV1024 (31-stg,1.8V)		0.02	uW/MHz/gate

COMMENTS: DEEP_SUBMICRON