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### Problem 1:

In figure 1.4 we can find the count of transistors in the processor increases by about  $\sim 10$  times per seven years. In 2002 the count was about 0.1 Billion, so we can predict the count in 2020 to be about

0.1 <u>billion \* 10^(18/7) = 37.28 billion.</u>

The answers to this problem will vary considerably as it is an extrapolation question

## Problem 2:

The transistor level schematic for a CMOS 3-input NAND gate can be made like this (other ways are possible)



### Problem 3:

Area of die =  $A_{dir} = (5mm)^2 = 25 mm^2 = 0.25cm^2$ Area of wafer =  $A_{wafer} = \left(\frac{300}{2}\right)^2 * \pi = 70685mm^2 = 706.85 cm^2$ Hard yield of die  $Y_H = e^{-Adie*d} = e^{-.25*1.4} = e^{-0.157} = 0.705$ The total yield  $Y = Y_H * Y_S = 0.705 * 1 = 0.705$ The cost per good die  $C_{good} = \frac{C_{wafer}}{A_{wafer}/A_{die}} * \frac{1}{Y} = \frac{\$3200}{\frac{70685}{25}} * \frac{1}{0.705} = \$1.605$ 

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### Problem 4:

$$Y = \frac{x-u}{g} = \frac{3mv - 0mv}{1.5 mv} = \frac{3}{2} = 1.5$$

$$P_{Soft\_Amp} = \int_{-1.5}^{1.5} f(x) \, dx = 2F_N(1.5) - 1 = 0.866$$
There are multiple ways to perform this step

Two Op Amps per chip  $P_{Soft\_chip} = 0.866^2 = 0.750$ 

#### **Problem 5:**

Since the input offset voltage follow Gaussian distribution we have the soft yield  $\theta$ :

 $Y_s = P_{soft} = 2F_N(y) - 1 = 0.98 = F_N(y) = 0.990$ 

There are multiple ways to perform this step.

$$y = 2.33 = \frac{x-u}{g} = \frac{1.5mv-0}{\left(\frac{20mV\mu m}{\sqrt{A}}\right)} => A = \frac{965.14\,\mu m^2}{965.14\,\mu m^2}$$

### **Problem 6:**

The area of a die in new process  $= A_{die} = \left(\frac{7}{65}\right)^2 * 0.5cm^2 = 5.7988 * 10^{-3}cm^2$ The hard yield  $= Y_H = e^{-A_{die}*d} = e^{-0.00696} = 0.9931$ The yield  $Y = Y_H * Y_S = 0.9931$ 

 $C_{good} = \frac{C_{wafer}}{(A_{wafer}/A_{die})} * \frac{1}{Y} = \frac{\$10000}{\frac{1590.4}{0.005799}} * \frac{1}{0.9931} = \$0.0367$ 

# Problem 7:

This switch level model assumes A = 1 and  $\overline{C} = 1$ .



An inverter should be used to convert C to  $\sim$ C (not shown)

## Problem 8:

When both inputs are 0V the output is  $VDD = \frac{3V}{3V}$ When one input is 0V and the other is 3V the output is  $VDD = \frac{3V}{3V}$ When both inputs are 3V the output is  $VSS = \frac{0V}{3V}$ 

## Problem 9:

Here is one solution to this problem:

```
1 module NOR2 (i_A, i_B, o_F);
2 input i_A, i_B;
3 output o_F;
4 
5 assign o_F = ~(i_A||i_B);
6 
7 endmodule
module OR2 (i_A, i_B, o_F);
input i_A, i_B;
output o_F;
wire A_nor_B;
NOR2 nor0(.i_A(i_A), .i_B(i_B), .o_F(A_nor_B));
NOR2 nor1(.i_A(A_nor_B), .i_B(A_nor_B), .o_F(o_F));
```

endmodule

```
1 module AND2 (i_A, i_B, o_F);
2 input i_A, i_B;
3 output o_F;
4 wire A_not, B_not;
5 
6 | NOR2 nor0(.i_A(i_A), .i_B(i_A), .o_F(A_not));
7 NOR2 nor1(.i_A(i_B), .i_B(i_B), .o_F(B_not));
8 NOR2 nor2(.i_A(A_not), .i_B(B_not), .o_F(o_F));
9 
10 endmodule
```

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```
1
2
3
      module HW2_Problem_TB();
        reg r_A, r_B, r_C;
        wire w F;
 4
        initial
 5
6
7
        begin
          r_{A} = 1'b0;
 8
          r^{B} = 1'b0;
          r_{c} = 1'b0;
 9
10
        end
11
12
        always
          #10 r_A = ~r_A;
13
14
        always
          #20 r_B = ~r_B;
15
16
        always
17
          #40 r_C = ~r_C;
18
19
        HW2_Problem name(.i_A(r_A), .i_B(r_B), .i_C(r_C), .o_F(w_F));
20
21
      endmodule
 1
2
3
      module HW2_Problem (i_A, i_B, i_C, o_F);
        input i_A, i_B, i_C;
        output o_F;
 4
        wire A_not, C_not;
 5
6
7
        wire nA_B, nA_B_C, B_nC, A_B_nC;
       8
 9
10
11
12
13
14
15
      endmodule
```

ireor 1	l n ne l	0.00									
Now	00 ns	ns 10	ns 20	ns 30	ns 40	ns 50	ns 60	ns 70	ns 80	ns 90	ns 100
W_F	0										
r_C	0	L									
r_B	0	l									
<u>-</u> A	U	L									