Homework 3 Spring 2019 TA: Abdullah Al-Obaidi

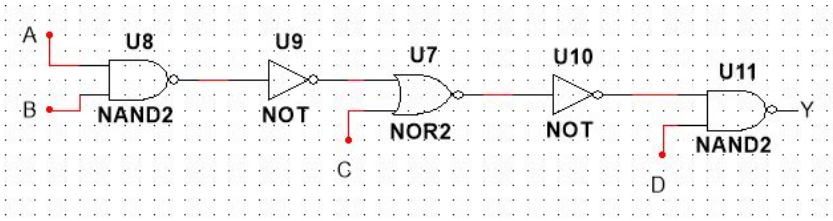
Notes:

Multiple problems (ones involving logical functions implementation and Verilog) have multiple correct answer. Only one example is shown below.

Problem 1:

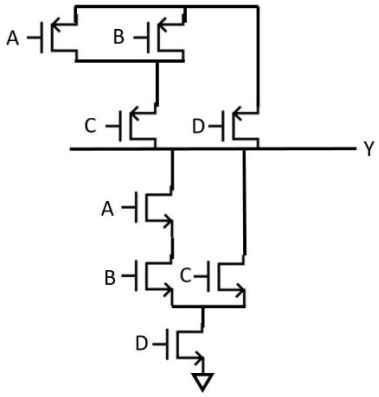
$Y = \overline{(AB + C)D}$

One possible design with static CMOS gates,



This design uses 16 transistors.

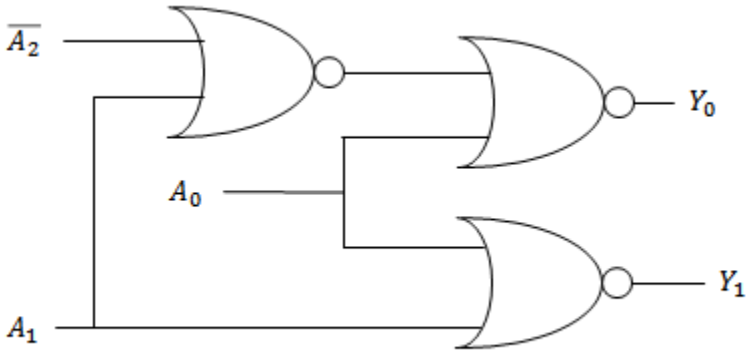
The below is one design for a compound CMOS gate



This design uses 8 transistors

Problem 2:

$Y_0 = \overline{A_0}(A_1 + \overline{A_2})$
$Y_1 = \overline{A_0} * \overline{A_1}$



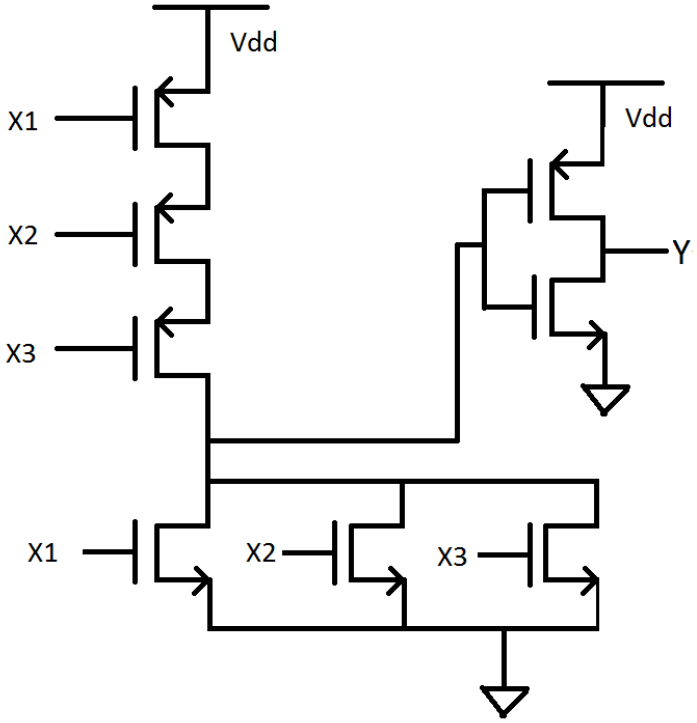
Problem 3:

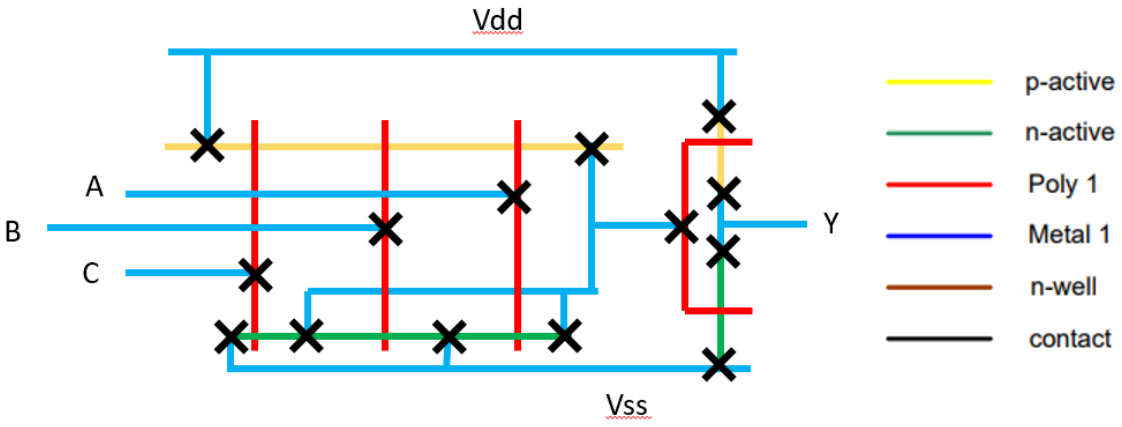
For minimum sized 2 input NOR,

$R_{SWN} = 2k\Omega, R_{SWP} = 6k\Omega, C = 60fF$

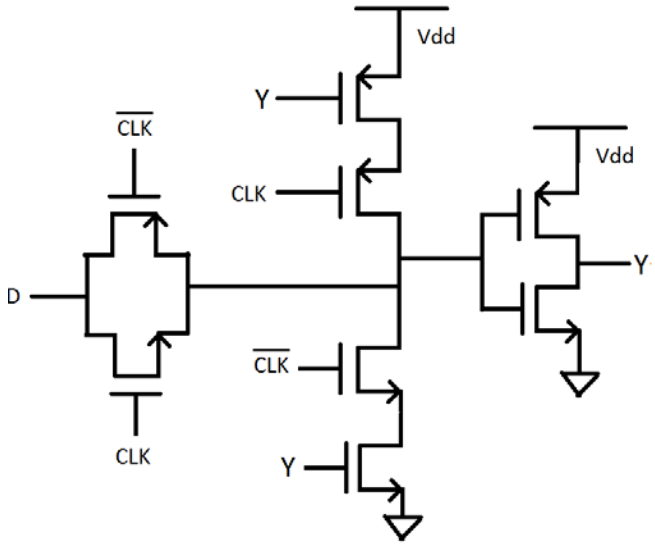
$T_{LH} = 2 * R_{SWP} * C = 12k * 60f = 720 * 10^{-12} seconds = 720pS$

Problem 4:


Vdd
X1
X2
X3
Vdd
Y
X1
X2
X3

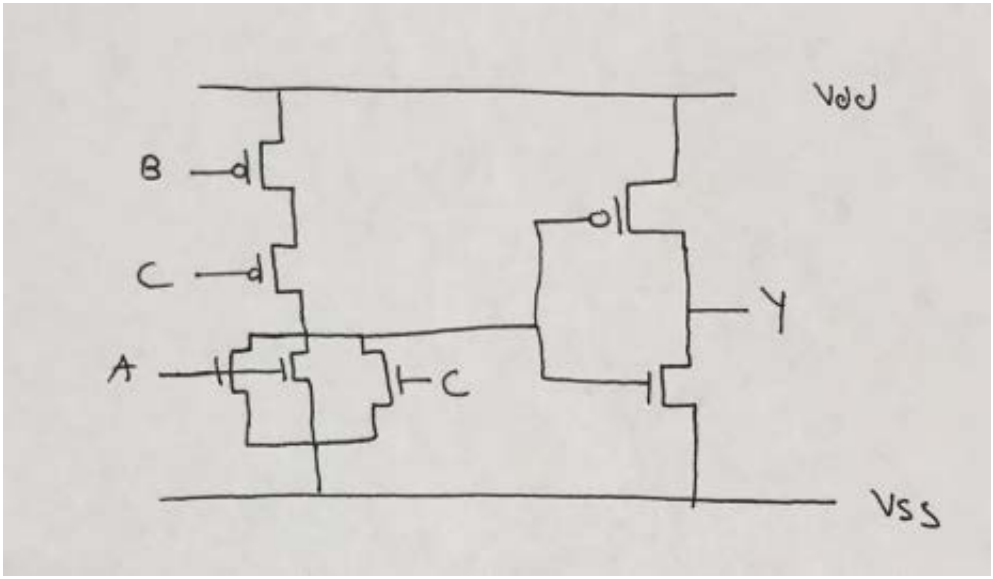

Vdd
A
B
C
Y
Vss
p-active
n-active
Poly 1
Metal 1
n-well
contact

Problem 5:



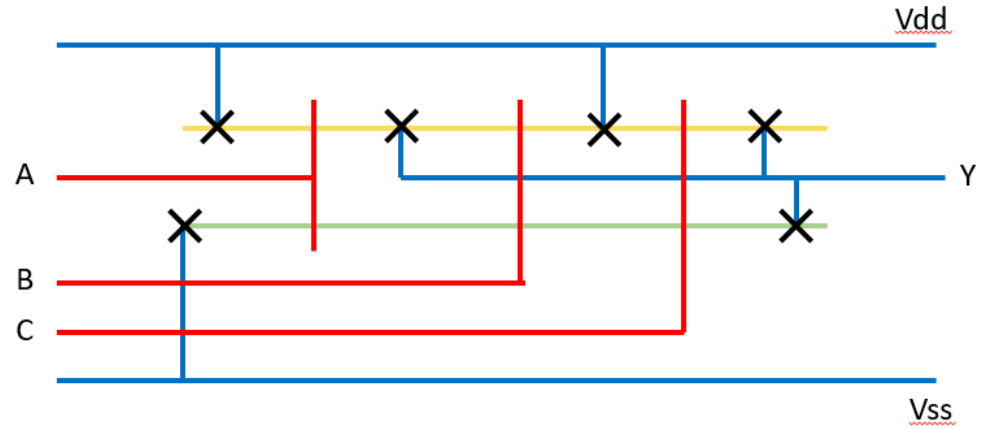
Middle stage can also be realize by splitting it into an inverter and a transmission gate

Problem 6:



Problem 7:

Correct Diagram:



Problem 8:

a) $R_{W\_Aluminum} = \frac{2.8*10^{-8}}{0.2*10^{-6}} * \frac{240}{5} + \frac{2.8*10^{-8}}{0.2*10^{-6}} * \frac{40-5}{5} = 7.7\Omega$

$V_{wire} = 5 * \frac{50}{50+7.7} = 4.33\ V$

b) $R_{W_{Copper}} = 4.675\ \Omega$

$V_{Resistor} = 5 * \left(\frac{50}{50+4.675}\right) = 4.572\ V$

c) $V_{RW} < 5V * 5\% = 0.25V$

$5V * \left(\frac{R_W}{50+R_W}\right) < 0.25V \rightarrow\ R_W < 2.632\ \Omega$

$R_W = 7.7 * \frac{5\mu m}{Width_{wire}} \rightarrow Width_{Wire} \geq 14.63\ \mu m$

Problem 9:

Each inverter has $C_L = 1.5\ fF + 1.5\ fF = 3fF$

total load capacitance $C = 3\ pF * 6 = 18\ fF$

$R_{SWp} = 6k\Omega \rightarrow T_{LH} = 6\ k * 18\ f = 108 * 10^{-12} s = 108\ ps$

Problem 10:

This is one simple implementation. The mux module and the test bench can be made in multiple ways.

Base Code:

```
module MUX (A,B,SEL,F);
input[1:0] A,B;
input SEL;
output[1:0] F;
assign F = SEL ? A : B;
endmodule
```

Test bench Code:

```
module mux_tb();
reg[1:0] A, B;
reg SEL;
wire[1:0] F;

initial
begin
 A = 0;
 B = 0;
 SEL = 0;
end

always
#10 SEL = ~SEL;
always
#20 A = A + 1;
always
#40 B = B + 1;

MUX test(.A(A), .B(B), .SEL(SEL), .F(F));
endmodule
```

Simulation results: