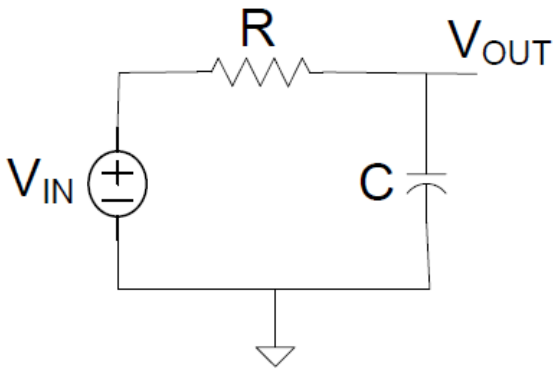
EE 330
Homework Assignment 5
Spring 2019 (Due Friday Feb 15th)

Problem 1 How many 12 inch wafers can be obtained from a 2m silicon pull? Assume the kerf width when a wire saw is used is to cut the wafers is 150μm. In solving this problem, state and use a typical value for the wafer thickness.

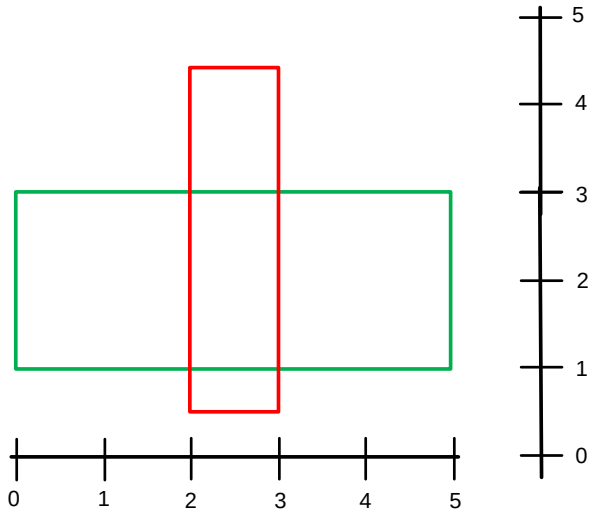
Problem 2 A first-order RC filter is shown. The 3-dB band edge of this filter is given by $\omega_{3dB} = \frac{1}{RC}$. Assume Poly 1 is used to make the resistor and the capacitor is a Poly Insulator M1 capacitor. This filter is to be fabricated in the TSMC 0.18μ CMOS process that is characterized by the parameters attached to this assignment.

a) Design this circuit and estimate the layer's area required to implement this filter in your design if the 3dB band edge is to be located at 1K Hz and the capacitor value is 8 pF. (Only consider area of resistor and capacitor, ignore V_{IN}, wires and groud)

b) If the resistor is too big or the capacitor is too big, the area required to realize this filter becomes very large. Determine the value of R and C that will minimize the total area and compare the area required for this design with that you required in part a).



Problem 3 Consider the layout of a transistor shown below where red is polysilicon and green is n-active. Rulers with dimensions in µm are shown.



a) What is the drawn length and width of the transistor?
b) Assume positive photoresist is used pattern the polysilicon region to protect it during the polysilicon etch. If the photoresist is over-exposed so that the edges move by 0.1µm from the desired location and the photoresist development is perfect, and the polysilicon is under-etched so that the edges move by 0.1µm, what will be the actual length and width of the transistor?
c) Repeat part b) if negative photoresist is used.

Problem 4 Thermal oxide growth of field oxide causes the wafer surface to become somewhat nonplanar. If 5000Å of field oxide is thermally grown, what is the difference in the thickness of the wafer between regions where field oxide is present and where it is absent. In solving this problem, state and use a typical value for the wafer thickness.

Problem 5 Design a 3K (+/- 2%) resistor in the TSMC 0.18µ CMOS process. Use Poly 1 with a silicide block for the resistor. The width-length ratio of an imaginary box enclosing the resistor should have a W/L ratio of between 1:2 and 2:1. The layout of the resistor can be either sketched or come from a Cadence layout.

Problem 6 Design a 500fF capacitor in the TSMC 0.18µ CMOS process. Clearly specify which layers you are using for this capacitor. The layout of the capacitor can be either sketched or come from a Cadence layout.

Problem 7 Assume a resistor has a resistance of 4.534KΩ at T=250°K. If the TCR of this resistor is constant of value 1200 ppm/°C, what will be the resistance at T=320°K?

Problem 8 Consider a Poly 1 (without silicide block) interconnect in the 0.18µ CMOS process that is 1µ wide and 100µ long. What is the resistance of this interconnect? What is the capacitance from this interconnect to the substrate? If Metal 1 is above this interconnect, what is the capacitance between this interconnect and Metal 1?

Problem 9-10 Use Modelsim create a one-bit Half Adder. For the inputs use two one-bit inputs. For the outputs, use a one-bit output and a carry out bit. Create a test bench for the code ad show the results and waveforms.

MOSIS WAFER ACCEPTANCE TESTS

RUN: T4BK (MM_NON-EPI_THK-MTL) VENDOR: TSMC
TECHNOLOGY: SCN018 FEATURE SIZE: 0.18 microns

INTRODUCTION: This report contains the lot average results obtained by MOSIS from measurements of MOSIS test structures on each wafer of this fabrication lot. SPICE parameters obtained from similar measurements on a selected wafer are also attached.

COMMENTS: DSCN6M018_TSMC

TRANSISTOR PARAMETERS	W/L	N-CHANNEL	P-CHANNEL	UNITS
MINIMUM	0.27/0.18			
Vth		0.50	-0.53	volts
SHORT	20.0/0.18			
Idss		571	-266	uA/um
Vth		0.51	-0.53	volts
Vpt		4.7	-5.5	volts
WIDE	20.0/0.18			
Ids0		22.0	-5.6	pA/um
LARGE	50/50			
Vth		0.42	-0.41	volts
Vjbkd		3.1	-4.1	volts
Ijlk		<50.0	<50.0	pA
K' (Uo*Cox/2)		171.8	-36.3	uA/V^2
Low-field Mobility		398.02	84.10	cm^2/V*s

COMMENTS: Poly bias varies with design technology. To account for mask bias use the appropriate value for the parameters XL and XW in your SPICE model card.

Design Technology	XL (um)	XW (um)
SCN6M_DEEP (lambda=0.09)	0.00	-0.01
thick oxide	0.00	-0.01
SCN6M_SUBM (lambda=0.10)	-0.02	0.00
thick oxide	-0.02	0.00

FOX TRANSISTORS	GATE	N+ACTIVE	P+ACTIVE	UNITS
Vth	Poly	>6.6	<-6.6	volts

PROCESS PARAMETERS	N+	P+	POLY	N+BLK	PLY+BLK	M1	M2	UNITS
Sheet Resistance	6.6	7.5	7.7	61.0	317.1	0.08	0.08	ohms/sq
Contact Resistance	10.1	10.6	9.3				4.18	ohms
Gate Oxide Thickness	40							angstrom

PROCESS PARAMETERS	M3	POLY_HRI	M4	M5	M6	N_W	UNITS
Sheet Resistance	0.08	991.5	0.08	0.08	0.01	941	ohms/sq
Contact Resistance	8.97		14.09	18.84	21.44		ohms

COMMENTS: BLK is silicide block.

CAPACITANCE PARAMETERS

	N+	P+	POLY	M1	M2	M3	M4	M5	M6	R_W	D_N_W	M5P	N_W	UNITS
Area (substrate)	998	1152	103	39	19	13	9	8	3		129		127	aF/um^2
Area (N+active)			8566	54	21	14	11	10	9					aF/um^2
Area (P+active)			8324											aF/um^2
Area (poly)				64	18	10	7	6	5					aF/um^2
Area (metal1)					44	16	10	7	5					aF/um^2
Area (metal2)						38	15	9	7					aF/um^2
Area (metal3)							40	15	9					aF/um^2
Area (metal4)								37	14					aF/um^2
Area (metal5)									36			1003		aF/um^2
Area (r well)	987													aF/um^2
Area (d well)										574				aF/um^2
Area (no well)	139													aF/um^2
Fringe (substrate)	244	201		18	61	55	43	25						aF/um
Fringe (poly)				69	39	29	24	21	19					aF/um
Fringe (metal1)					61	35		23	21					aF/um
Fringe (metal2)						54	37	27	24					aF/um
Fringe (metal3)							56	34	31					aF/um
Fringe (metal4)								58	40					aF/um
Fringe (metal5)									61					aF/um
Overlap (P+active)			652											aF/um

CIRCUIT PARAMETERS			UNITS
Inverters	K		
Vinv	1.0	0.74	volts
Vinv	1.5	0.78	volts
Vol (100 uA)	2.0	0.08	volts
Voh (100 uA)	2.0	1.63	volts
Vinv	2.0	0.82	volts
Gain	2.0	-23.33	
Ring Oscillator Freq.			
D1024_THK (31-stg,3.3V)		338.22	MHz
DIV1024 (31-stg,1.8V)		402.84	MHz
Ring Oscillator Power			
D1024_THK (31-stg,3.3V)		0.07	uW/MHz/gate
DIV1024 (31-stg,1.8V)		0.02	uW/MHz/gate

COMMENTS: DEEP_SUBMICRON

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SPICE 3f5 Level 8, Star-HSPICE Level 49, UTMOST Level 8
* DATE: Jan 21/05
* LOT: T4BK                    WAF: 3004
* Temperature_parameters=Default
.MODEL CMOSN NMOS (                                LEVEL   = 49
+VERSION = 3.1            TNOM    = 27             TOX     = 4E-9
+XJ      = 1E-7           NCH     = 2.3549E17      VTH0    = 0.3662648
+K1      = 0.5802748      K2      = 3.124029E-3    K3      = 1E-3
+K3B     = 3.3886871      W0      = 1E-7           NLX     = 1.766159E-7
+DVT0W   = 0              DVT1W   = 0              DVT2W   = 0
+DVT0    = 1.2312416      DVT1    = 0.3849841      DVT2    = 0.0161351
+U0      = 265.1889031    UA      = -1.506402E-9   UB      = 2.489393E-18
+UC      = 5.621884E-11   VSAT    = 1.017932E5     A0      = 2
+AGS     = 0.4543117      B0      = 3.433489E-7    B1      = 5E-6
+KETA    = -0.0127714     A1      = 1.158074E-3    A2      = 1
+RDSW    = 136.5582806    PRWG    = 0.5            PRWB    = -0.2
+WR      = 1              WINT    = 0              LINT    = 1.702415E-8
+XL      = 0              XW      = -1E-8          DWG     = -4.211574E-9
+DWB     = 1.107719E-8    VOFF    = -0.0948017     NFACTOR = 2.1860065
+CIT     = 0              CDSC    = 2.4E-4         CDSCD   = 0
+CDSCB   = 0              ETA0    = 3.335516E-3    ETAB    = 6.028975E-5
+DSUB    = 0.0214781      PCLM    = 0.6602119      PDIBLC1 = 0.1605325
+PDIBLC2 = 3.287142E-3    PDIBLCB = -0.1           DROUT   = 0.7917811
+PSCBE1  = 6.420235E9     PSCBE2  = 4.122516E-9    PVAG    = 0.0347169
+DELTA   = 0.01           RSH     = 6.6            MOBMOD  = 1
+PRT     = 0              UTE     = -1.5           KT1     = -0.11
+KT1L    = 0              KT2     = 0.022          UA1     = 4.31E-9
+UB1     = -7.61E-18      UC1     = -5.6E-11       AT      = 3.3E4
+WL      = 0              WLN     = 1              WW      = 0
+WWN     = 1              WWL     = 0              LL      = 0
+LLN     = 1              LW      = 0              LWN     = 1
+LWL     = 0              CAPMOD  = 2              XPART   = 0.5
+CGDO    = 8.06E-10       CGSO    = 8.06E-10       CGBO    = 1E-12
+CJ      = 9.895609E-4    PB      = 0.8            MJ      = 0.3736889
+CJSW    = 2.393608E-10   PBSW    = 0.8            MJSW    = 0.1537892
+CJSWG   = 3.3E-10        PBSWG   = 0.8            MJSWG   = 0.1537892
+CF      = 0              PVTH0   = -1.73163E-3    PRDSW   = -1.4173554
+PK2     = 1.600729E-3    WKETA   = 1.601517E-3    LKETA   = -3.255127E-3
+PU0     = 5.2024473      PUA     = 1.584315E-12   PUB     = 7.446142E-25
+PVSAT   = 1.686297E3     PETA0   = 1.001594E-4    PKETA   = -2.039532E-3
)
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.MODEL CMOSP PMOS (                                LEVEL   = 49
+VERSION = 3.1            TNOM    = 27             TOX     = 4E-9
+XJ      = 1E-7           NCH     = 4.1589E17      VTH0    = -0.3708038
+K1      = 0.5895473      K2      = 0.0235946      K3      = 0
+K3B     = 13.8642028     W0      = 1E-6           NLX     = 1.517201E-7
+DVT0W   = 0              DVT1W   = 0              DVT2W   = 0
+DVT0    = 0.7885088      DVT1    = 0.2564577      DVT2    = 0.1
+U0      = 103.0478426    UA      = 1.049312E-9    UB      = 2.545758E-21
+UC      = -1E-10         VSAT    = 1.645114E5     A0      = 1.627879
+AGS     = 0.3295499      B0      = 5.207699E-7    B1      = 1.370868E-6
+KETA    = 0.0296157      A1      = 0.4449009      A2      = 0.3
+RDSW    = 306.5789827    PRWG    = 0.5            PRWB    = 0.5
+WR      = 1              WINT    = 0              LINT    = 2.761033E-8
+XL      = 0              XW      = -1E-8          DWG     = -2.433889E-8
+DWB     = -9.34648E-11   VOFF    = -0.0867009     NFACTOR = 2
+CIT     = 0              CDSC    = 2.4E-4         CDSCD   = 0
+CDSCB   = 0              ETA0    = 1.018318E-3    ETAB    = -3.206319E-4
+DSUB    = 1.094521E-3    PCLM    = 1.3281073      PDIBLC1 = 2.394169E-3
+PDIBLC2 = -3.255915E-6   PDIBLCB = -1E-3          DROUT   = 0
+PSCBE1  = 4.881933E10    PSCBE2  = 5E-10          PVAG    = 2.0932623
+DELTA   = 0.01           RSH     = 7.5            MOBMOD  = 1
+PRT     = 0              UTE     = -1.5           KT1     = -0.11
+KT1L    = 0              KT2     = 0.022          UA1     = 4.31E-9
+UB1     = -7.61E-18      UC1     = -5.6E-11       AT      = 3.3E4
+WL      = 0              WLN     = 1              WW      = 0
+WWN     = 1              WWL     = 0              LL      = 0
+LLN     = 1              LW      = 0              LWN     = 1
+LWL     = 0              CAPMOD  = 2              XPART   = 0.5
+CGDO    = 6.52E-10       CGSO    = 6.52E-10       CGBO    = 1E-12
+CJ      = 1.157423E-3    PB      = 0.8444261      MJ      = 0.4063933
+CJSW    = 1.902456E-10   PBSW    = 0.8            MJSW    = 0.3550788
+CJSWG   = 4.22E-10       PBSWG   = 0.8            MJSWG   = 0.3550788
+CF      = 0              PVTH0   = 1.4398E-3      PRDSW   = 0.5073407
+PK2     = 2.190431E-3    WKETA   = 0.0442978      LKETA   = -2.936093E-3
+PU0     = -0.9769623     PUA     = -4.34529E-11   PUB     = 1E-21
+PVSAT   = -50            PETA0   = 1.002762E-4    PKETA   = -6.740436E-3
)
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TRANSISTOR PARAMETERS	W/L	N-CHANNEL	P-CHANNEL	UNITS
MINIMUM	3.0/0.6			
Vth		0.78	-0.93	volts
SHORT	20.0/0.6			
Idss		439	-238	uA/um
Vth		0.69	-0.90	volts
Vpt		10.0	-10.0	volts
WIDE	20.0/0.6			
Ids0		< 2.5	< 2.5	pA/um
LARGE	50/50			
Vth		0.70	-0.95	volts
Vjbkd		11.4	-11.7	volts
Ijlk		<50.0	<50.0	pA
Gamma		0.50	0.58	V^0.5
K' (Uo*Cox/2)		56.9	-18.4	uA/V^2
Low-field Mobility		474.57	153.46	cm^2/V*s

COMMENTS: XL_AMI_C5F

FOX TRANSISTORS	GATE	N+ACTIVE	P+ACTIVE	UNITS
Vth	Poly	>15.0	<-15.0	volts

PROCESS PARAMETERS	N+ACTV	P+ACTV	POLY	PLY2_HR	POLY2	MTL1	MTL2	UNITS
Sheet Resistance	82.7	103.2	21.7	984	39.7	0.09	0.09	ohms/sq
Contact Resistance	56.2	118.4	14.6		24.0		0.78	ohms
Gate Oxide Thickness	144							angstrom

PROCESS PARAMETERS	MTL3	N\PLY	N_WELL	UNITS
Sheet Resistance	0.05	824	815	ohms/sq
Contact Resistance	0.78			ohms

COMMENTS: N\POLY is N-well under polysilicon.

CAPACITANCE PARAMETERS	N+ACTV	P+ACTV	POLY	POLY2	M1	M2	M3	N_WELL	UNITS
Area (substrate)	429	721	82		32	17	10	40	aF/um^2
Area (N+active)			2401		36	16	12		aF/um^2
Area (P+active)			2308						aF/um^2
Area (poly)				864	61	17	9		aF/um^2
Area (poly2)					53				aF/um^2
Area (metal1)						34	13		aF/um^2
Area (metal2)							32		aF/um^2
Fringe (substrate)	311	256			74	58	39		aF/um
Fringe (poly)					53	40	28		aF/um
Fringe (metal1)						55	32		aF/um
Fringe (metal2)							48		aF/um
Overlap (N+active)			206						aF/um
Overlap (P+active)			278						aF/um