EE 330
Homework 7 Solutions

Problem 1

For the circuit on the left, the anode voltage can't exceed the cathode voltage of 15 V, so diode is off.

$I_1 = \frac{7}{4k + 2k} = 1.17\ mA$

For the circuit on the right, initially consider the diode is off. In this case the resistors act as a voltage divider so V_D = 15*(4/6) = 10V>9V. So our initial assumption is wrong and the diode is on.

$I_2 = \frac{9.7}{4k} = 2.4\ mA$

Problem 2.

A. $V_{OUT} = I(10k\Omega) + 0.575V, V_t = \frac{kT}{g}, I(T) = \left[J_{SX}\left(T^m e^{\frac{-V_{go}}{V_t}}\right)\right] A * e^{\frac{V_D}{V_t}}$

$$A * J_{SX}\left[T^m e^{\frac{-V_{go}}{V_t}}\right] * e^{\frac{0.575}{V_t}} = \frac{0.5A}{\mu^2} * [1.63 * 10^{-18}] * 200\mu^2 * 287.19 * 10^9$$

B. $V_{OUT} = 145V \rightarrow 20V$ (clipping)

C. $V_{OUT} = 12.8kV \rightarrow 20V$ (clipping)

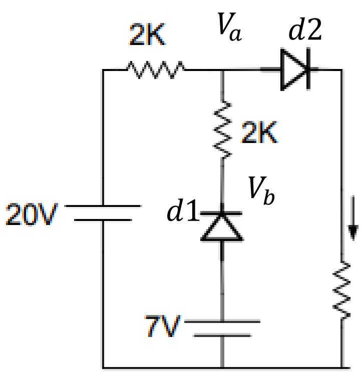
Problem 3

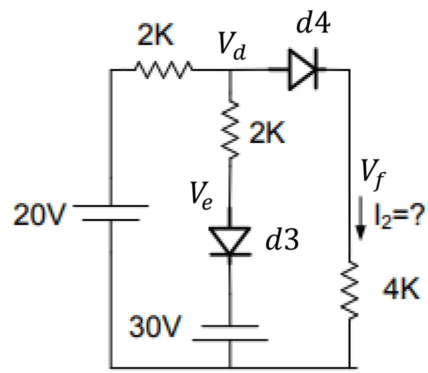
For the left figure:

Initially assume both diodes to be 'on'. Thus, $V_b = 7 - 0.6 = 6.4V$. Applying KCL at V_a will yields $V_a = 10.7V$. However, this would mean that the current through diode d1 is flowing from cathode to anode, which is incorrect. Thus, our assumption that diode d1 is on is "incorrect". Now, calculating V_a with diode d1 off and d2 on, yields $V_a = 13.5V$. Thus, $I_1 = \frac{13.5V - 0.6}{4k} = 3.2mA$.

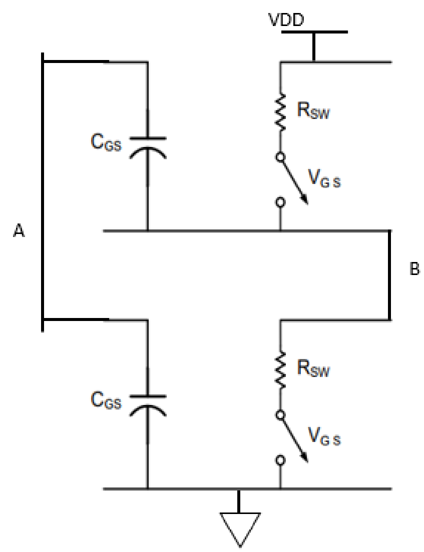
For the right figure,

Assuming both diodes are on. Thus, $V_e = -30 + 0.6 = -29.4V$ then the voltage at $V_d = -3.64V(using\ KCL)$. Thus, diode is off and I_2=0.





Problem 4

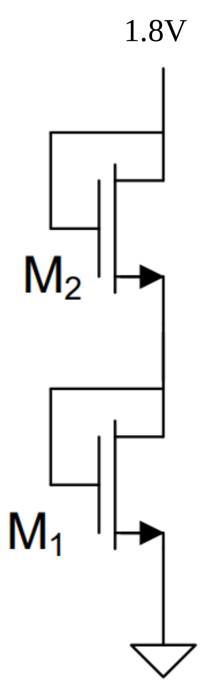


$$R_{sqn} = \frac{1}{\frac{\mu C_{ox} W}{L}(V_{GS} - V_T)} = \frac{1}{\frac{300\mu A}{V^2} * \frac{5\mu}{1\mu} * (1.8 - 0.5)} = 512\Omega$$

$$R_{sqp} = \frac{1}{\frac{75\mu A}{V^2} * \frac{20\mu}{2\mu} * (1.8 - 0.5)} = 1026\Omega$$

$$C_{GSN} = C_{OX}WL = (2.5fFu^{-2})(5\mu * 1\mu) = 12.5\ fF$$

$$C_{GSP} = (2.5fF\mu^{-2})(20\mu * 2\mu) = 100fF$$



Problem 5

Both transistors are in saturation.

$$u_n C_{OX} * \frac{W_1}{2L_1} * (V_{out} - V_{ss} - V_T)^2 = u_n C_{OX} * \frac{W_2}{2L_2} * (V_{DD} - V_{out} - V_T)^2$$

$$u_n C_{OX} * \frac{W_1}{2L_1} * (1V - 0V - 0.5V)^2 = u_n C_{OX} * \frac{W_2}{2L_2} * (2.5V - 1V - 0.5V)^2$$

$$\frac{W_1}{L_1} * (0.8V - 0.5V)^2 = \frac{W_2}{L_2} * (1.8V - 0.8V - 0.5V)^2$$

$$\frac{(W_2/L_2)}{(W_1/L_1)} = \frac{(0.8V - 0.5V)^2}{(1.8V - 0.8V - 0.5V)^2} = 0.6$$

$$If\ \frac{W_1}{L_1} = \frac{2\mu}{0.2\mu} = 10\ then\ \frac{W_2}{L_2} = \frac{1.2\mu}{0.2\mu} = 6$$

Problem 6

A.) $\alpha = \frac{I_C}{I_E} = \frac{1.00mA}{1.0250mA} = 0.9756$

$$\beta = \frac{\alpha}{1-\alpha} = \frac{0.9756}{1-0.9756} = 40$$

B.) $\alpha = \frac{1.00mA*1.005}{1.0250*(1-.005)} = 0.985$

$$\beta = \frac{0.985}{1-0.985} = 67.56$$

$$Error = \frac{67.56-40}{40} = 0.689 = 68.9\%$$

Problem 7

$$I_B = \frac{I_C}{\beta} = \frac{1.00mA}{40} = 25\mu A$$

$$\beta = \frac{I_C}{I_B} = \frac{1.00mA*1.005}{25\mu A*0.995} = 40.402$$

$$Error = \frac{40.402-40}{40} = 0.01005 = 1.005\%$$

Problem 8.

Assuming saturation:

$$I_{D_1} = 75*10^{-6}*\frac{5}{2*5}*(1.8-1-0.5)^2 = I_{D_2} = 300*10^{-6}\left(\frac{5}{10}\right)(V_{out}-0.5)^2$$

$V_{out} = 0.35V\ or\ 0.65V$, given $0.35 < 0.5$,

$V_{out} = 0.65V$

Problem 9

A.) $I_C = \frac{8V-5V}{3k\Omega} = 1.00mA$

$$V_t = \left(8.617*10^{-5}\frac{eV}{K}\right)(300K) = 25.85mV$$

$$I_C = J_s A_E e^{\frac{V_{BE}}{V_t}} = 20*10^{-14}*100*e^{\frac{V_{BE}}{25.85mV}} \rightarrow V_{BE} = V_x = 0.4582567V$$

B.) $I_C = J_s A_E e^{\frac{V_{BE}}{V_t}} = 20*10^{-14}*100*e^{\frac{0.536V-10uV}{25.85mV}} = 999.6uA$

$V_C = 8V - 3k\Omega*999.6uA = 5.00118\ V$

$$Change = \frac{5.00118-5}{5}*100 = 0.0236\%$$

C.) $V_t = \left(8.617*10^{-5}\frac{eV}{K}\right)(301K) = 25.93mV$

$$I_C = J_s A_E e^{\frac{V_{BE}}{V_t}} = 20 * 10^{-14} * 100 * e^{\frac{V_{BE}}{25.93mV}} \rightarrow V_{BE} = V_{x=} 0.4596749V$$

$$Change = \frac{0.4596749V - 0.4582567V}{0.4582567V} * 100 = 0.31\%$$

D.) A change of 10uV (0.002%) in V_x resulted in a change of 0.0236% at the output. Similarly, a change of 1^{o}C in temperature(keeping the input constant at 0.458V) would result in 3% change in the output voltage. Thus, the circuit seems to be very sensitive to changes in V_x and temperature.

Problem 10

```
`timescale 1ns/1ps
module DFF (D, Q, CLK, EN);
  input D, CLK,  EN;
  output Q;
  reg Q;

  always @(posedge(CLK)) begin
    if(CLK & EN) begin
      assign Q = D;
    end
  else begin
    assign Q = Q;
  end
end
endmodule
```