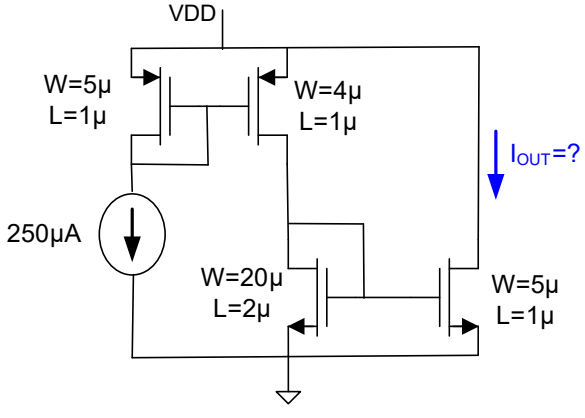
EE 330
Assignment 11
Spring 2019 Due Friday April 12th

Unless specified to the contrary, assume all n-channel MOS transistors have model parameters $\mu_n C_{OX} = 350\mu A/V^2$,$V_{Tn} = 0.5V$, all p-channel transistors have model parameters $\mu_p C_{OX} = 70\mu A/V^2$,$V_{Tp} = -0.5V$, and all JFET devices are from a process with $I_{DSSn0} = 100\mu A$, $I_{DSSp0} = 30\mu A$,$V_{Pp}=1V$, $V_{Pn}=-1V$, and , $\lambda=0$. In this process, assume that for all MOS devices, $L_{MIN}=W_{MIN}=0.18\mu$, and $V_{DD}=2V$. Assume also that a bipolar process is available with parameters $J_S = 10^{-14}A/\mu^2$ and $\beta_n=100$ and $\beta_p = 40$. Unless stated to the contrary, assume the output conductance of the BJT and the MOSFET are characterized, respectively, by $V_{AF}=100V$ and $\lambda=.01V^{-1}$.

Problem 1 Determine I_{OUT}. Assume $V_{DD}=2V$.



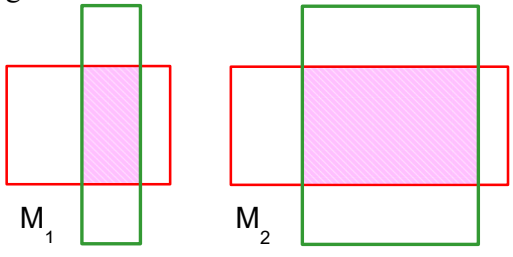
Problem 2 Assume you have available a supply voltage of $V_{DD}=3V$ and a 5 mA sourcing current (one end connected to V_{DD}).

a) Design a current mirror that provides two outputs, a sinking current of 100uA and a sourcing current of 1mA using MOS transistors.

b) What is the maximum voltage at the drain of the transistor providing the 1 mA current source for your design if it is to work as a current mirror?

Problem 3 Design a noninverting amplifier with a nominal gain of +5 that has an input impedance that is between 100K and 200K that can drive a 2K resistive load using MOS transistors, resistors, capacitors, and one dc voltage source.

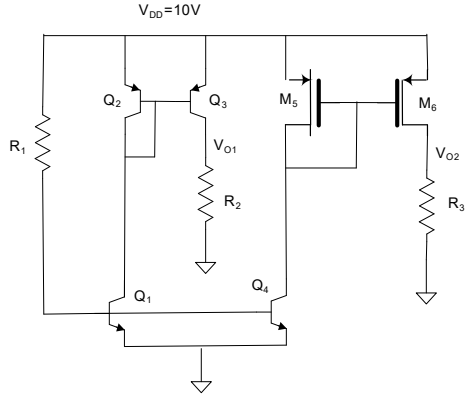
Problem 4 A potential layout strategy for a basic current mirror is shown below where the mirror gain is determined by the W/L ratio of the layout on the right to the W/L ratio of the layout on the left. If an n-channel current mirror is designed using this layout approach with an ideal mirror gain of $M = \frac{W_2}{L_2} \Big/ \frac{W_1}{L_1}$ and with nominal values of $L_1=L_2=4u$ and $W_1=2u$, $W_2=10u$, determine the actual mirror gain if the field oxide encroachment into the active region results in an inward movement of the edges of 0.25u.



Problem 5 Assume the MOS transistors are all operating in the saturation region and the MOS transistors are all operating in the Forward Active region.

a) Determine the output voltages V_{01} and V_{02} in terms of the MOS device dimensions, W and L , the emitter areas, and the resistor variables R_1, R_2, and R_3.

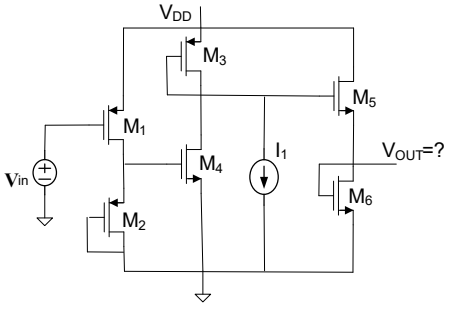
b) If $R_1=80K$, $A_{E1}=A_{E2}=100\mu^2$, $A_{E3}=50\ \mu^2$, $A_{E4}=300\ \mu^2$,$W_5=10\mu$, $L_5=1\mu$,$W_6=16\mu$, $L_6=4\mu$, Determine R_2 and R_3 so that $V_{01}=6V$ and $V_{02}=3V$.



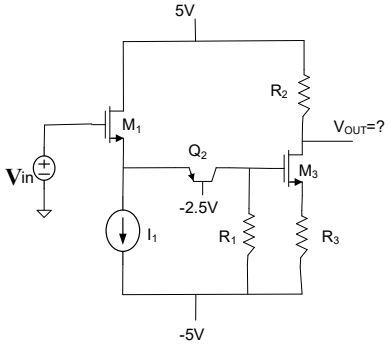
Problem 6 Consider the following amplifier structure where all devices are operating in the saturation region

a) Determine the small signal voltage gain in terms of the small-signal model parameters of the transistors.

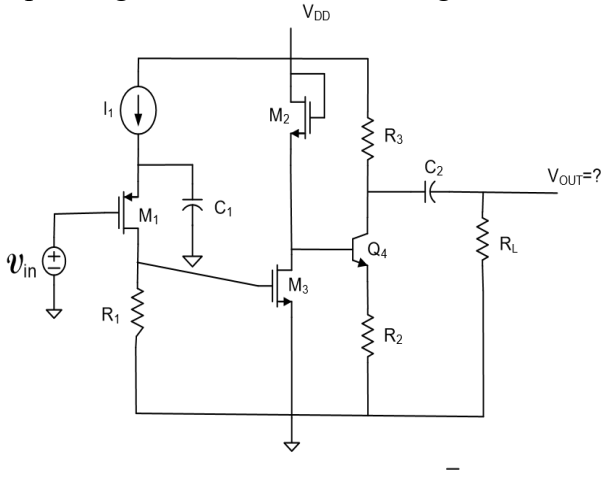
b) Assume V_{DD}=2V, I_1=500uA, and the quiescent current in transistors M_1,M_4, and M_5 is 500uA. Numerically determine the small signal voltage gain if the quiescent voltage on the gate of M_4 is 1V, the voltage on the gate of M_5 is 1.3V, and the quiescent output voltage is 0.7V. Be sure to use the model parameters given at the top of page 1 when solving this problem.



Problem 7 Determine the small signal voltage gain in terms of the small signal model parameters of the devices. Assume the MOS transistors are operating in the saturation region and the bipolar transistor is operating in the forward active region. Assume the MOS transistors are in a 0.5u CMOS process with $\mu_n C_{OX}$=100μA/v^2 ,$\mu_p C_{OX}=\mu_n C_{OX}/3$,V_{TNO}=0.5V, and V_{TP0}= -0.5V.



Problem 8 Determine the small signal voltage gain in terms of the small signal model parameters of the devices. Assume the MOS transistors are operating in the saturation region and the bipolar transistor is operating in the forward active region.



Problem 9 Design a noninverting amplifier using Bipolar transistors with a nominal voltage gain of 60 V/V that has an input impedance larger than 50 kΩ and that can drive a 5 kΩ load resistor. V_{DD} = 1.8 V.

Problem 10 Assume the BJTs are operating in the forward active region and the MOS device is in saturation. Assume all capacitors are very large.

a) Draw the small signal equivalent circuit.

b) Determine an expression for the small-signal voltage gain in terms of the small signal model parameters of the transistors and the passive components