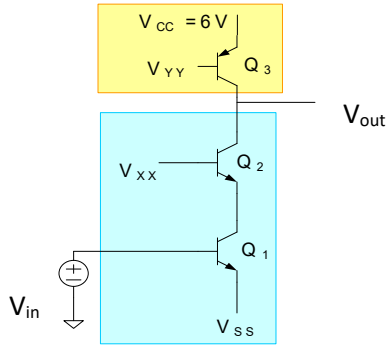
EE 330
Assignment 13
Spring 2019

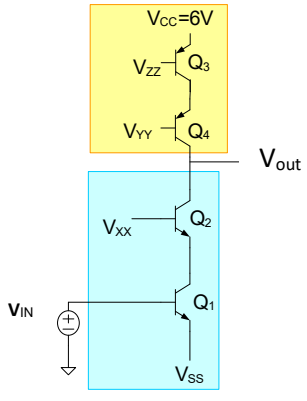
You might need to review Digital Logic from EE/CPRE 281 to be able to answer some of the problems on this assignment

Unless specified to the contrary, assume all n-channel MOS transistors have model parameters $\mu n_{COX} = 350\mu A/V^2$, $V_{Tn} = 0.5V$, all p-channel transistors have model parameters $\mu p_{COX} = 70\mu A/V^2$,$V_{Tp}= -0.5V$, and all JFET devices are from a process with IDSSn0= 100µA, IDSSp0= 30µA,VPp=1V, VPn=-1V, and , λ=0. In this process, assume that for all MOS devices, $L_{MIN}=W_{MIN}=0.18\mu$, and VDD=2V. Assume also that a bipolar process is available with parameters $J_S= 10^{-14}A/\mu^2$ and βn=100 and βp= 40. Unless stated to the contrary, assume the output conductance of the BJT and the MOSFET are characterized, respectively, by $V_{AF}=100V$ and $\lambda=.01V^{-1}$.

Problem 1 Assume the biasing voltages have been selected so that the quiescent current is 1 mA and that all transistors are operating in the forward active region. Determine the small-signal voltage gain. Assume β for all transistors is 100.



Problem 2 Assume the biasing voltages have been selected so that the quiescent current is 1 mA and that all transistors are operating in the forward active region. Determine the small-signal voltage gain. Assume β for all transistors is 100.



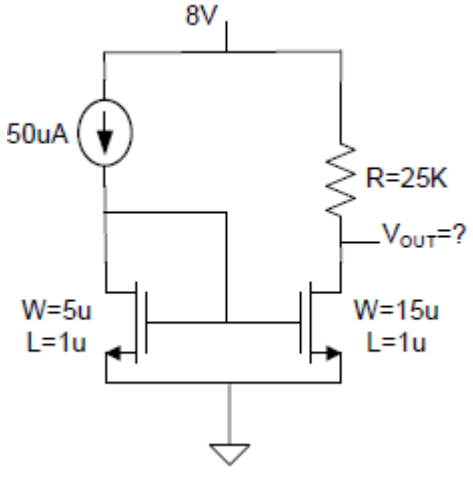
Problem 3 If a DC input voltage of 1uV is placed in series with $\mathbf{V}_{IN}$ in the previous circuit and $V_{OUTQ} = 2V$, how much change in the output voltage from the quiescent value of 2V can be expected? Comment on the implications of this observation.

Problem 4 Assume you have available a 2mA sourcing current (one end connected to V_{DD}) and a single DC voltage source, V_{DD}.

a) Design a current mirror that provides a sinking current of 200 µA using MOS transistors.

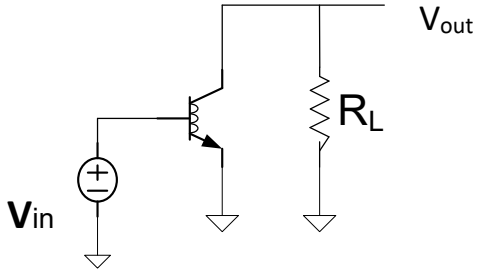
b) What is the minimum voltage on the drain of the 200 µA current source in your design for it to still work as a current mirror?

Problem 5 Determine V_{OUT}



Problem 6 Give all of the two-input Boolean functions and identify which of those are useful or are actually used.

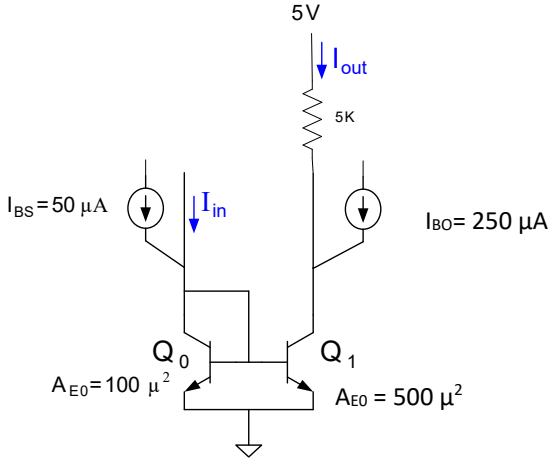
Problem 7 The small-signal equivalent circuit of a common emitter amplifier is shown below. If the emitter area of the BJT is $100\mu^2$ and the load resistor R_L is 10K, bias this circuit so that the quiescent output voltage is 5V and the DC voltage across R_L is also 5V while maintaining the same small signal gain that this circuit has. You have one dc power supply available of any value you choose and any number of resistors and capacitors.



Problem 8 Consider the following circuit.

a) Determine an analytical expression that relates I_{OUT} to I_{IN}

b) With a computer simulation, plot the relationship between I_{OUT} and I_{IN} as I_{IN} is varied between -50uA and +50uA.



Problem 9 A Boolean System is supposed to have an output F that is high when the Boolean inputs A and B are high or when the inputs C and D are high and E is low or when the input A is low and the input E is high.

a) Give a behavioral description of this system in terms of the input/output variables A,B,C,D,E, and F.
b) Write Verilog code describing this system at the behavioral level
c) Give a gate-level structural description of this system if the only gates that are NOR gates with any number of inputs

Problem 10 Give two distinct structural implementations at the gate level of a system with the following Behavioral Description: The output F is high when A is high and B is high or when C is high and B is low. Otherwise the F output is low.

MOSIS WAFER ACCEPTANCE TESTS

RUN: T4BK (MM_NON-EPI_THK-MTL) VENDOR: TSMC
TECHNOLOGY: SCN018 FEATURE SIZE: 0.18 microns

INTRODUCTION: This report contains the lot average results obtained by MOSIS from measurements of MOSIS test structures on each wafer of this fabrication lot. SPICE parameters obtained from similar measurements on a selected wafer are also attached.

COMMENTS: DSCN6M018_TSMC

TRANSISTOR PARAMETERS	W/L	N-CHANNEL	P-CHANNEL	UNITS
MINIMUM	0.27/0.18			
Vth		0.50	-0.53	volts
SHORT	20.0/0.18			
Idss		571	-266	uA/um
Vth		0.51	-0.53	volts
Vpt		4.7	-5.5	volts
WIDE	20.0/0.18			
Ids0		22.0	-5.6	pA/um
LARGE	50/50			
Vth		0.42	-0.41	volts
Vjbkd		3.1	-4.1	volts
Ijlk		<50.0	<50.0	pA
K' (Uo*Cox/2)		171.8	-36.3	uA/V^2
Low-field Mobility		398.02	84.10	cm^2/V*s

COMMENTS: Poly bias varies with design technology. To account for mask bias use the appropriate value for the parameters XL and XW in your SPICE model card.

Design Technology	XL (um)	XW (um)
SCN6M_DEEP (lambda=0.09)	0.00	-0.01
thick oxide (lambda=0.10)	0.00 -0.01 -0.02 0.00	SCN6M_SUBM thick
oxide	-0.02 0.00	

FOX TRANSISTORS	GATE	N+ACTIVE	P+ACTIVE	UNITS
Vth	Poly	>6.6	<-6.6	volts

PROCESS PARAMETERS	N+	P+	POLY	N+BLK	PLY+BLK	M1	M2	UNITS

Sheet Resistance	6.6	7.5	7.7	61.0	317.1	0.08	0.08	ohms/sq
Contact Resistance	10.1	10.6	9.3				4.18	ohms
Gate Oxide Thickness	40							angstrom

PROCESS PARAMETERS	M3	POLY_HRI	M4	M5	M6	N_W	UNITS
Sheet Resistance	0.08	991.5	0.08	0.08	0.01	941	ohms/sq
Contact Resistance	8.97		14.09	18.84	21.44		ohms

COMMENTS: BLK is silicide block.

CAPACITANCE PARAMETERS

	N+	P+	POLY	M1	M2	M3	M4	M5	M6	R_W	D_N_W	M5P	N_W	UNITS
Area (substrate)	998	1152	103	39	19	13	9	8	3		129		127	aF/um^2
Area (N+active)			8566	54	21	14	11	10	9					aF/um^2
Area (P+active)			8324											aF/um^2
Area (poly)				64	18	10	7	6	5					aF/um^2
Area (metal1)					44	16	10	7	5					aF/um^2
Area (metal2)						38	15	9	7					aF/um^2
Area (metal3)							40	15	9					aF/um^2
Area (metal4)								37	14					aF/um^2
Area (metal5)									36			1003		aF/um^2
Area (r well)	987													aF/um^2
Area (d well)										574				aF/um^2
Area (no well)	139													aF/um^2
Fringe (substrate)	244	201		18	61	55	43	25						aF/um
Fringe (poly)				69	39	29	24	21	19					aF/um
Fringe (metal1)					61	35		23	21					aF/um
Fringe (metal2)						54	37	27	24					aF/um
Fringe (metal3)							56	34	31					aF/um
Fringe (metal4)								58	40					aF/um
Fringe (metal5)									61					aF/um
Overlap (P+active)			652											aF/um

CIRCUIT PARAMETERS			UNITS
Inverters	K		
Vinv	1.0	0.74	volts
Vinv	1.5	0.78	volts
Vol (100 uA)	2.0	0.08	volts
Voh (100 uA)	2.0	1.63	volts
Vinv	2.0	0.82	volts
Gain	2.0	-23.33	Ring
Oscillator Freq.			
D1024_THK (31-stg,3.3V)		338.22	MHz
DIV1024 (31-stg,1.8V)		402.84	MHz
Ring Oscillator Power			
D1024_THK (31-stg,3.3V)		0.07	uW/MHz/gate
DIV1024 (31-stg,1.8V)		0.02	uW/MHz/gate

COMMENTS: DEEP_SUBMICRON