EE 330
Assignments 14
Spring 2019
Due Fri April 26th

If references to a semiconductor processes are needed beyond what is given in a specific problem or question, assume a 0.18u CMOS process is available with the following key process parameters; $\mu_n C_{OX}=350\mu A/v^2$, $\mu_p C_{OX} = \mu_n C_{OX}/3$,$V_{TNO}=0.5V$, $V_{TPO}= - 0.5V$, $C_{OX}=8fF/\mu^2$, $\lambda = 0$, $\gamma = 0$, $L_{MIN}=W_{MIN}=0.18\mu$, and $V_{DD}=2V$. $W_{min} = L_{min} = 0.2\ \mu m$

Problem 1:

If a semiconductor process were available with $V_{Tn}= 0.25*V_{DD}$ and $V_{Tp}= -0.1V$, determine R_{pd}, R_{pu}, t_{HL}, t_{LH}, and V_{trip} of a minimum-sized inverter if it is driving a 20 fF load. Assume $\mu_n C_{OX}=350\mu A/v^2$, $\mu_p C_{OX}=70\mu A/v^2$, and $V_{DD}=1.8V$.

Problem 2:

a) In the same semiconductor process described in **Problem 1**, give a sizing strategy needed to place V_{trip} at exactly $V_{DD}/2$.

b) In the same semiconductor process described in **Problem 1**, give a sizing strategy needed to achieve $t_{HL}=t_{LH}$.

Problem 3:

Consider a two-input NOR gate sized for equal worst-case rise and fall times that is driving both input terminals of an identical device.

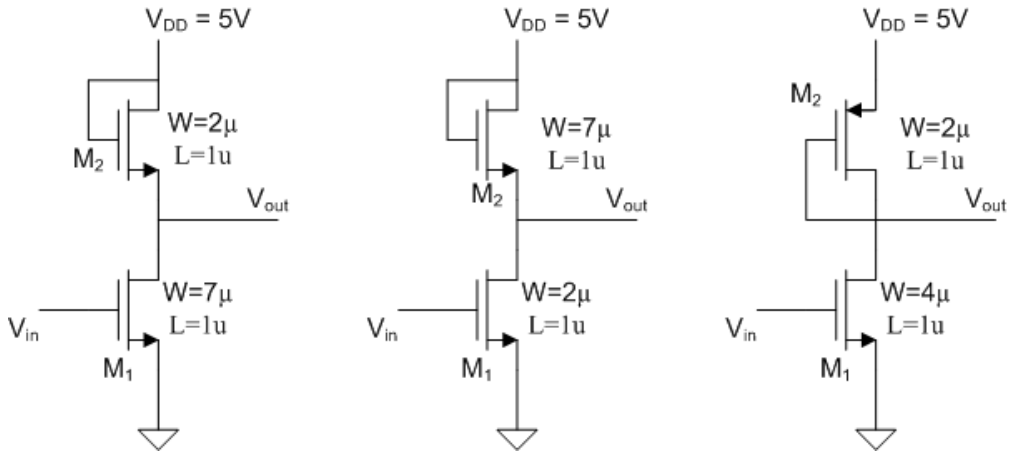
a) Determine sizes of all transistors
b) Determine the fastest and slowest t_{HL} for the output of the first gate in this cascade.

Problem 4:

Size the devices in a 4-input NAND gate for equal worst-case rise and fall times.

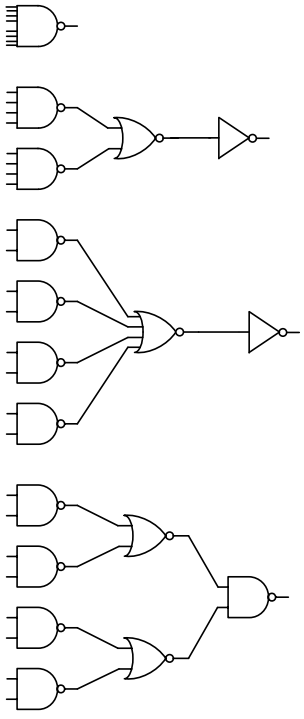
Problem 5:

The circuits shown have been proposed as digital inverters. Determine which will behave as digital inverters and which will not. If the circuit performs as a digital inverter, determine V_H and V_L. Assume the devices are all in the process with μC_{OX}=100 uA/V^2, V_{Tn}=1V, V_{Tp} = -1, γ = 0 and λ=0.



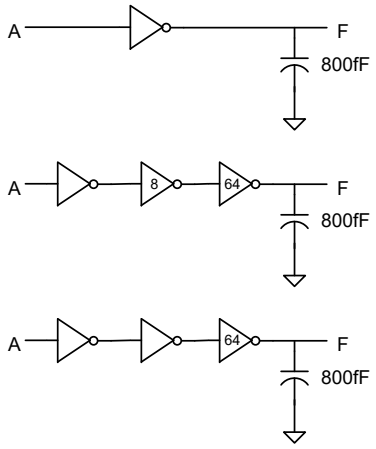
Problem 6:

Four different implementations of the 8-input NAND function are shown. If the devices are sized for equal worst-case rise and fall times, compute the input capacitance at each input and the total area for these 4 different implementations. Assume L = L_{min} for all transistors.



Problem 7:

Three different circuits are shown driving the same load. The overdrive factors if different than 1 are indicated. Quantitatively compare the propagation delay of these circuits. $C_{ref} = 4fF$.

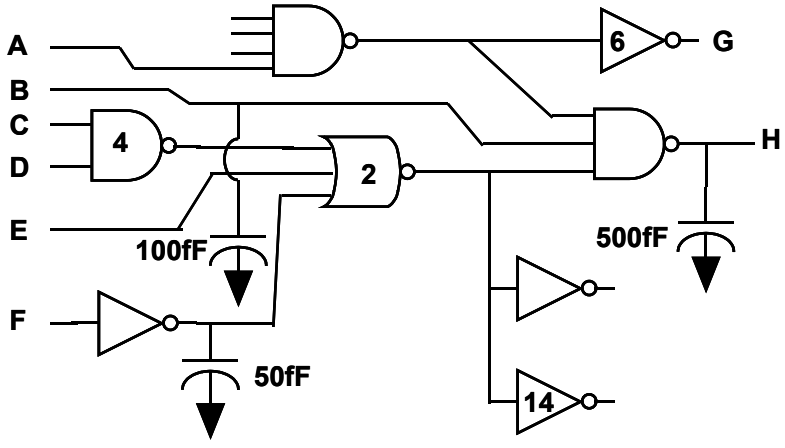


Problem 8:

A logic circuit designed in conventional CMOS is shown. Assume all gates are sized for equal worst-case rise and fall times and that the input capacitance of an equal rise/equal fall reference inverter is 4fF and that it has a propagation delay ($T_{HL} + T_{LH}$) of 20psec. The overdrive factor, if different than 1, is indicated by the number on the gate symbol.

a) Determine the propagation delay ($T_{HL} + T_{LH}$) from the D input to the H output

b) Repeat part a) if all devices are minimum sized (the overdrive factor is no longer germane). Assume the input capacitance to the reference inverter is now 0.8fF.

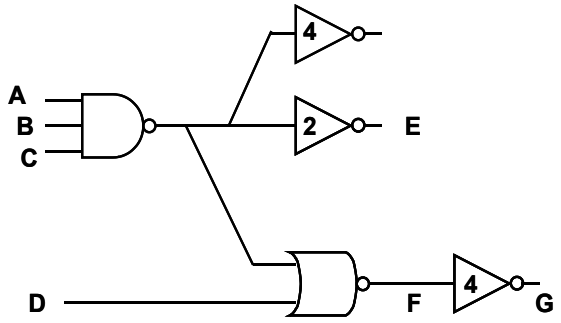


Problem 9:

Assume you are working in a 0.18u CMOS process.

a) Size the devices in the 3-input NAND gate for an overdrive of 4 and the 2-input NOR gate for an overdrive of 6 with the equal rise/fall sizing strategy. The overdrive factors for the inverters are indicated.

b) With this sizing, how does the propagation delay from B to G compare to that of a minimum- sized reference inverter driving an identical path?



Problem 10:

Assume you have need to drive a 500 pF load as fast as possible. Design an output pad driver that drives this load as fast as possible. Assume the input signal that you are directing to the load drives a minimum-sized reference inverter and that your pad driver is attached to the output of this inverter. Assume you are working in the 0.18u TSMC process and that an equal rise and fall time sizing strategy is to be used. C_{ref} = 4fF.