# EE 330 Laboratory 5
# Resistors, Bonding Pads, and Pad Frames

## Contents




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Updated 2/3/2019

## *Objective*

The objective of this experiment is to investigate the design and layout of resistors, the basic bonding pads that comprise a pad frame, and diodes. Then these will be combined into a basic pad protection circuit.

## Part 1: Layout of a resistor

A resistor can be created using almost any layer available in the process. For example, in the TSMC180nm process, a rectangular poly resistor can be created by drawing a rectangular poly region with terminals at its ends as shown in Figure 1. The value of this resistor will be the product of the sheet resistance times the number of squares. (Note: A corner counts as 0.55 squares) The resistor is often shaped to reduce the overall area, often making a U shape or serpentine for larger resistances.

Since a layout pattern with contacts on two ends can be used for either an interconnect or for a resistor, and since the same physical devices are used for both, the CAD tools have no way of determining what is intended to be a resistor that appears in a circuit schematic and what is intended to be an interconnect which shows no resistance in a schematic. To allow the CAD tools to correctly recognize the regions that correspond to resistors in a circuit schematic, an identification cover called *res_id* is added at layout that covers all regions that are to correspond to resistors in the circuit schematic. A *res_id* cover is shown in Figure 1. The *res_id* cover is an identification layer, not an additional physical layer that alters the fabrication process.

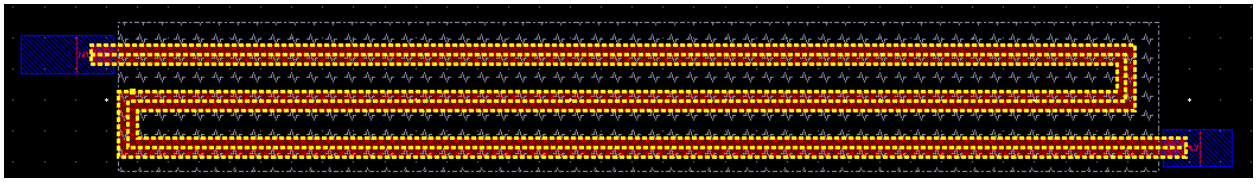

Figure 1

### Part 1.1 Create a resistor layout

Create a resistor of 5 kΩ (+/- 1%) while keeping the diagonal of a bounding rectangle reasonably small using any layer. Use the parameters included in Appendix 1 for this design. Extract the resistor to compare the extracted value with the design value (the extracted view should have a box that says “Res”, when you press Shift+F this will show the resistance value). Do not forget to add the correct via to connect the contacts (the two Metal 1 rectangles in Figure 1) to your resistor.

## Part 2: Introduction to bonding pads

A bonding pad is used as part of the connection of the circuit on a die to a pin on a package. One side of a wire (often gold) connects to the bonding pad while the other side connects to the corresponding pin on a package. This interconnecting wire is called a "bonding wire". Although only the top metal layer (Metal 6 for the TMSC 0.18µ process) is actually used for the connection with the bonding wire, typically the bonding pad is made of all available metal layers stacked on top of each other and interconnected through vias. This arrangement allows connection from the core of the chip to the pad and, in turn, the outside world using any metal layer to interface between the pad and the internal circuit.

The last major processing step in the manufacturing of a wafer is the "passivation" layer (an insulator) that covers the entire chip to protect circuits from environmental contamination or minor damage on the surface. Since the bonding pads need to be accessible for electrical connection to the chip package, this top passivation layer must be removed from the bonding pads. This top passivation layer is termed the *glass* layer. As with all layers in a semiconductor process, the *glass* layer is governed by its own set of design rules (rules 10.x of the MOSIS design rules). Go the Mosis design rules and look at the Overglass section. This should give you a clearer idea of what you are supposed to make.

Note: In the layout the glass layers we create are **anywhere this top passivation layer will be cut** out to allow electrical contact.

### Part 2.1: Create the layout of a bonding pad

**Create a bonding pad** comprised of stacked layers of metal 1-6 with a pad opening in the glass layer. Use stacked vias (stacking of vias is allowed in the TSMC 180nm process) to interconnect these metal layers. To minimize the resistance in the interconnections of these metal layers, use near the maximum possible number of vias, by creating multiple rows and columns, when connecting adjacent metal layers. The pad should be as small as possible while still meeting design rules but the opening in the glass layer is to be 60µm x 60µm and this requirement is important in determining the lower bound for the area of the pad, as the metal of the pad must contain the glass.

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Hint: You can cover the entire surface of a pad with vias efficiently. Use the menu item **Create → Vias** first **Choose Stacked Vias** so you can apply Metal 1-6 vias at the same time and specify the number of **Rows and Columns** of vias you want. You will need to calculate how many rows and columns of vias that you need first.

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## Part 3: Layout of a diode

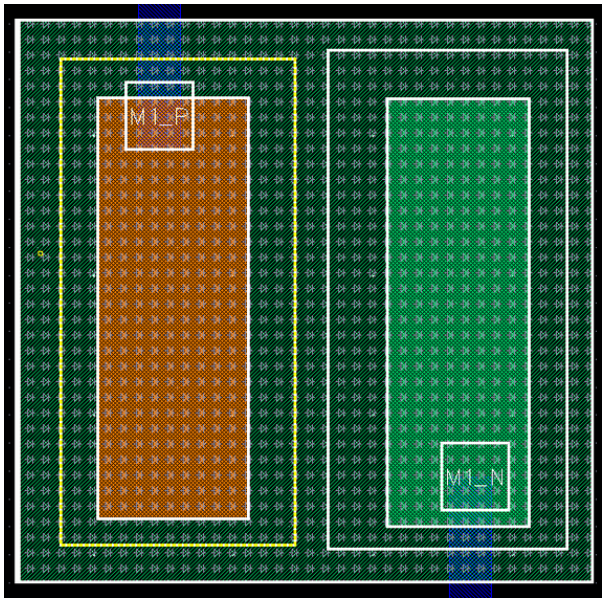


Figure 2

In the n-well bulk CMOS process, diodes can be created in two ways: one is with a p+ diffusion in an n-well and the other is with a n+ diffusions in the substrate. For the purpose of this lab, we will use the p+ diffusion diodes and layout each diode in its own n-well, see Figure 2. However, the anode in the figure is smaller than would be efficient, see Figure 3.

For extraction to work correctly, you must completely cover the diffusions used to form the diodes with the cover layer *dio_id* so that the extraction tool recognizes this as a circuit component.

For this laboratory experiment, the total area occupied by the protection circuit (both diodes and the resistor) will be about equal to the total area you used for the bonding pad itself in Part 2.1. The schematic for the pad and pad protection circuit is shown in Figure 4 on the next page

The resistor can be placed on top of the diodes in the layout. With this in mind, create the layout of one diode in a cell by itself and make sure that it extracts as a diode. This can then be duplicated to form the second diode. Together, they must fit inside the area allocated for the pad protection circuit. We will ignore the electrical properties of the diodes in this experiment and focus only on the correct connectivity.

### Part 3.1 Create a diode layout

**Create the layout for a diode**. Diodes are more efficient the larger their diffusion area. You will want to make your layout about half the area of your bonding pad.

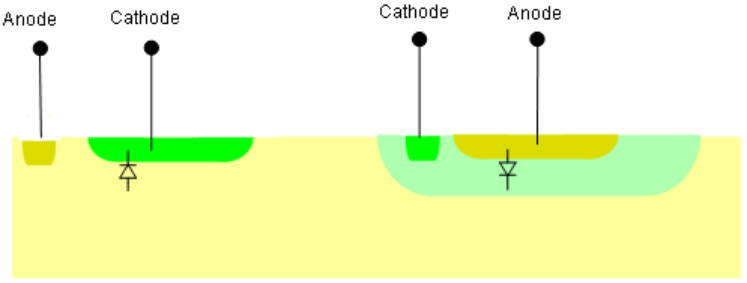


Figure 3

## Part 4: Pad Protection Circuitry

Protecting the circuit from electro-static discharge (ESD) induced damage is crucial. Typically, protection circuitry is designed by engineers specializing in ESD protection and is provided to the circuit designers. For the purpose of this lab, you are going to create a simple protection circuit, not necessarily something that is reliable enough to be used in an actual production circuit, but good enough to introduce the concept of protecting a circuit from ESD damage and good enough to provide some protection from ESD events if included on a fabricated circuit.

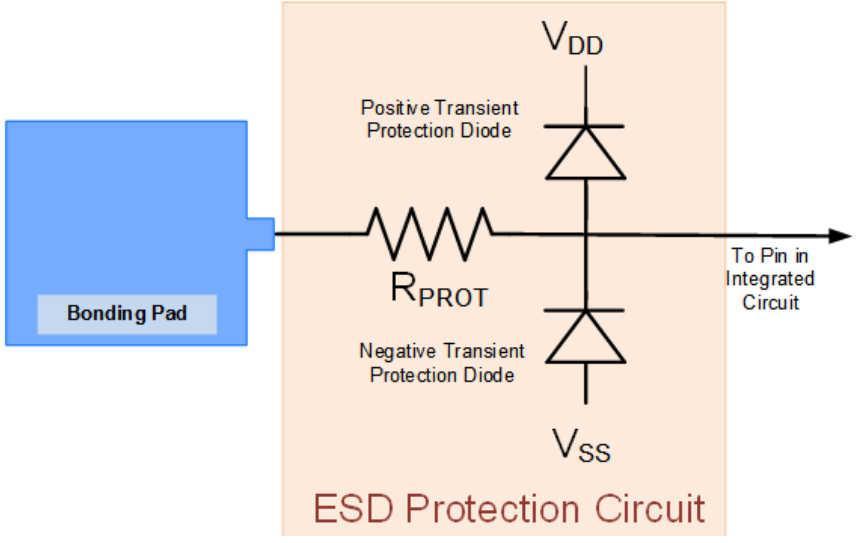


Figure 4

The schematic of a simple protection circuit is shown in figure 4. In this circuit, the diodes protect the chip core from transient voltages on the bonding pad that are beyond the power supply voltages. The resistor is typically made of poly and has a ***value of 50 ohms*** ( you will need to make this in layout) in this protection circuit.

Every pin on the integrated circuit will have a pad protection circuit. Depending upon whether the pin is an input, an output, or a supply voltage, the protection circuit will vary. These variations could be in the size of the resistor, in the size of the diodes, or in some other modifications to the protection circuitry. Pad protection circuits are generally included in a library and the designer simply selects the protection circuit that corresponds to the functionality of each node.

### Part 4.1 Create a Pad Protection Schematic

**Create a new schematic** (call it bondingPadWithESD or something similar) and recreate the schematic of the ESD protection circuit (the Bonding Pad is just an input pin in this schematic). This schematic will be used for LVS later.

## Part 5: Layout of the bonding pad with protection circuit

Create a layout of a bonding pad with ESD protection. Instantiate the needed components in the bonding pad design(we made most of these in other parts of the lab). Make sure your layout pass LVS. A common mistake that causes LVS fail is the direction of the diode. Ensure that the cathode and anode are connected how you expect them to be. Build a symbol for this protection circuitry.

Attempting to run a simulation of this ESD protection will not work. This is because the computer does not have a model for the diodes. You will need to create a diode model that tells the software how to model the diode in the schematic. To do so, go to the folder containing your diode (cd ~/ee330/{lab library}/diode, or something similar) and create a text file called **diode.scs** (gedit diode.scs) and include the following text:

```
simulator lang = spectre

library dio
section d
model diode diode is=1.8e-12 rs=1.43 n=1.22
endsection d
endlibrary dio
```

You will need to add this model to a simulation later.

### Part 5.1: Human Body Model

The human body model is an electrical equivalent of a human touching a circuit to induce static discharge. It is modeled as a 100pF capacitor discharging through a 1500 ohm resistor in series to the device under test (DUT). Devices are qualified into different classes depending upon how much voltage they can handle from this configuration. This of course corresponds to how much static electricity you build up before touching your device! The different classes can be found at the bottom of this page.

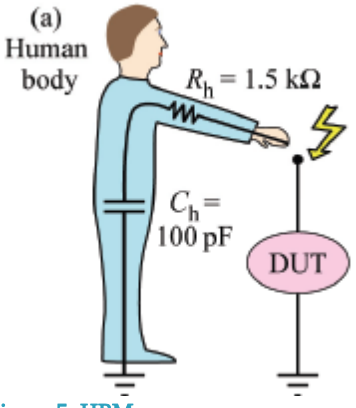


Figure 5: HBM

**Create a new schematic** and call it **HBM_TB**. Add the human body model and your protection circuitry. Remember to hook up Vss and Vdd. Simulate the circuit assuming the output of the protection circuit is loaded with a 1pF capacitor. Set the starting voltage of the charged capacitor using the 'Initial Conditions' query in the properties of the 100pF capacitor. Set the starting voltage of the 1pF load capacitor to 0V.

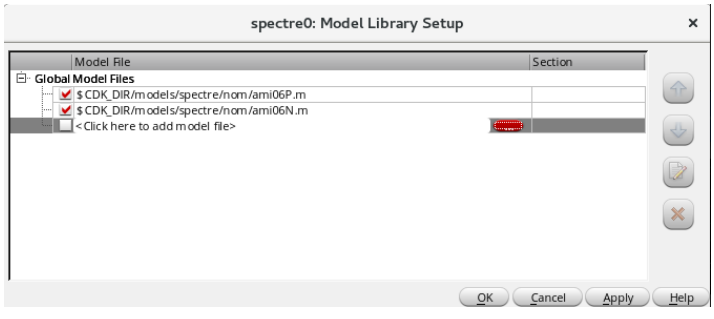


Figure 6

**Before simulating your test circuit, you must include the diode file created earlier in the model.** To do this, open ADE L and go to Setup→Model Libraries and a popup will appear like figure 6. Click on the (…) button to the right of <Click here to add model file> then find your diode.scs file in your file system. Click on the section area to the right of this and a small down arrow will appear. Click on the drop down list and select, "d".

Run the circuit for a variety of starting voltages and see how the protection circuitry works. What is your starting output voltage ? If we specify Vdd = 3.3V and any voltage above 5V destroys the circuitry (a capacitor in this simulation), to what class of devices would this belong? How could you improve the protection of the circuit?

| Class | ESD withstand voltage, $V_w$ |
|---|---|
| 0 | 0 ~ 250 V |
| 1A | 250 ~ 500 V |
| 1B | 500 ~ 1000 V |
| 1C | 1000 ~ 2000 V |
| 2 | 2000 ~ 4000 V |
| 3A | 4000 ~ 8000 V |
| 3B | > 8000 V |

## Part 6: Pad Frames

We could use the pads and pad protection circuit designed above to create a pad frame but for this pad frame, pad protection circuits that have already been made with additional spacing requirements. Details about creating a pad frame using a template from a cell library follow.

A 40-pin pad frame for the TSMC 0.18µ CMOS process is shown in Figure 7. To use this pad frame, it must be added to your Cadence library. Details may be given by your TA, but you will obtain a tar file from either the class website or the shared google drive and extract it similar to how you shared your gates in the previous lab.

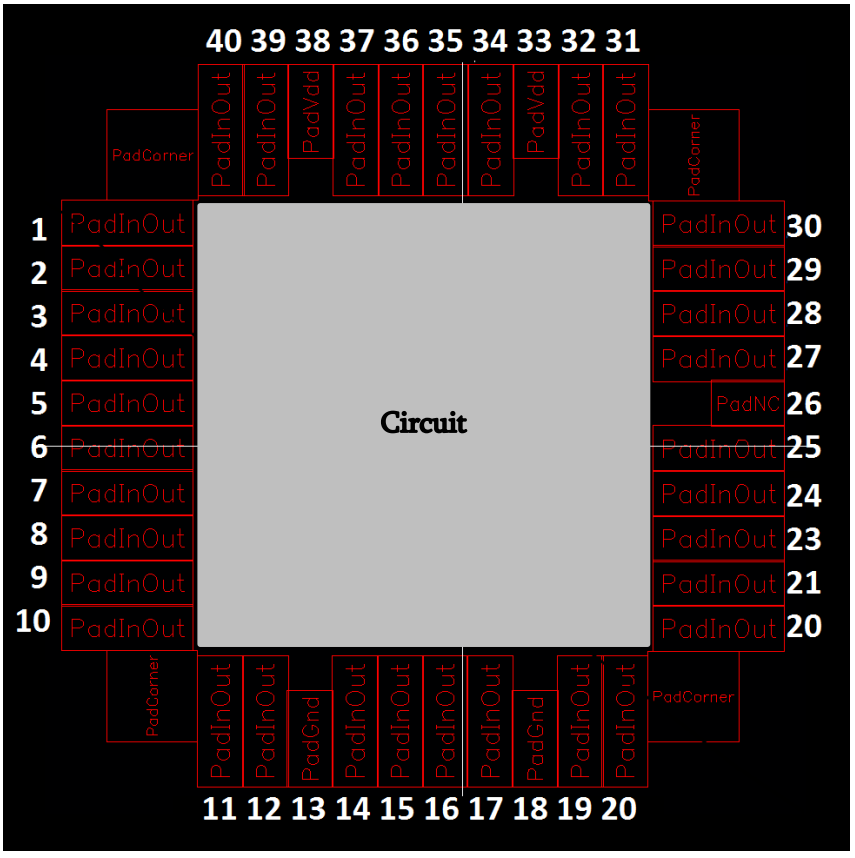


Figure 7

This pad frame has 44 pad cells. The circuit that has been designed will be located in the light-colored region in the interior of the pad frame as indicated. In this pad frame, each of the pad cells has a name/label associated with it. A list of the different pad cells that are available in this pad frame appears in Table 1.

Table 1 Pads available in pad frame of Figure 7.

| Pad cell name | Description | Includes Pad |
|---|---|---|
| PadVdd | Power (Vdd) | Yes |
| PadGnd | Ground (alt Vss) | Yes |
| PadInOut | Analog input/output pad | Yes |
| PadNC | Spacer pad with no connection to bonding pad | Yes[1] |
| PadCorner | Frame Corner | No |
| [1] The pad cannot be used as a bonding pad to make connection to the circuit | | |

The type of pads at any location can be modified simply by selecting the pad (use the outer connection of padframe to select it) going into its properties and changing the instance's "cell" field from one frame to another. For example, if a Vdd connection is desired at one location, the pad cell **PadInOut** can be replaced with the pad cell **PadVdd**. Note that all pad cells except the frame corners, **PadFc** , are identical in size. When using this pad frame, all 44 pad cells must be present and the position of the frame corners must not be altered.

### Connect your Boolean Function to a Pad Frame

Download the ISU_PadFrames_tsmc02.tar.gz file either from the class website or the shared google drive folder. Move it to your ee330 folder and extract it there (this can be done from the command line similar to how you transferred gates last week, or through the GUI). However, note that it end as a folder with the name ISU_PadFrames_tsmc02. Once you have the folder, open your cds.lib file (either from the GUI or with

```
gedit ~/ee330/cds.lib
```

from the command line. Then add the line,

```
DEFINE ISU_PadFrames_tsmc02 ~/ee330/ISU_PadFrames_tsmc02
```

and save the file. When you open up cadence again you should have a library with the pad frame cells.

Because the library was attached through cds.lib it will not have a technology file attached to it. Use the CIW to open the Technology File Manager and attach the NCSU_TechLib_tsmc02 technology file to it.

Create a PAD frame using the 40-pin pad frame template and place the logic circuit you designed in Lab 4 into the pad frame. Place the Boolean inputs A, B, and C, at pads 4, 5 and 6 respectively, connect $V_{DD}$ to Pad 1 and $V_{SS}$ (gnd) to Pad 8. Use Table 1 to determine which type of pad cell is to be used at each location (e.g. use **PadInOut** for Boolean inputs and outputs, **PadVdd** for the $V_{DD}$ supply voltage and pad **PadGnd** for the $V_{SS}$ connection). Use **PadNC** at the remaining 34 locations. No simulation is needed for this part.

## Deliverables:

- Verification sheet
- Introduction:
    - Discuss what is done in lab
    - Discuss why is it useful
- Part 1 – Layout of a Resistor:
    - Screenshot of extracted view with resistor value visible
    - Discuss your layout process. What material you used? How did you come up with design? etc.
- Part 2 – Bonding Connections:
    - Screenshot of bonding pad with relevant measurements showing
    - Explain what are bonding pads and why are they useful
- Part 3 – Layout of Diode:
    - Screenshot of both layout and of extracted view verifying it is a diode
    - Discuss your layout process. What is the diode in your layout? What is the anode ? How does a diode work?
- Part 4 – Pad Protection Circuitry:
    - Screenshots of both schematic and layout
    - Verify that it passes LVS
    - Explain how does this protection circuit work?
- Part 5 – Human Body Model :
    - Screenshot of your test bench and your output waveform
    - Discuss your results. To what class does this protection circuit belong to?
- Part 6 – Pad frames:
    - Screenshots of your circuit connected to pad frame
- Conclusion:
    - Discuss what you learned in lab
    - Add any comments on what you liked or what would you want to see changed

# Appendix 1

MOSIS WAFER ACCEPTANCE TESTS

RUN: T92Y (MM_NON-EPI_THK-MTL) VENDOR: TSMC
TECHNOLOGY: SCN018 FEATURE SIZE: 0.18 microns
Run type: DED

INTRODUCTION: This report contains the lot average results obtained by MOSIS from measurements of MOSIS test structures on each wafer of this fabrication lot. SPICE parameters obtained from similar measurements on a selected wafer are also attached.

COMMENTS: DSCN6M018_TSMC

| TRANSISTOR PARAMETERS | W/L | N-CHANNEL | P-CHANNEL | UNITS |
|---|---|---|---|---|
| MINIMUM | 0.27/0.18 | | | |
| Vth | | 0.50 | -0.49 | volts |
| SHORT | 20.0/0.18 | | | |
| Idss | | 572 | -276 | uA/um |
| Vth | | 0.52 | -0.49 | volts |
| Vpt | | 4.7 | -5.2 | volts |
| WIDE | 20.0/0.18 | | | |
| Ids0 | | 20.8 | -15.2 | pA/um |
| LARGE | 50/50 | | | |
| Vth | | 0.42 | -0.41 | volts |
| Vjbkd | | 3.7 | -4.4 | volts |
| Ijlk | | <50.0 | <50.0 | pA |
| K' (Uo*Cox/2) | | 171.0 | -37.0 | uA/V^2 |
| Low-field Mobility | | 406.07 | 87.86 | cm^2/V*s |

COMMENTS: Poly bias varies with design technology. To account for mask bias use the appropriate value for the parameters XL and XW in your SPICE model card.

| Design Technology | XL (um) | XW (um) |
|---|---|---|
| SCN6M_DEEP (lambda=0.09) | 0.00 | -0.01 |
| thick oxide | 0.00 | -0.01 |
| SCN6M_SUBM (lambda=0.10) | -0.02 | 0.00 |
| thick oxide | -0.02 | 0.00 |

| FOX TRANSISTORS | GATE | N+ACTIVE | P+ACTIVE | UNITS |
|---|---|---|---|---|
| Vth | Poly | >6.6 | <-6.6 | volts |

| PROCESS PARAMETERS | N+ | P+ | POLY | N+BLK | PLY+BLK | M1 | M2 | UNITS |
|---|---|---|---|---|---|---|---|---|
| Sheet Resistance | 7.0 | 8.1 | 8.3 | 59.5 | 306.6 | 0.08 | 0.08 | ohms/sq |
| Contact Resistance | 8.3 | 8.8 | 8.1 | | | | 4.83 | ohms |
| Gate Oxide Thickness | 41 | | | | | | | angstrom |

| PROCESS PARAMETERS | M3 | POLY_HRI | M4 | M5 | M6 | N_W | UNITS |
|---|---|---|---|---|---|---|---|
| Sheet Resistance | 0.08 | | 0.08 | 0.07 | 0.01 | 951 | ohms/sq |
| Contact Resistance | 9.74 | | 15.36 | 21.50 | 23.45 | | ohms |

COMMENTS: BLK is silicide block.

| Capacitance Parameters | N+ | P+ | Poly | M1 | M2 | M3 | M4 | M5 | M6 | R_W | D_N_W | M5P | N_W | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Area (Substrate) | 969 | 1234 | 101 | 34 | 14 | 9 | 7 | 5 | 4 | | 129 | | 130 | aF/um^2 |
| Area (N+ active) | | | 8517 | 53 | 20 | 14 | 11 | 9 | 8 | | | | | aF/um^2 |
| Area (P+ active) | | | 8275 | | | | | | | | | | | aF/um^2 |
| Area (poly) | | | | 64 | 17 | 10 | 7 | 5 | 4 | | | | | aF/um^2 |
| Area (metal1) | | | | | 35 | 14 | 9 | 6 | 5 | | | | | aF/um^2 |
| Area (metal2) | | | | | | 36 | 14 | 9 | 6 | | | | | aF/um^2 |
| Area (metal3) | | | | | | | 37 | 14 | 9 | | | | | aF/um^2 |
| Area (metal4) | | | | | | | | 36 | 14 | | | | | aF/um^2 |
| Area (metal5) | | | | | | | | | 35 | | | | 1039 | aF/um^2 |
| Area (r well) | 953 | | | | | | | | | | | | | aF/um^2 |
| Area (d well) | | | | | | | | | | 562 | | | | aF/um^2 |
| Area (no well) | 140 | | | | | | | | | | | | | aF/um^2 |
| Fringe (Substrate) | 196 | 229 | | 53 | 36 | 29 | 24 | 21 | 19 | | | | | aF/um |
| Fringe (poly) | | | | 68 | 38 | 29 | 23 | 19 | 18 | | | | | aF/um |
| Fringe (metal1) | | | | | 49 | 34 | | 22 | 20 | | | | | aF/um |
| Fringe (metal2) | | | | | | 45 | 35 | 27 | 23 | | | | | aF/um |
| Fringe (metal3) | | | | | | | 54 | 34 | 30 | | | | | aF/um |
| Fringe (metal4) | | | | | | | | 63 | 43 | | | | | aF/um |
| Fringe (metal5) | | | | | | | | | 66 | | | | | aF/um |