EE 330
Lecture 10

IC Fabrication Technology Part III

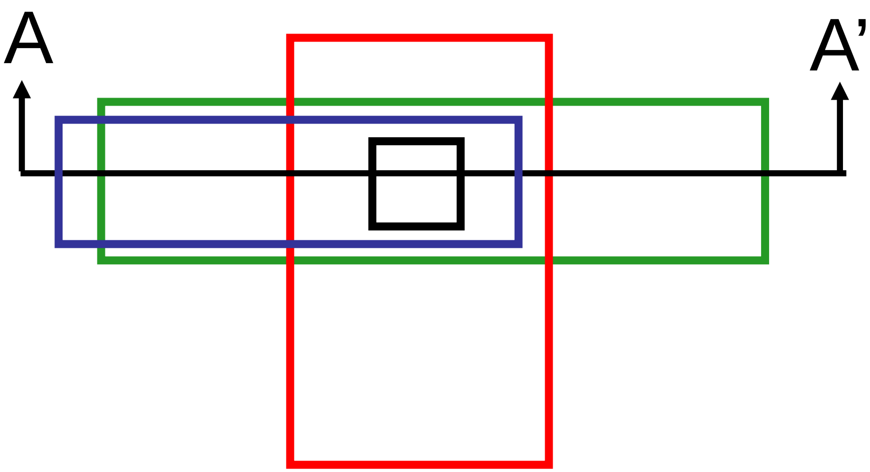
- Metalization and Interconnects
- Parasitic Capacitances
- Back-end Processes

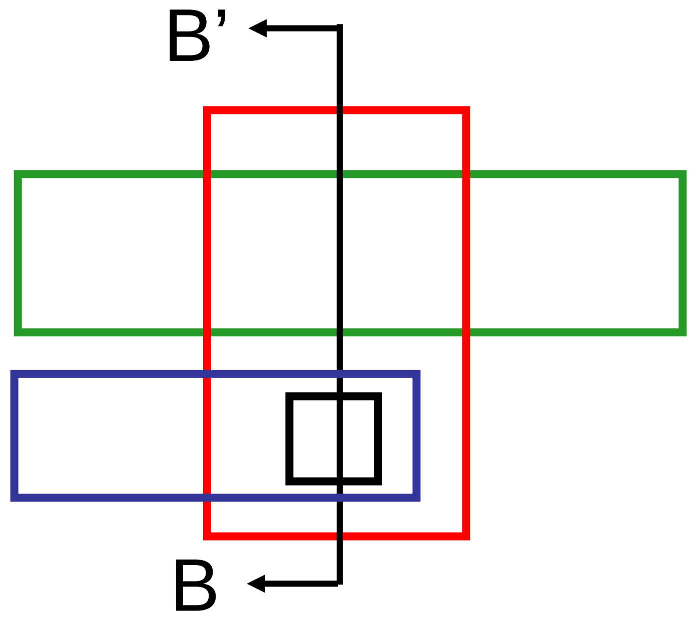
IC Fabrication Technology

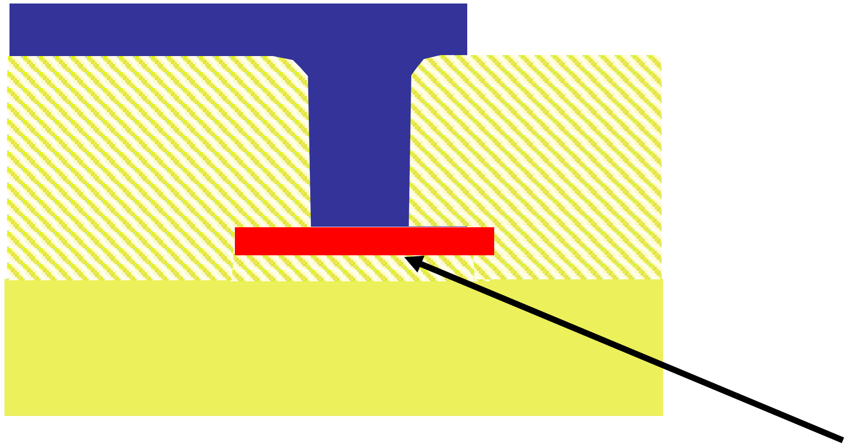
- Crystal Preparation
- Masking
- Photolithographic Process
- Deposition
- Etching
- Diffusion
- Ion Implantation
- Oxidation
- Epitaxy
- Polysilicon
- Planarization
- Contacts, Interconnect and Metalization

Review from Last Lecture

Contacts







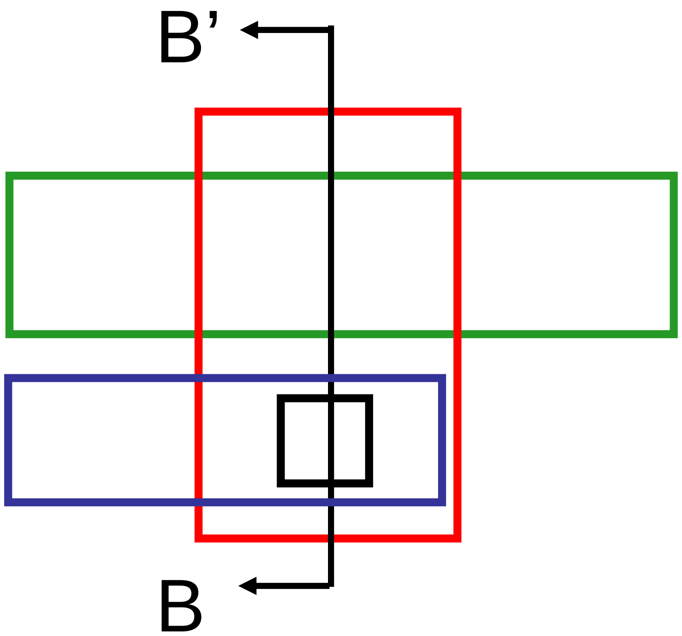
Acceptable Contact

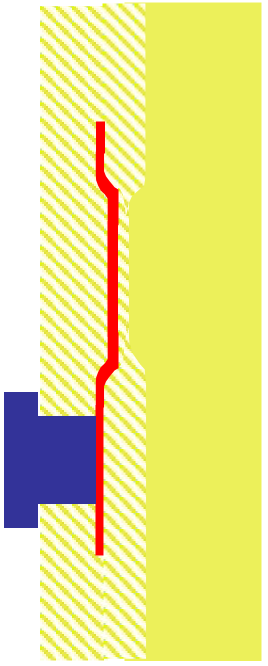
Unacceptable Contact

Vulnerable to pin holes
(usually all contacts are same size)

Review from Last Lecture

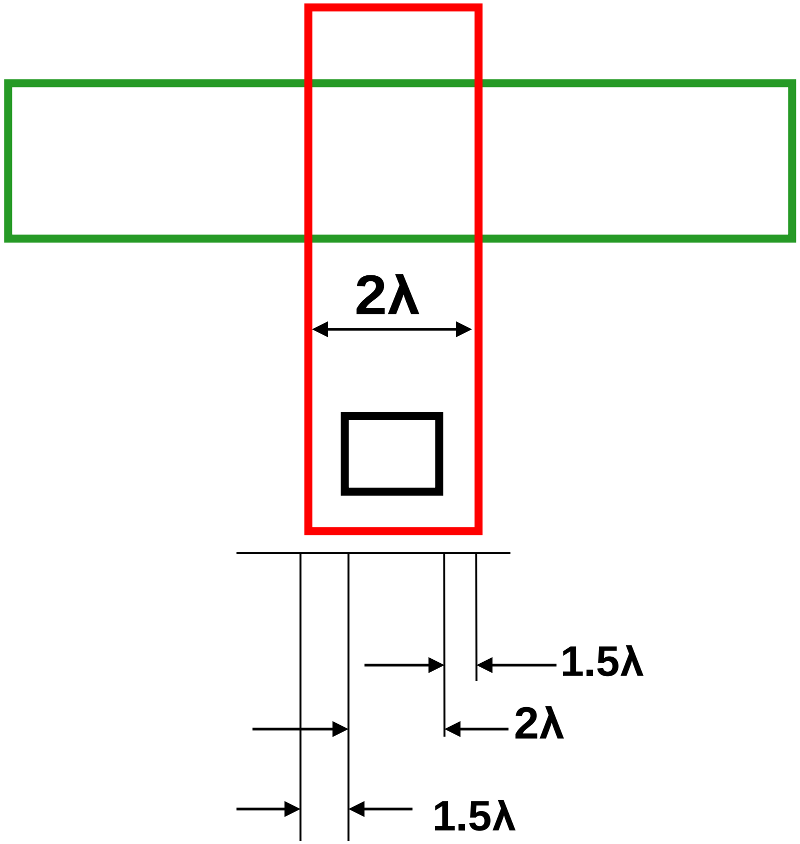
Contacts



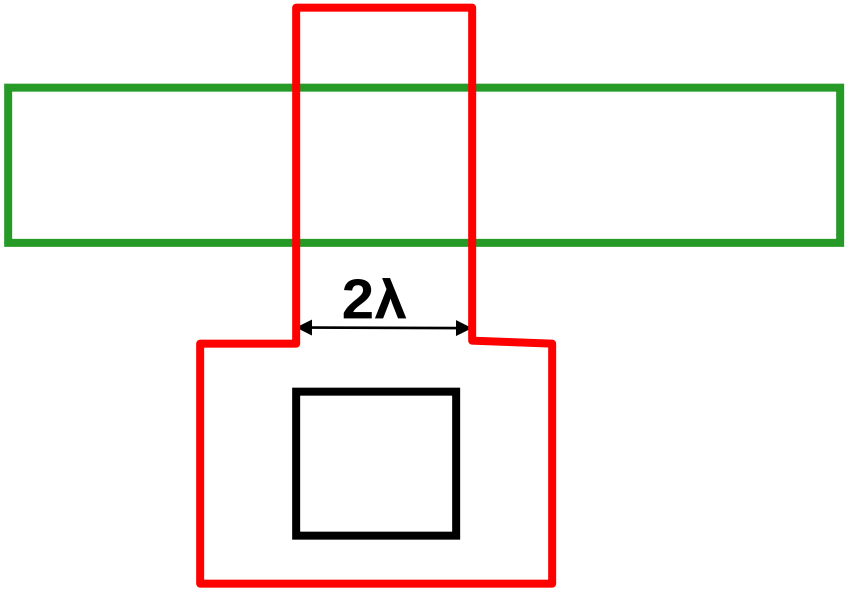


Acceptable Contact

Contacts

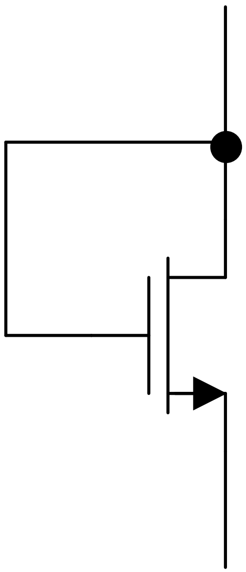


Design Rule Violation

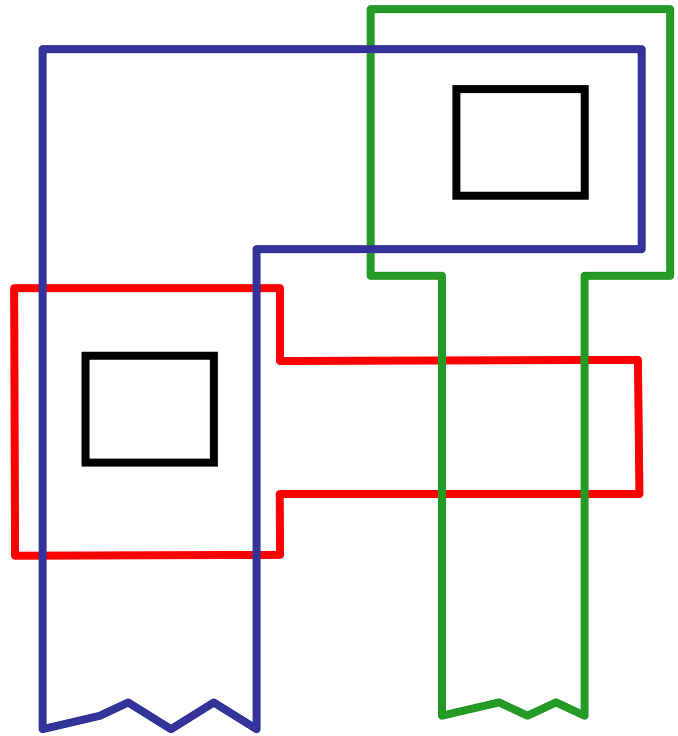


“Dog Bone” Contact

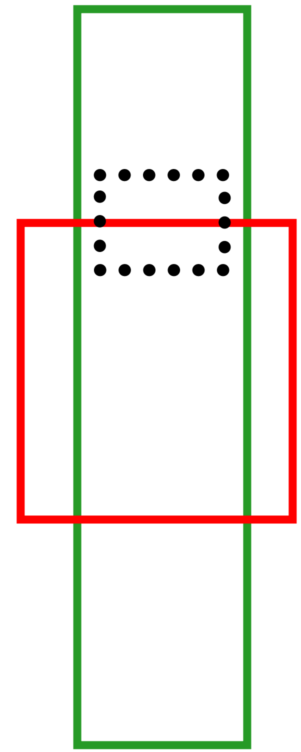
Contacts



Common
Circuit
Connection



Standard Interconnection



Buried Contact

Can save area but not
allowed in many processes

Metalization

- Aluminum widely used for interconnect
- Copper often replacing aluminum in recent processes
- Must not exceed maximum current density
  - around 1ma/u for aluminum and copper
- Ohmic Drop（IR drop）must be managed
- Parasitic Capacitances must be managed
- Interconnects from high to low level metals require connections to each level of metal
- Stacked vias permissible in some processes

Metalization

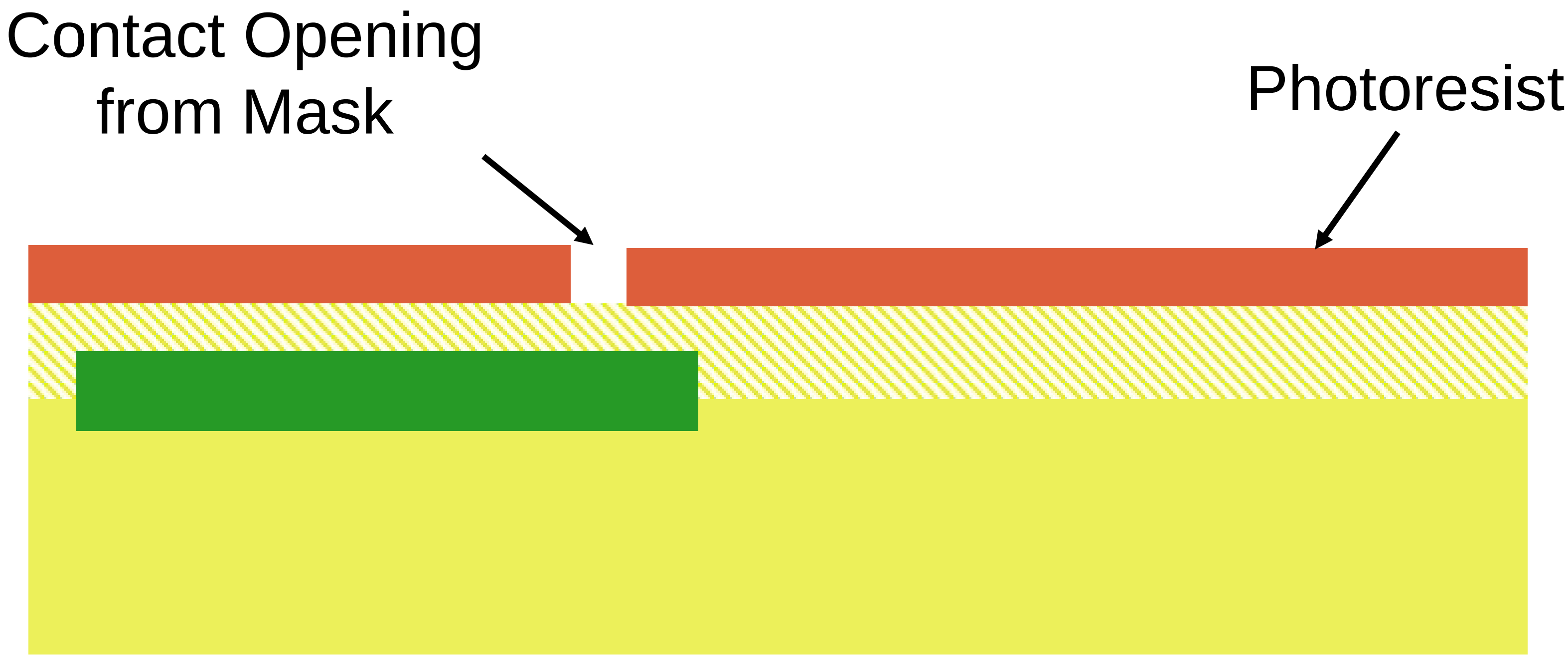
Aluminum

- Aluminum is usually deposited uniformly over entire surface and etched to remove unwanted aluminum
- Mask is used to define area in photoresist where aluminum is to be removed

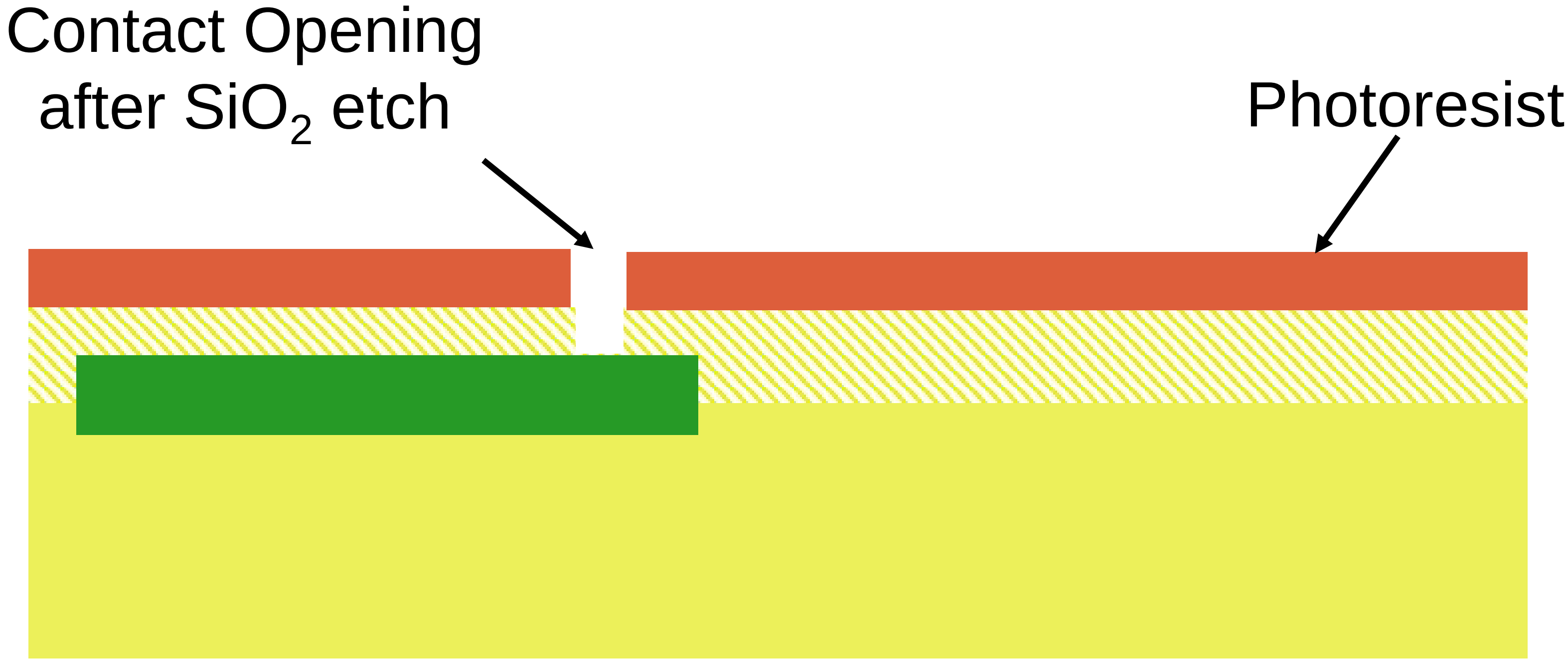
Copper

- Plasma etches not effective at removing copper because of absence of volatile copper compounds
- Barrier metal layers needed to isolate silicon from migration of copper atoms
- Damascene or Dual-Damascene processes used to pattern copper

Patterning of Aluminum

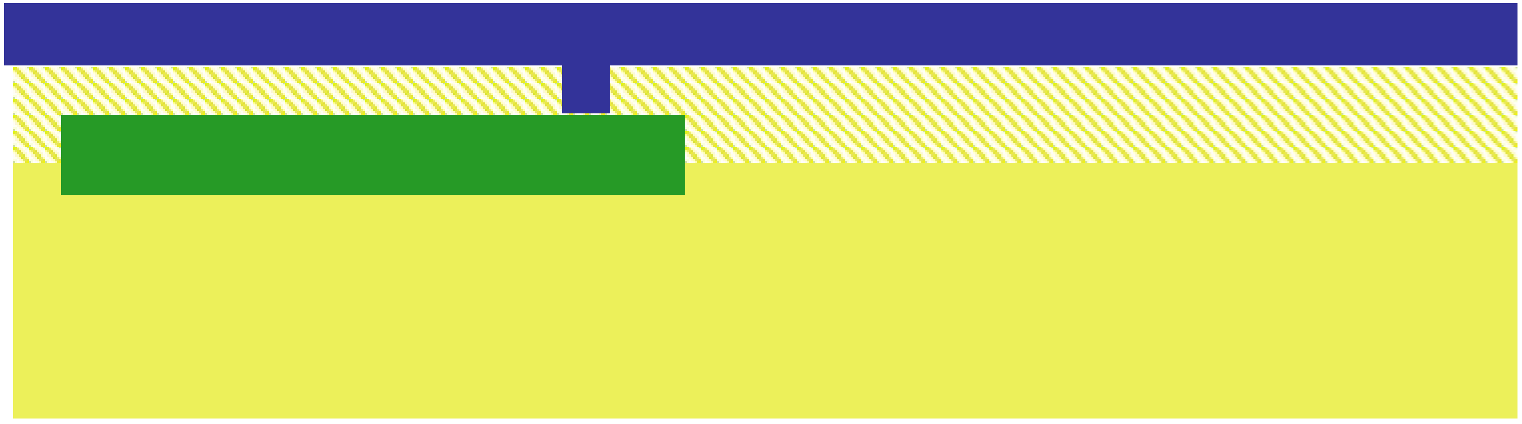


Patterning of Aluminum

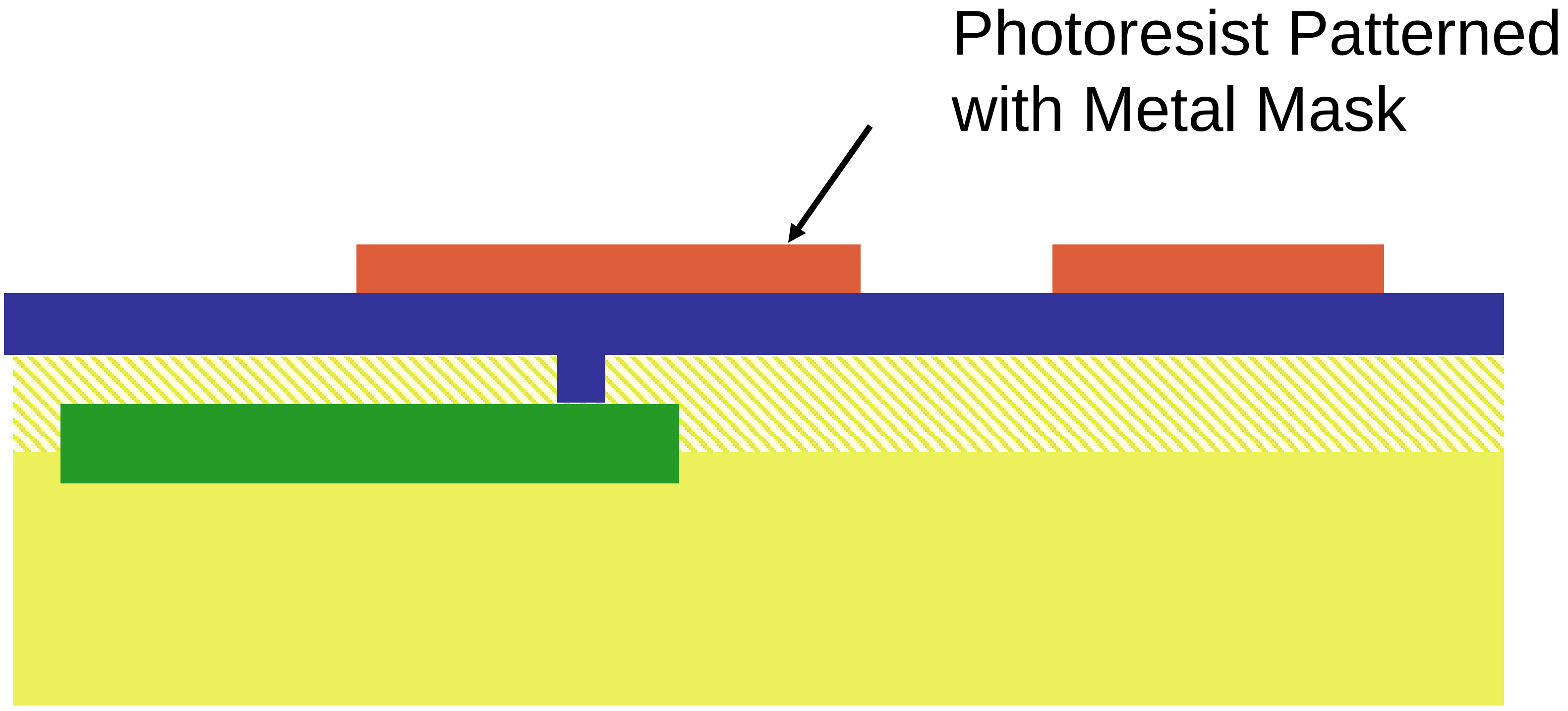


Patterning of Aluminum

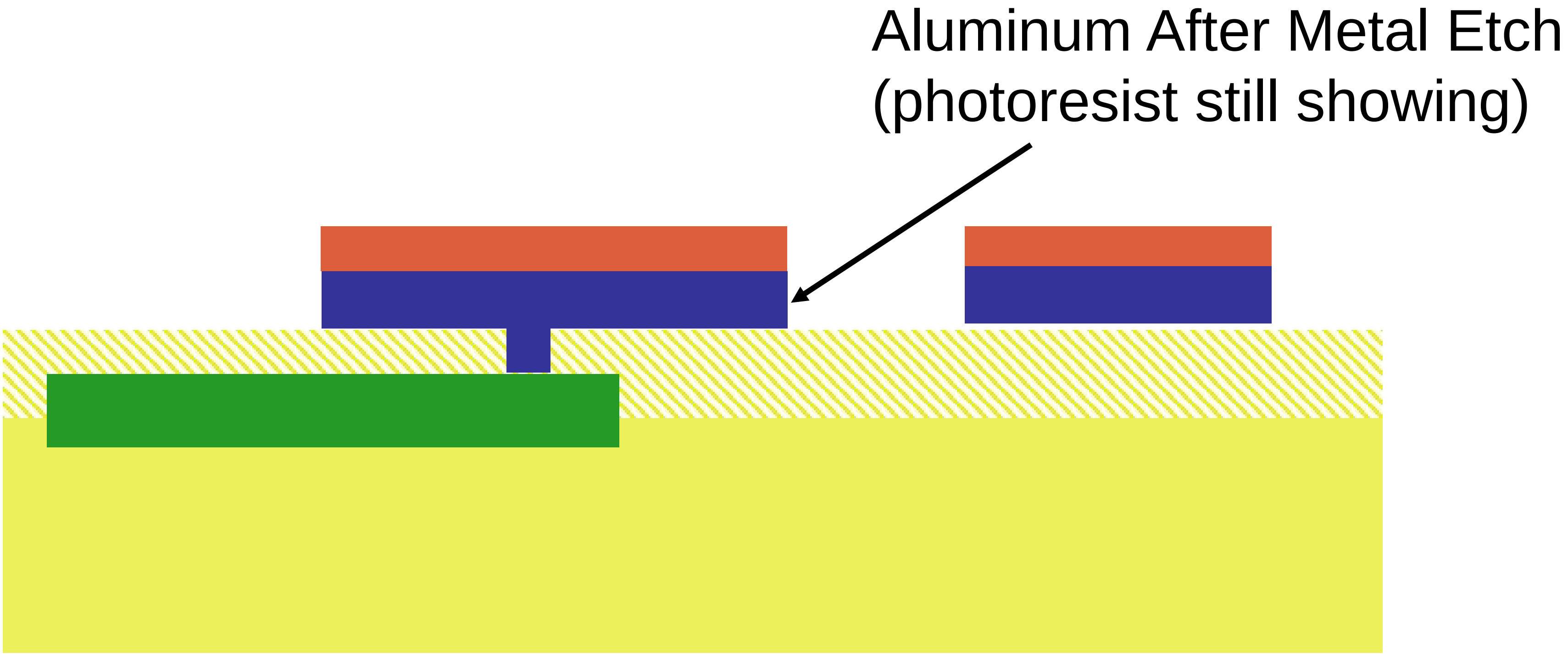
Metal Applied to Entire Surface



Patterning of Aluminum



Patterning of Aluminum



Copper Interconnects

Limitations of Aluminum Interconnects

- Electromigration
- Conductivity not real high

Relevant Key Properties of Copper

- Reduced electromigration problems at given current level
- Better conductivity

Challenges of Copper Interconnects

- Absence of volatile copper compounds (does not etch)
- Copper diffuses into surrounding materials (barrier metal required)

Material	ρ (Ω·m) at 20 °C	σ (S/m) at 20 °C	Temperat coefficient[(K^{-1})
Carbon (graphene)	1.00×10^{-8}	1.00×10^{8}	−0.0002
Silver	1.59×10^{-8}	6.30×10^{7}	0.0038
Copper	1.68×10^{-8}	5.96×10^{7}	0.003862
Annealed copper[note 2]	1.72×10^{-8}	5.80×10^{7}	0.00393
Gold[note 3]	2.44×10^{-8}	4.10×10^{7}	0.0034
Aluminium[note 4]	2.82×10^{-8}	3.50×10^{7}	0.0039
Calcium	3.36×10^{-8}	2.98×10^{7}	0.0041
Tungsten	5.60×10^{-8}	1.79×10^{7}	0.0045
Zinc	5.90×10^{-8}	1.69×10^{7}	0.0037
Nickel	6.99×10^{-8}	1.43×10^{7}	0.006
Lithium	9.28×10^{-8}	1.08×10^{7}	0.006
Iron	9.71×10^{-8}	1.00×10^{7}	0.005
Platinum	1.06×10^{-7}	9.43×10^{6}	0.00392
Tin	1.09×10^{-7}	9.17×10^{6}	0.0045
Carbon steel (1010)	1.43×10^{-7}	6.99×10^{6}	

Source:
Sept 13, 2017

Lead	2.20×10^{-7}	4.55×10^{6}	0.0039
Titanium	4.20×10^{-7}	2.38×10^{6}	0.0038
Grain oriented electrical steel	4.60×10^{-7}	2.17×10^{6}	
Manganin	4.82×10^{-7}	2.07×10^{6}	0.000002
Constantan	4.90×10^{-7}	2.04×10^{6}	0.000008
Stainless steel[note 5]	6.90×10^{-7}	1.45×10^{6}	0.00094
Mercury	9.80×10^{-7}	1.02×10^{6}	0.0009
Nichrome[note 6]	1.10×10^{-6}	6.7×10^{5}	0.0004
GaAs	1.00×10^{-3} to 1.00×10^{8}	1.00×10^{-8} to 10^{3}	
Carbon (amorphous)	5.00×10^{-4} to 8.00×10^{-4}	1.25×10^{3} to 2×10^{3}	−0.0005
Carbon (graphite)[note 7]	2.50×10^{-6} to 5.00×10^{-6} ∥basal plane 3.00×10^{-3} ⊥basal plane	2.00×10^{5} to 3.00×10^{5} ∥basal plane 3.30×10^{2} ⊥basal plane	
PEDOT:PSS	2×10^{-6} to 1×10^{-1}	1×10^{1} to 4.6×10^{5}	?
Germanium[note 8]	4.60×10^{-1}	2.17	−0.048
Sea water[note 9]	2.00×10^{-1}	4.80	
Swimming pool water[note 10]	3.33×10^{-1} to 4.00×10^{-1}	0.25 to 0.30	

Silicon[note 8]	6.40×10^{2}	1.56×10^{-3}	−0.075
Wood (damp)	1.00×10^{3} to 1.00×10^{4}	10^{-4} to 10^{-3}	
Deionized water[note 12]	1.80×10^{5}	5.50×10^{-6}	
Glass	1.00×10^{11} to 1.00×10^{15}	10^{-15} to 10^{-11}	?
Hard rubber	1.00×10^{13}	10^{-14}	?
Wood (oven dry)	1.00×10^{14} to 1.00×10^{16}	10^{-16} to 10^{-14}	
Sulfur	1.00×10^{15}	10^{-16}	?
Air	1.30×10^{14} to 3.30×10^{14}	3×10^{-15} to 8×10^{-15}	
Carbon (diamond)	1.00×10^{12}	$\sim 10^{-13}$	
Fused quartz	7.50×10^{17}	1.30×10^{-18}	?
PET	1.00×10^{21}	10^{-21}	?
Teflon	1.00×10^{23} to 1.00×10^{25}	10^{-25} to 10^{-23}	?

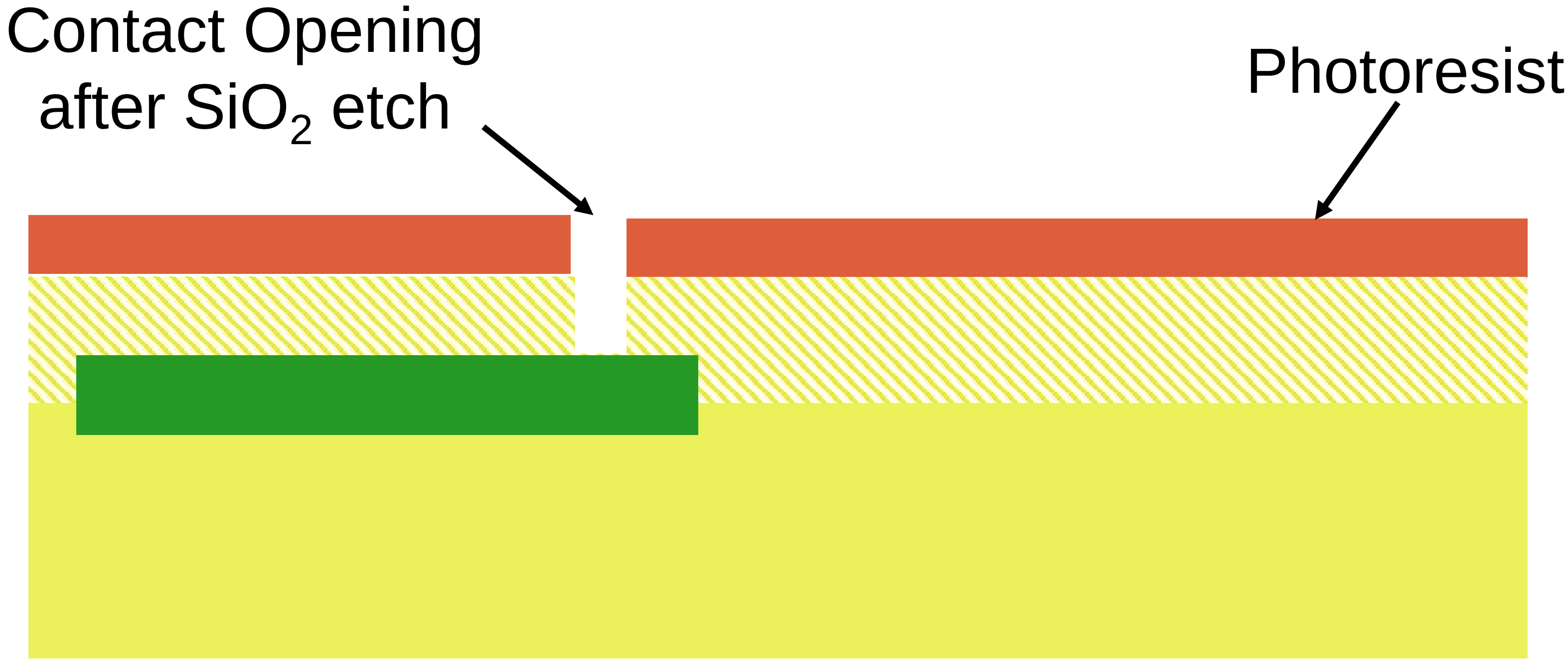
Copper Interconnects

Practical methods of realizing copper interconnects took many years to develop

Copper interconnects widely used in some processes today

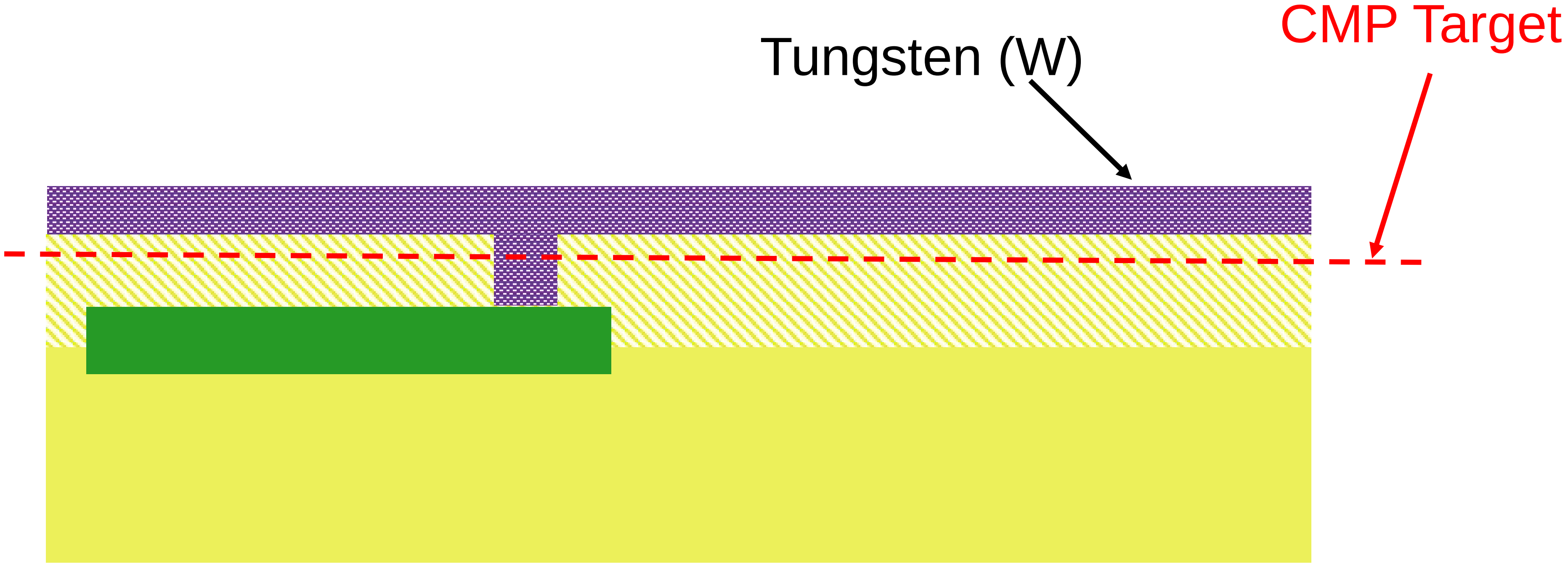
Patterning of Copper

Damascene Process



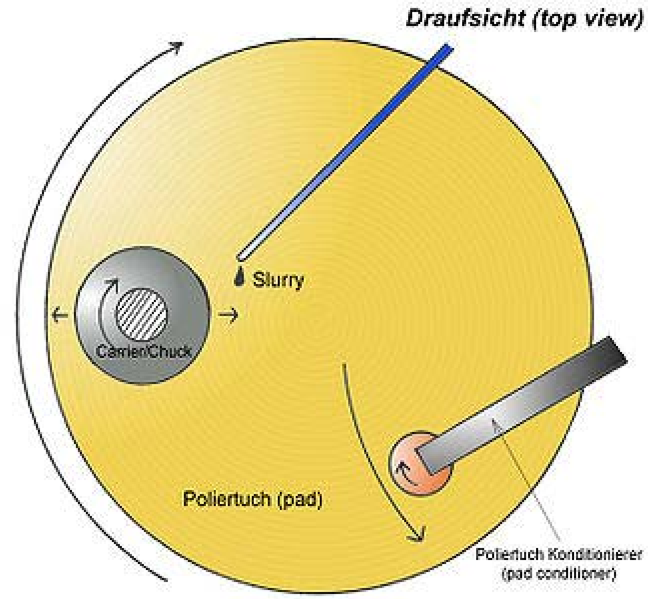
Patterning of Copper

Damascene Process

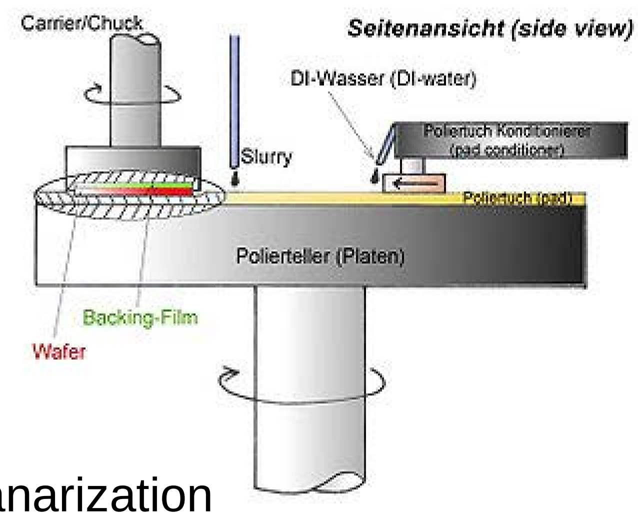


W has excellent conformality when formed from WF6

Chemical-Mechanical Planarization (CMP)



- Polishing Pad and Wafer Rotate in non-concentric pattern to thin, polish, and planarize surface
- Abrasive/Chemical polishing
- Depth and planarity are critical

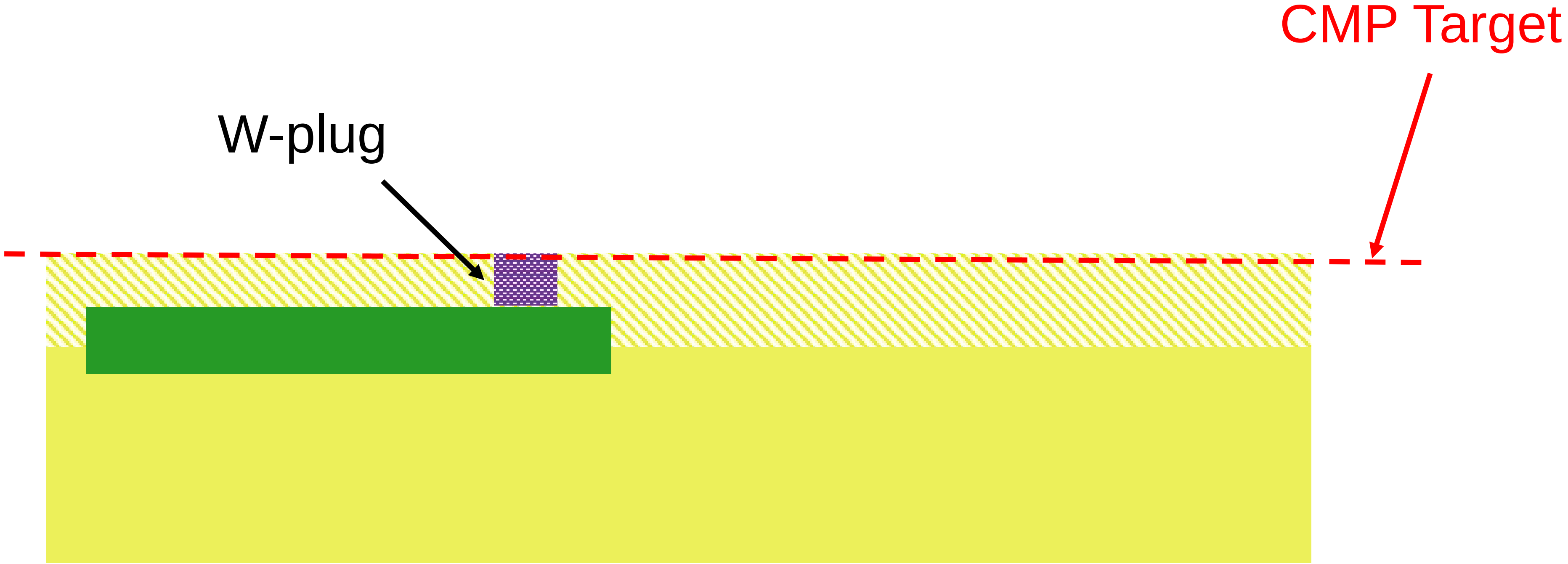


Acknowledgement:
http://en.wikipedia.org/wiki/Chemical-mechanical_planarization

Patterning of Copper

Damascene Process

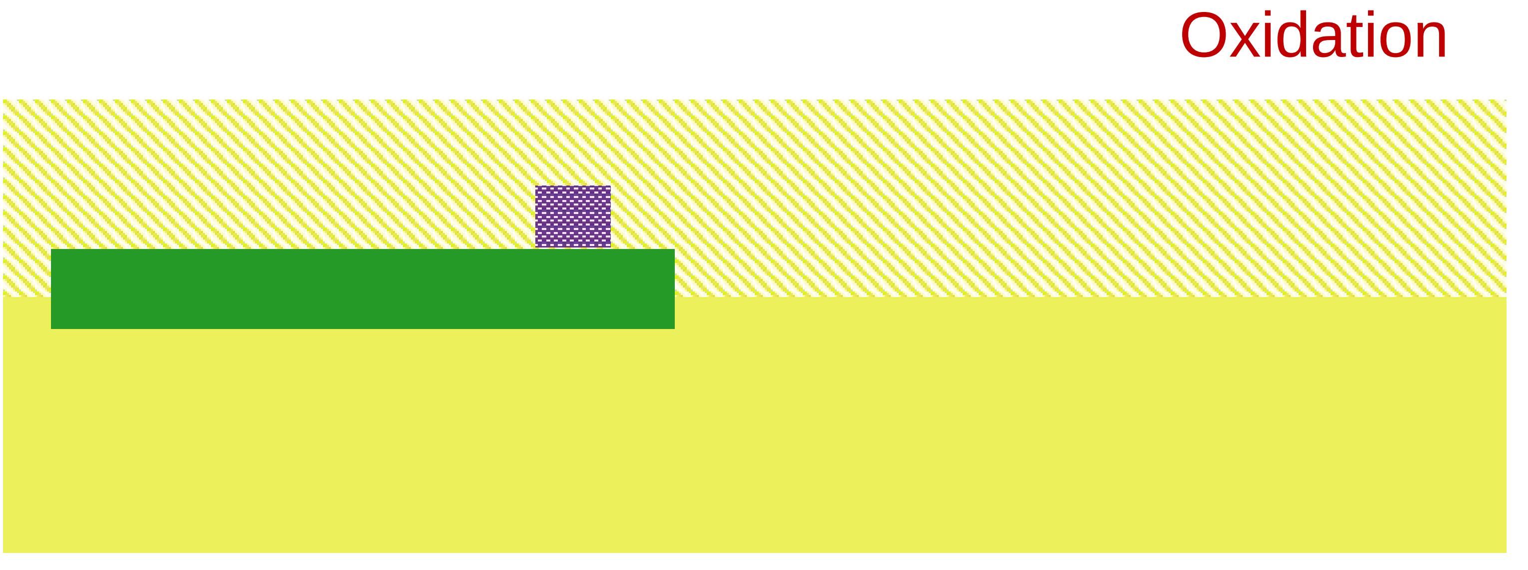
After first CMP Step



Patterning of Copper

Damascene Process

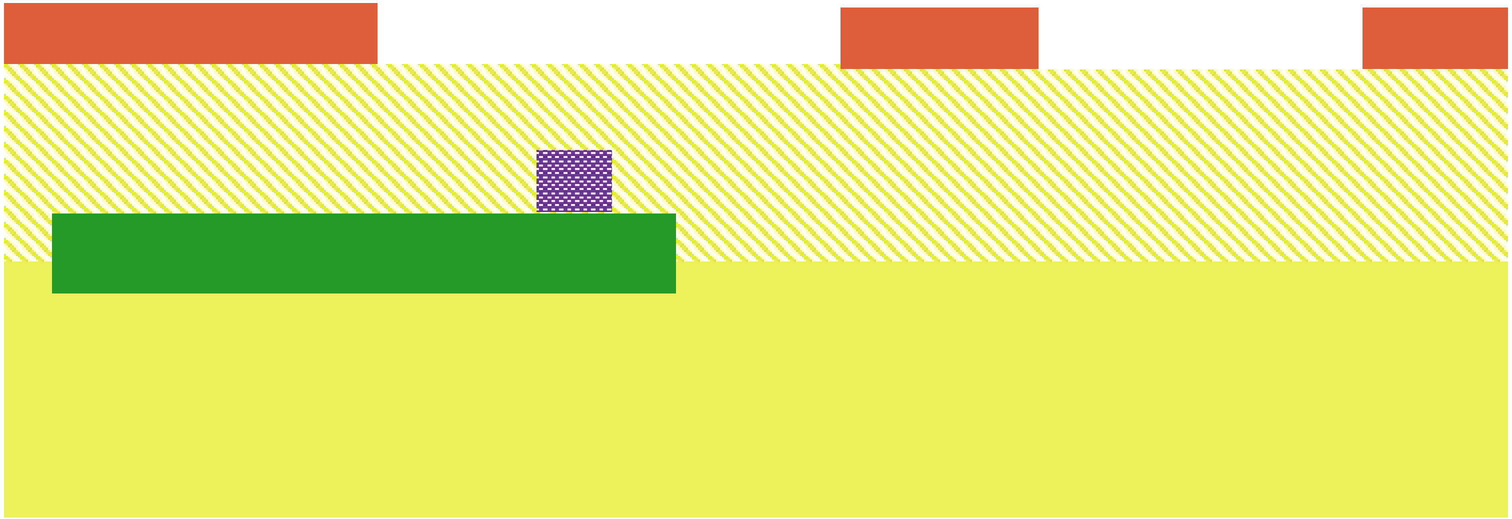
After first CMP Step



Patterning of Copper

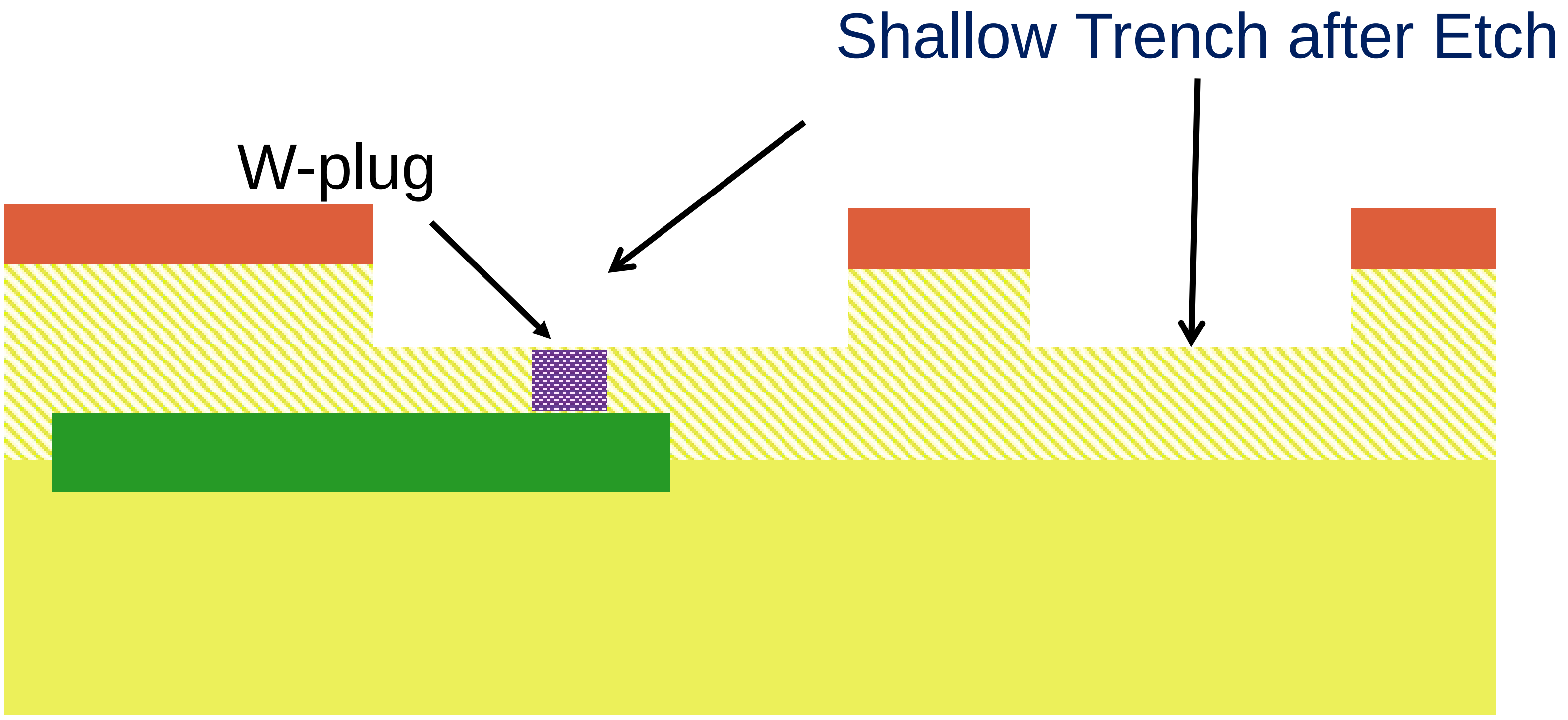
Damascene Process

Photoresist Patterned with
Metal Mask Defines Trench



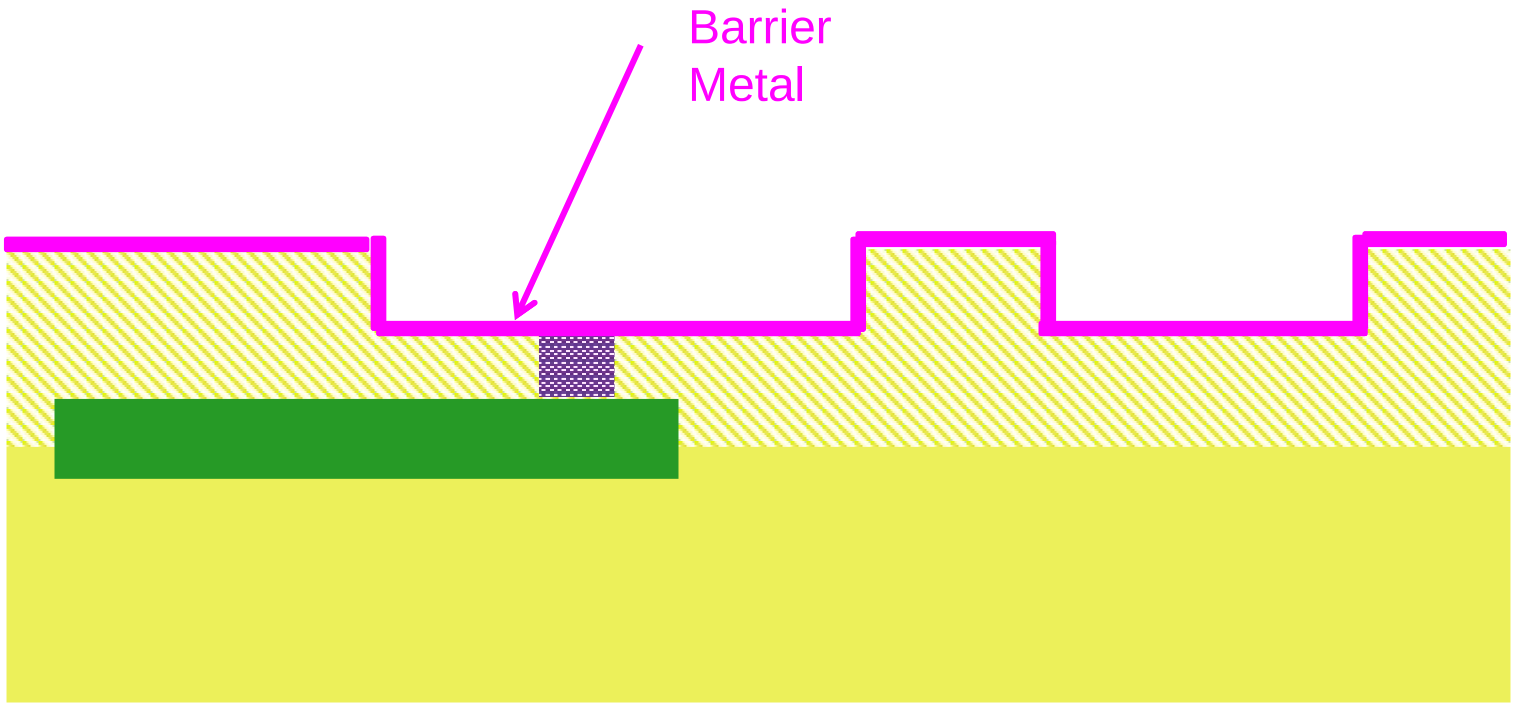
Patterning of Copper

Damascene Process



Patterning of Copper

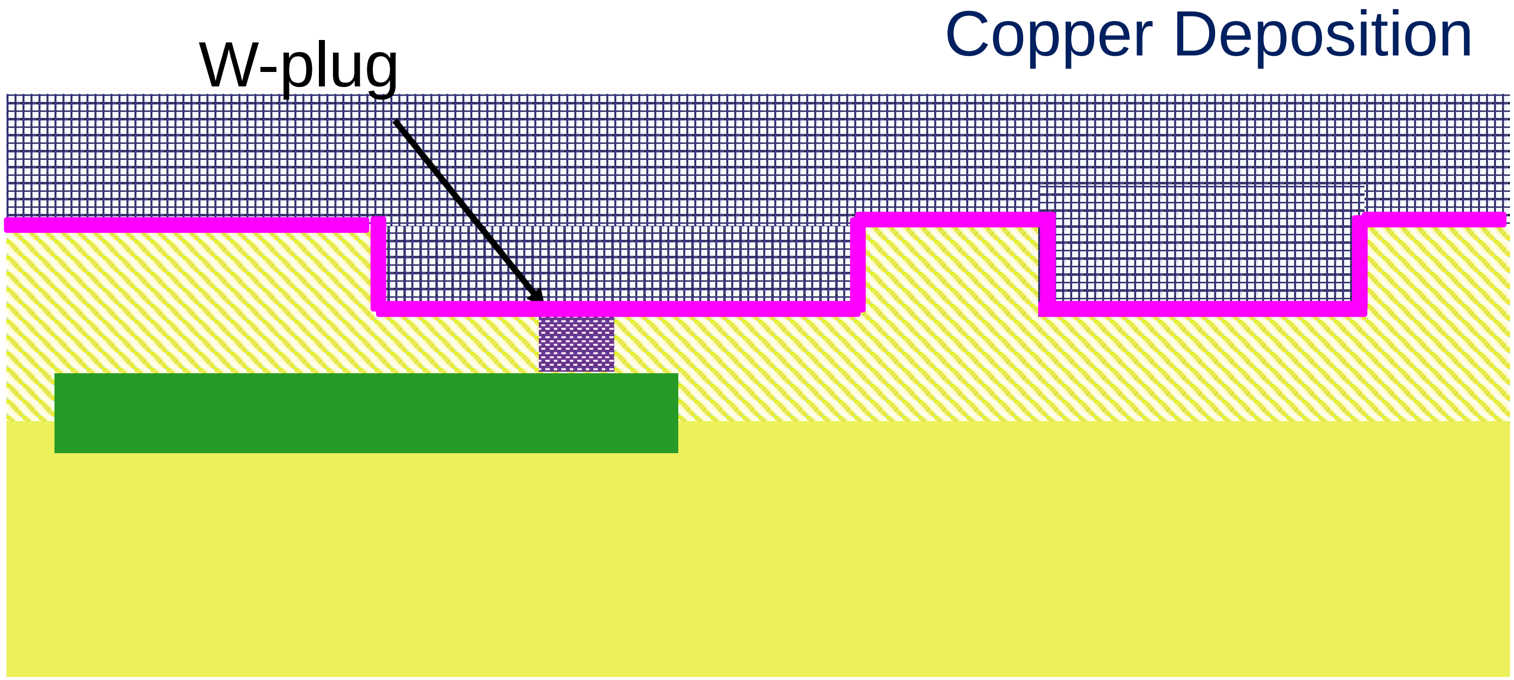
Damascene Process



(Barrier metal added before copper to contain the copper atoms)

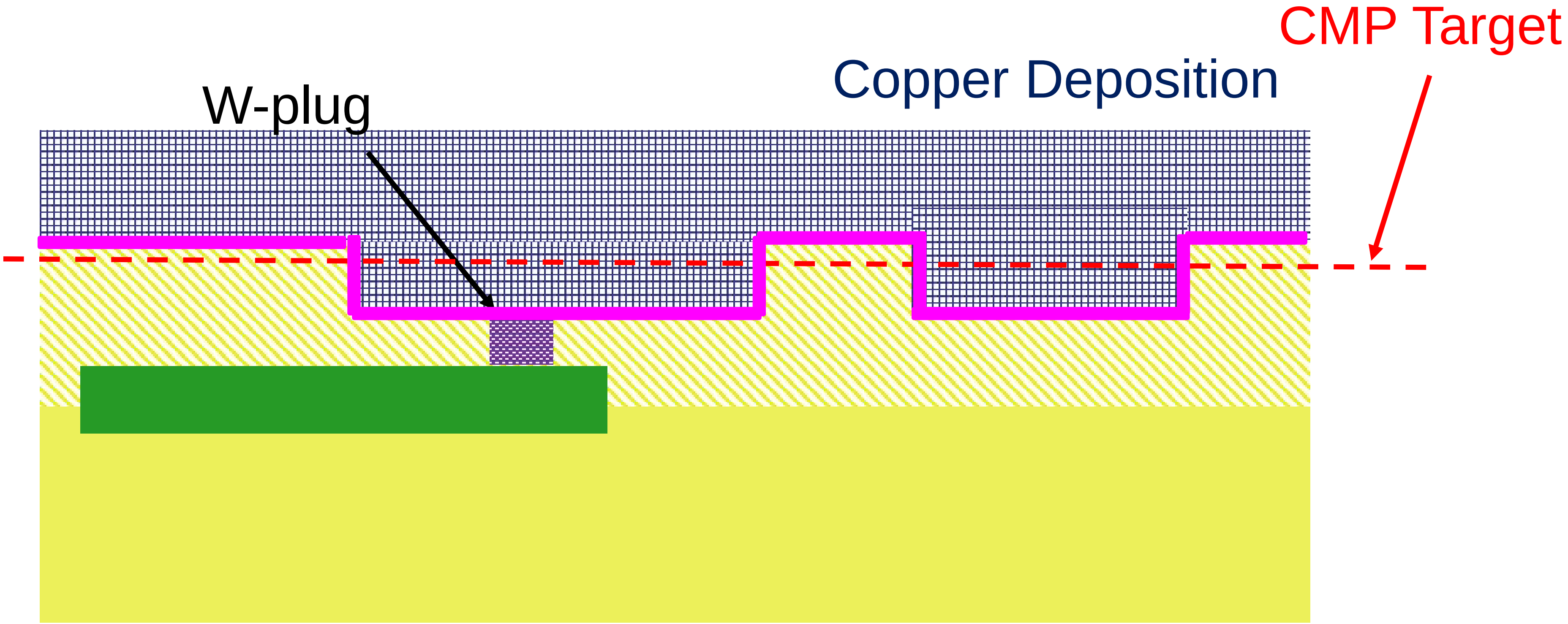
Patterning of Copper

Damascene Process



Patterning of Copper

Damascene Process

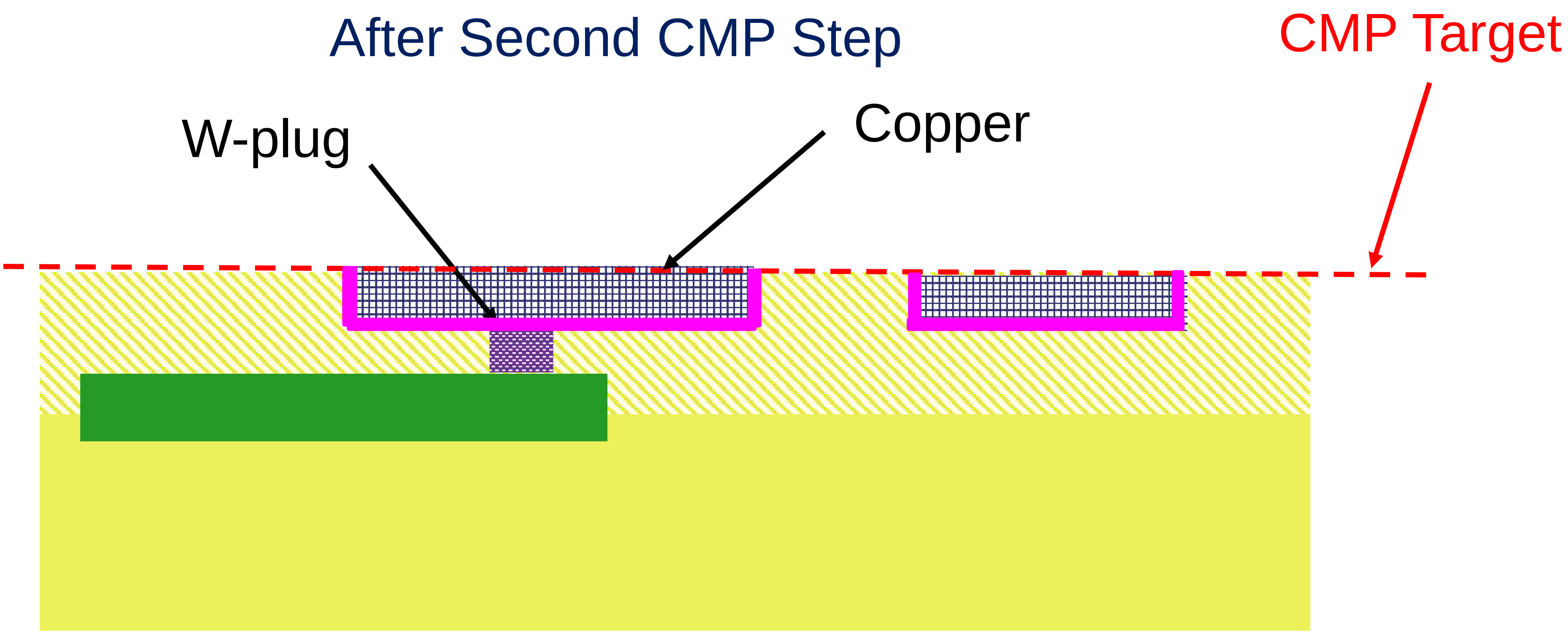


Copper is deposited or electroplated (Barrier Metal Used for Electroplating Seed)

Patterning of Copper

Damascene Process

After Second CMP Step

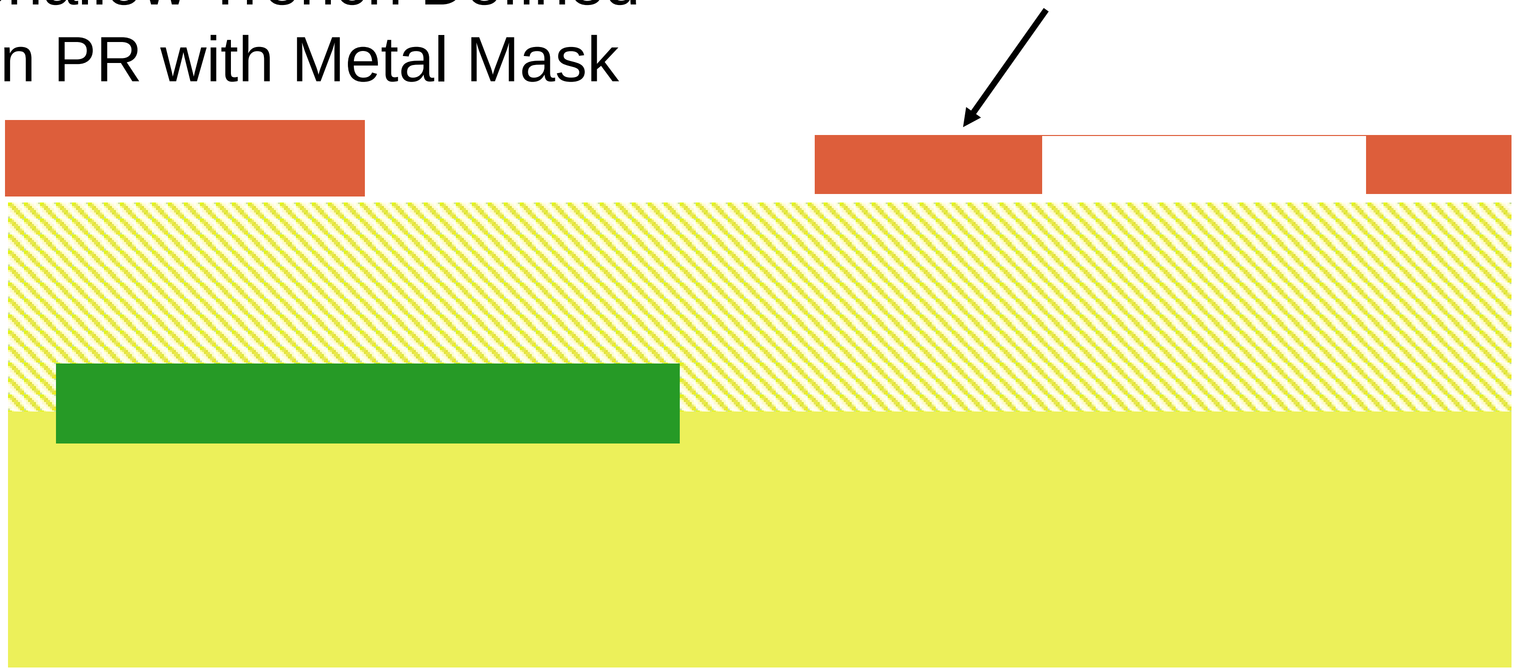


Patterning of Copper

Dual-Damascene Process

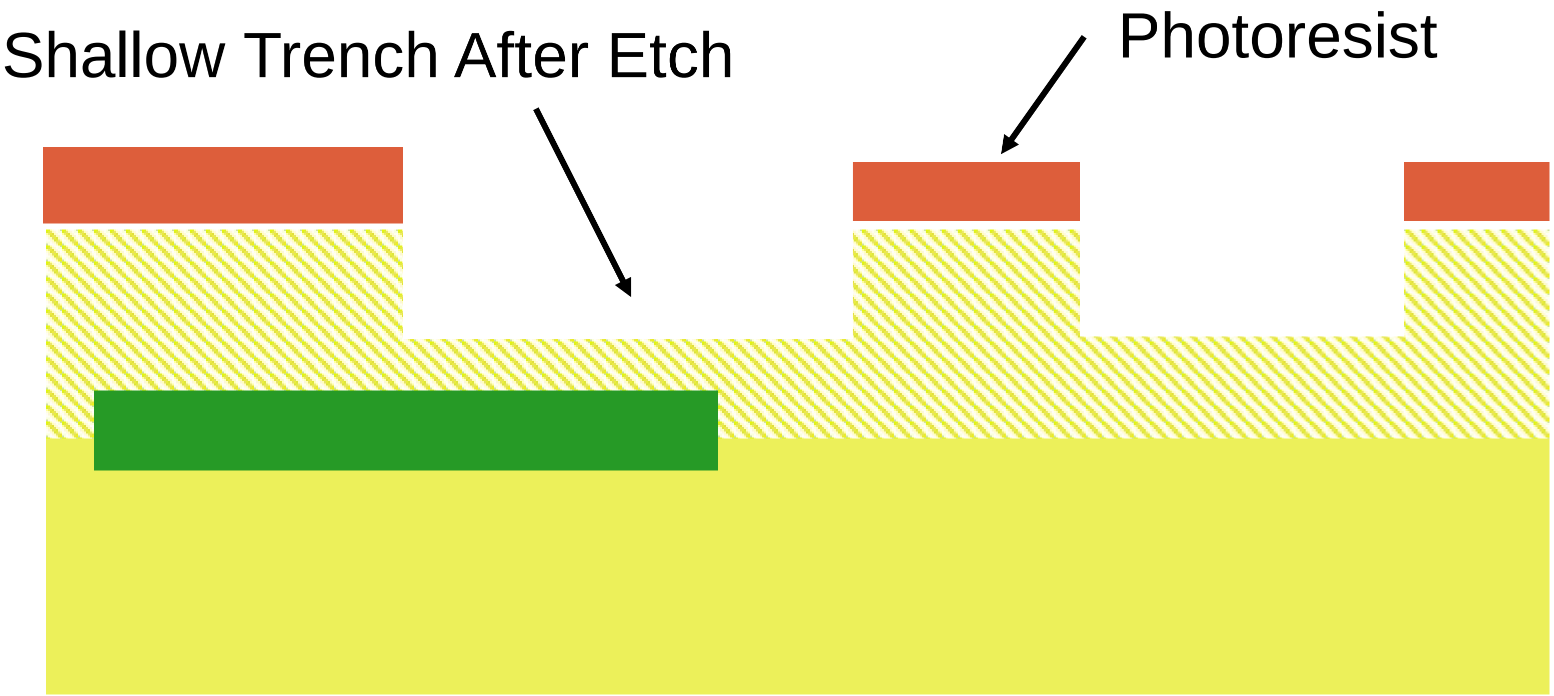
Shallow Trench Defined
in PR with Metal Mask

Photoresist



Patterning of Copper

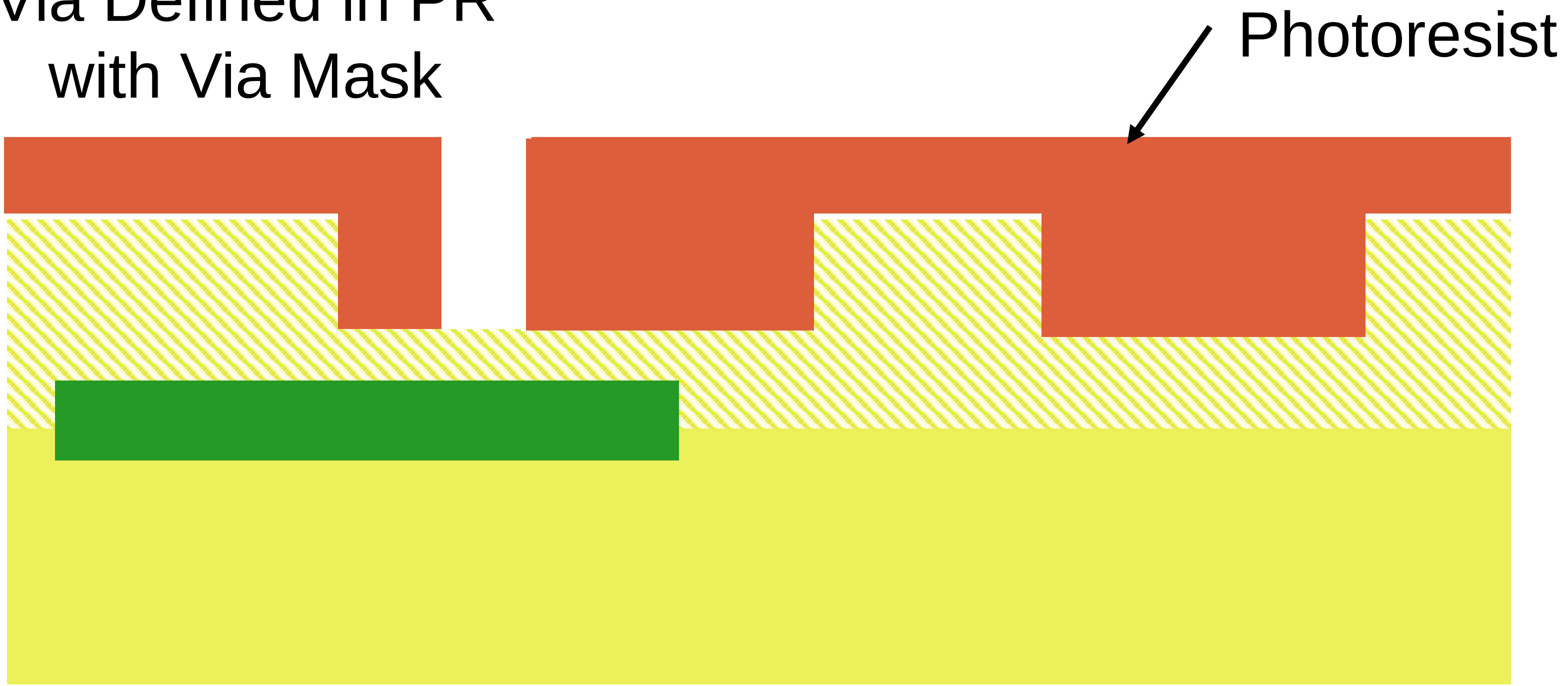
Dual-Damascene Process



Patterning of Copper

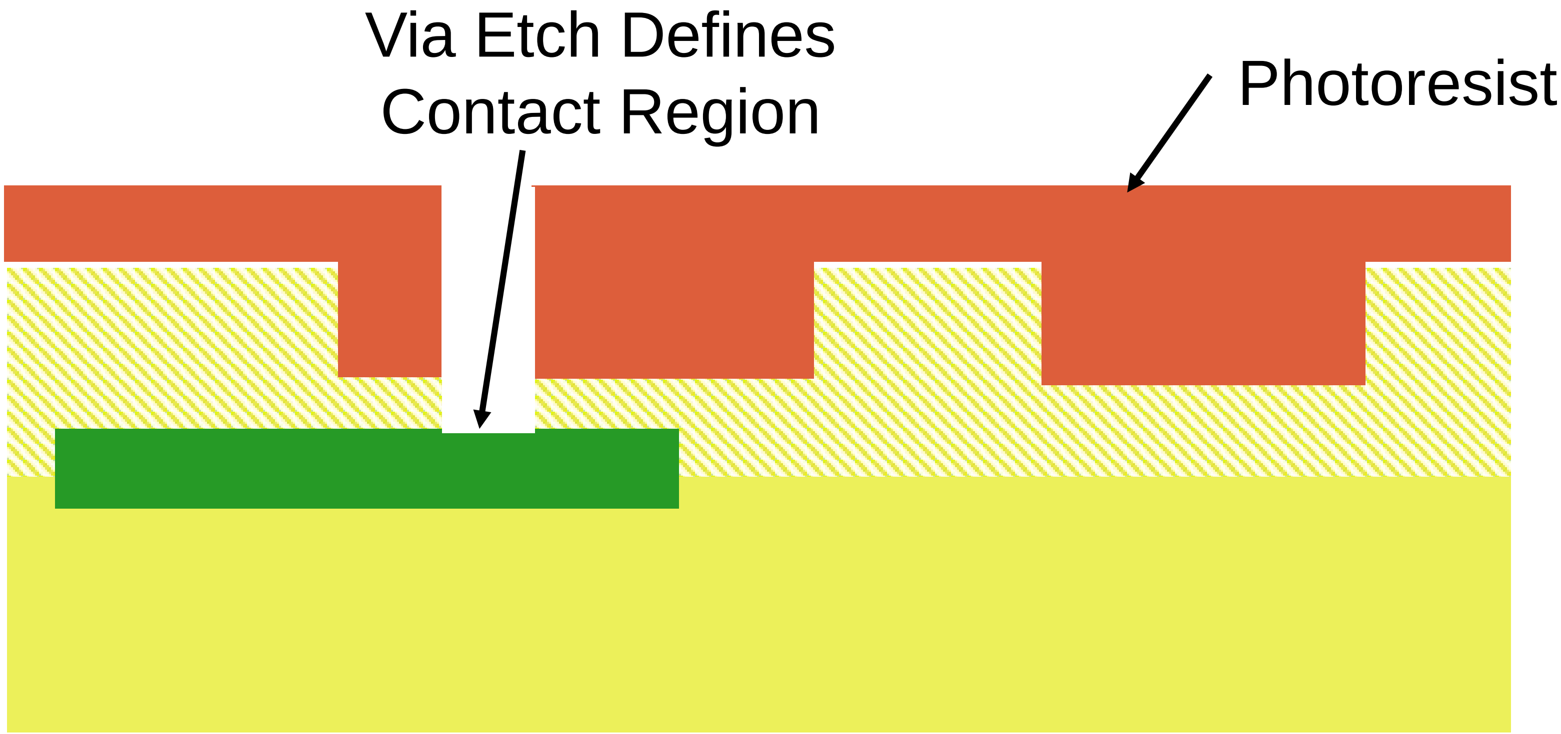
Dual-Damascene Process

Via Defined in PR
with Via Mask



Patterning of Copper

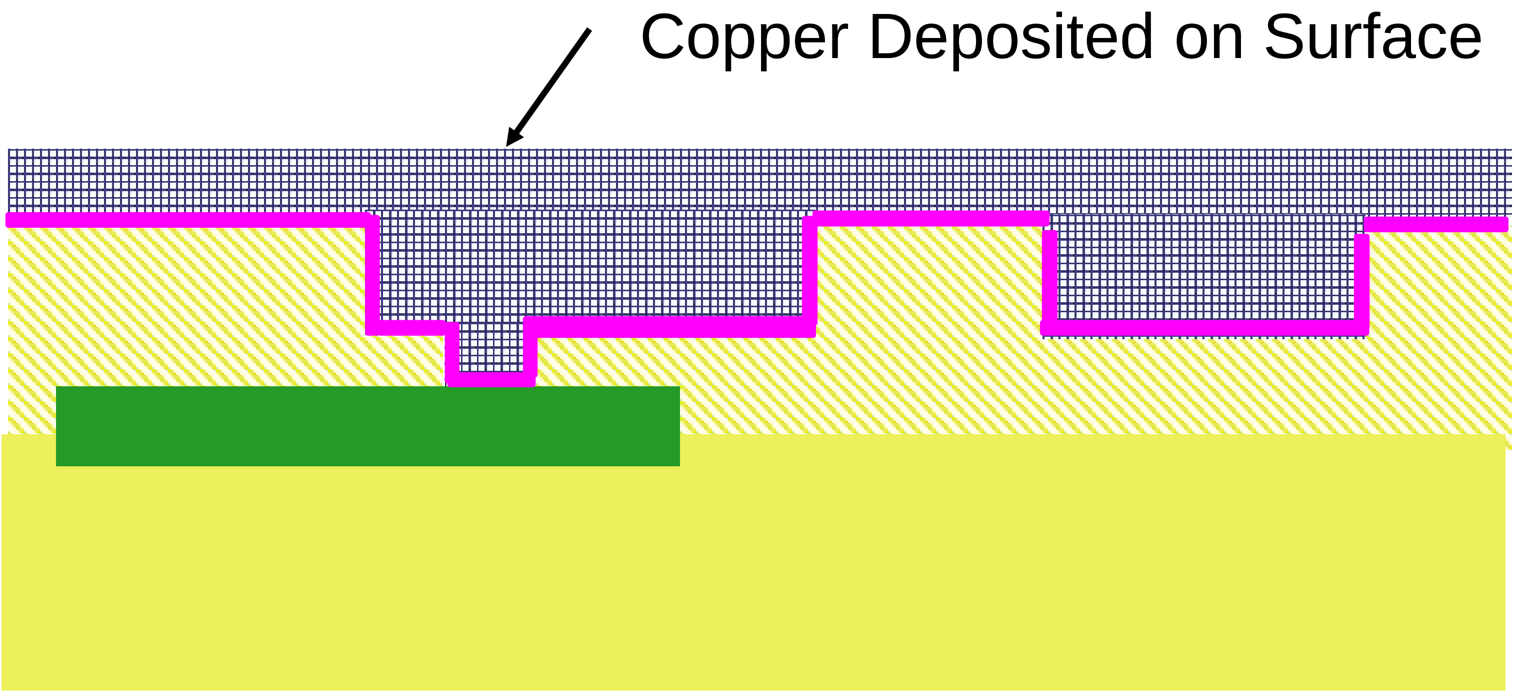
Dual-Damascene Process



(Barrier Metal added before copper but not shown)

Patterning of Copper

Dual-Damascene Process



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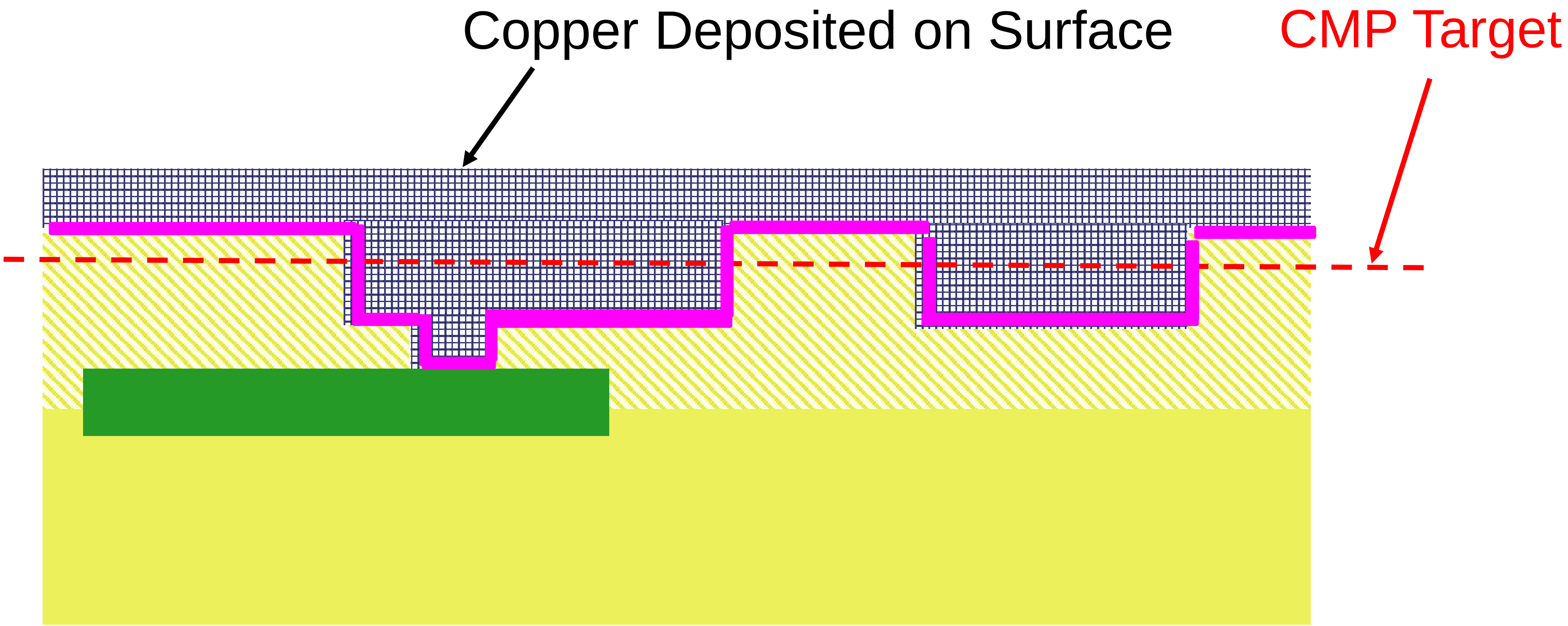
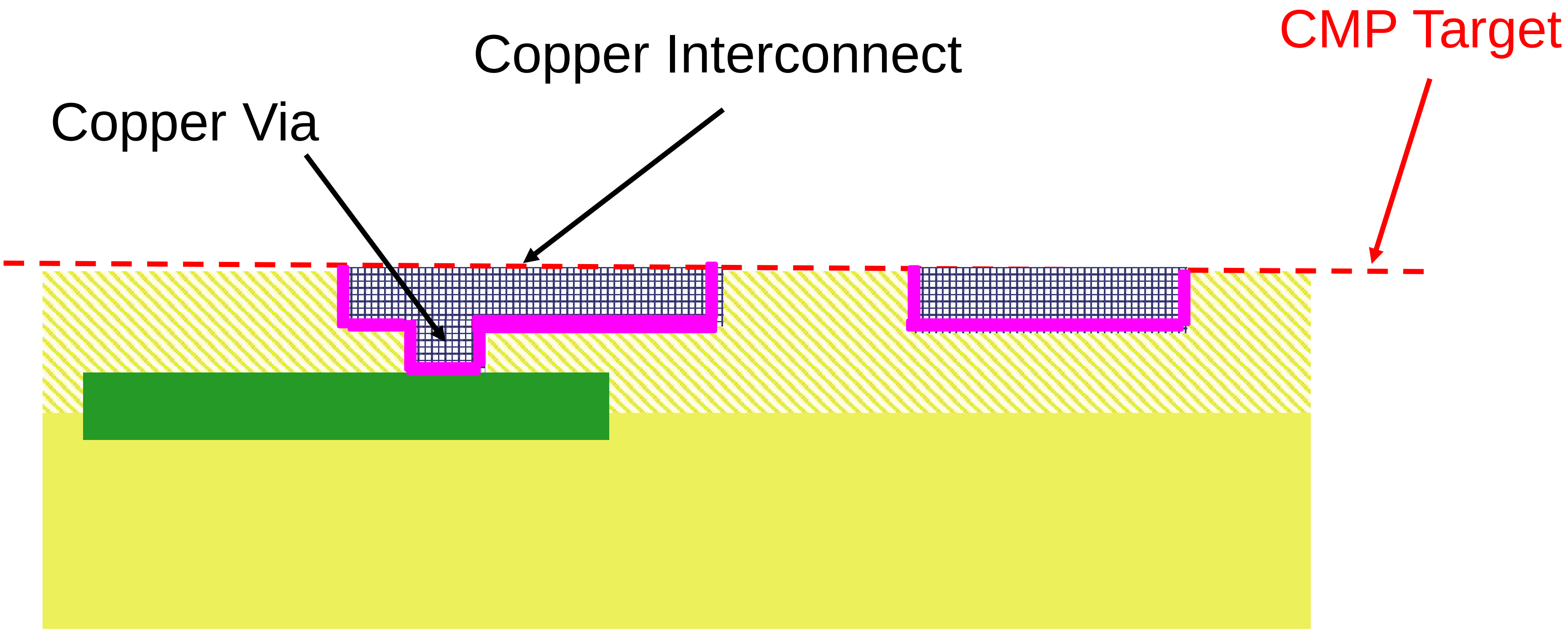
Patterning of Copper

Dual-Damascene Process



Patterning of Copper

Dual-Damascene Process



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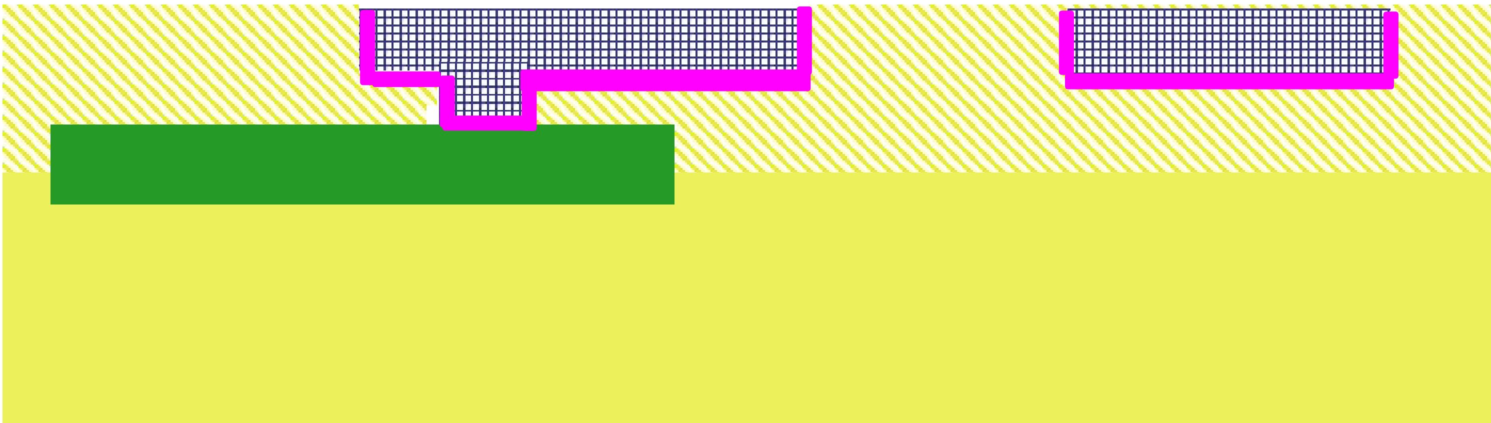


Both Damascene Processes Realize Same Structure

Damascene Process

Two Dielectric Deposition Steps
Two CMP Steps
Two Metal Deposition Steps
Two Dielectric Etches
W-Plug

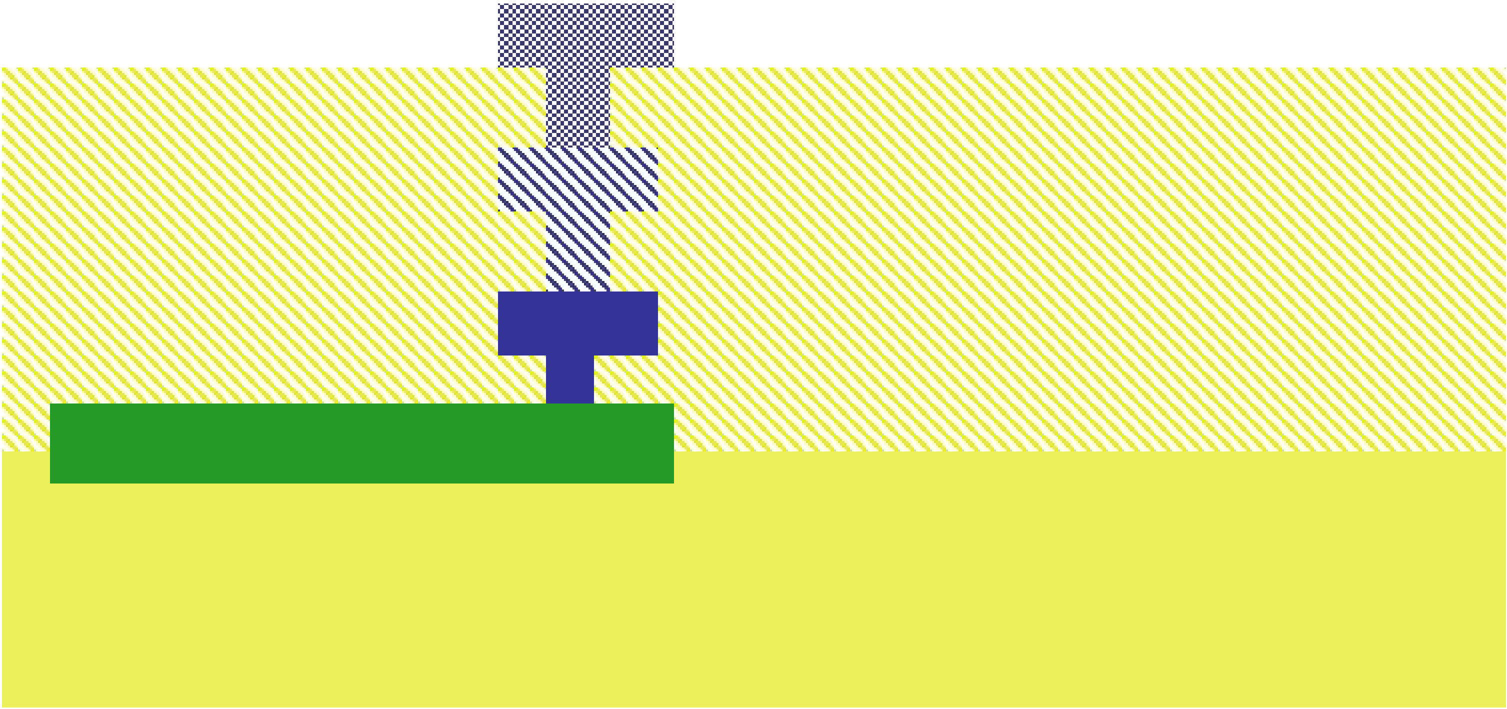
Dual-Damascene Process

One Dielectric Deposition Steps
One CMP Steps
One Metal Deposition Steps
Two Dielectric Etches
Via formed with metal step

Multiple Level Interconnects

3-rd level metal connection to n-active without stacked vias

Multiple Level Interconnects



3-rd level metal connection to n-active with stacked vias

Interconnect Layers May Vary in Thickness or Be Mostly Uniform

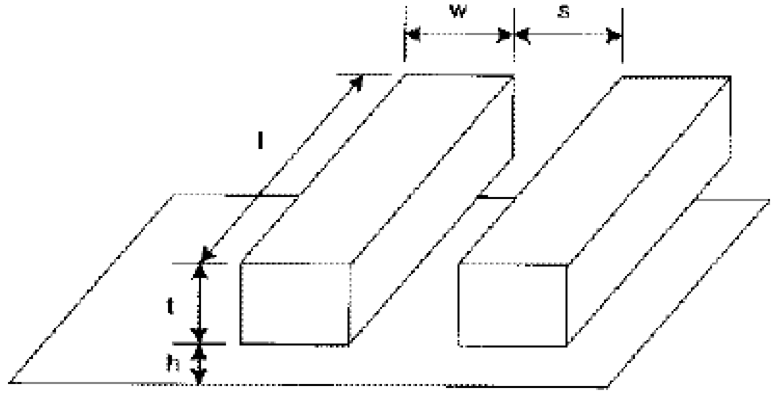


FIG 4.30 Interconnect geometry

Layer	t (nm)	w (nm)	s (nm)	AR
6	1720	860	860	2.0
	1000			
5	1600	800	800	2.0
	1000			
4	1080	540	540	2.0
	700			
3	700	320	320	2.2
	700			
2	700	320	320	2.2
	700			
1	480	250	250	1.9
	800			

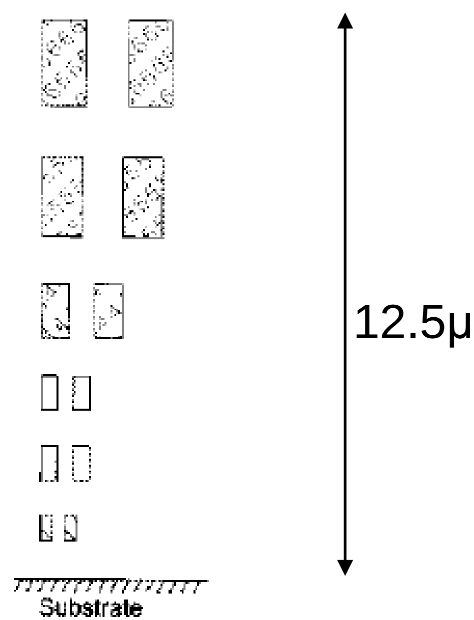


FIG 4.31 Layer stack for 6-metal Intel 180 nm process

Interconnects

- Metal is preferred interconnect
  - Because conductivity is high
- Parasitic capacitances and resistances of concern in all interconnects
- Polysilicon used for short interconnects
  - Silicided to reduce resistance
  - Unsilicided when used as resistors
- Diffusion used for short interconnects
  - Parasitic capacitances are high

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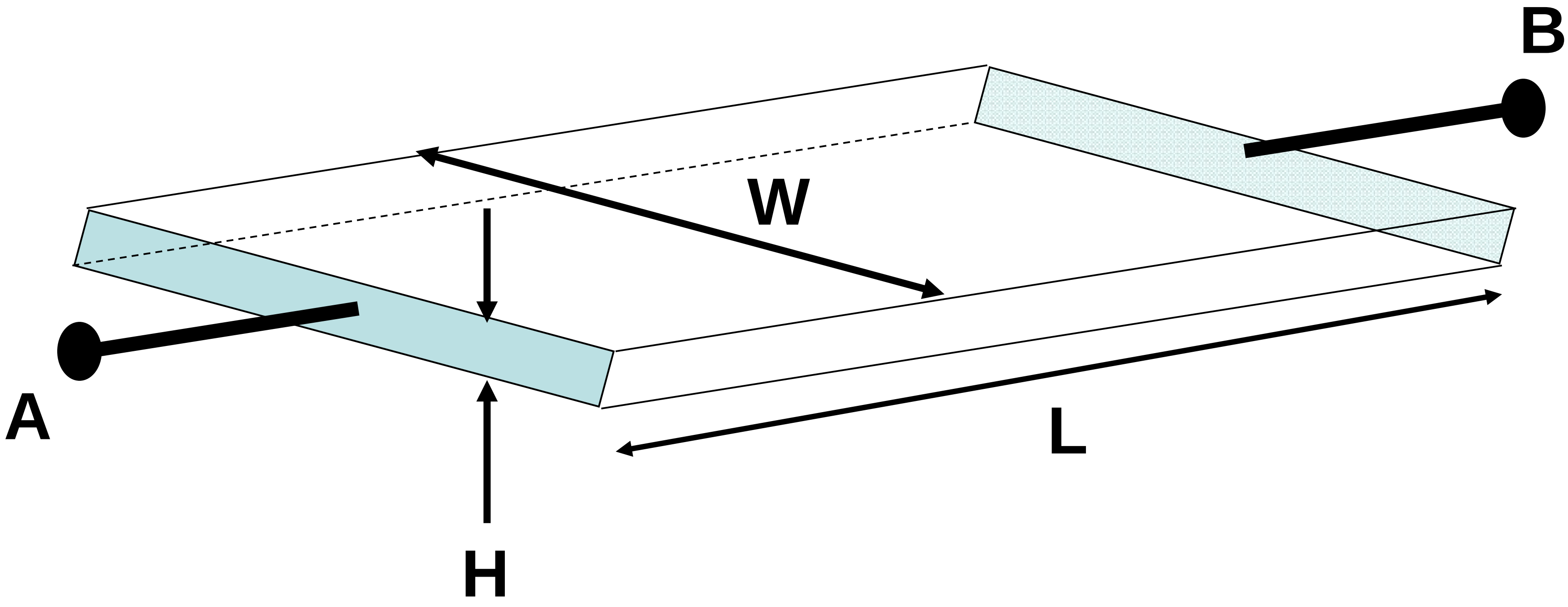
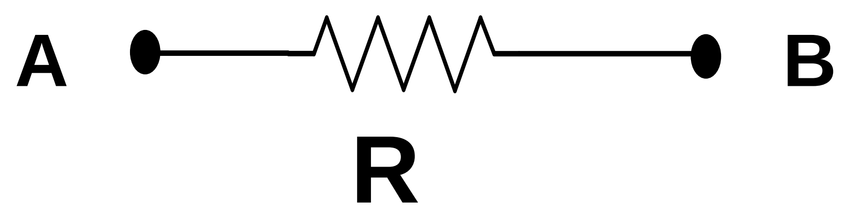
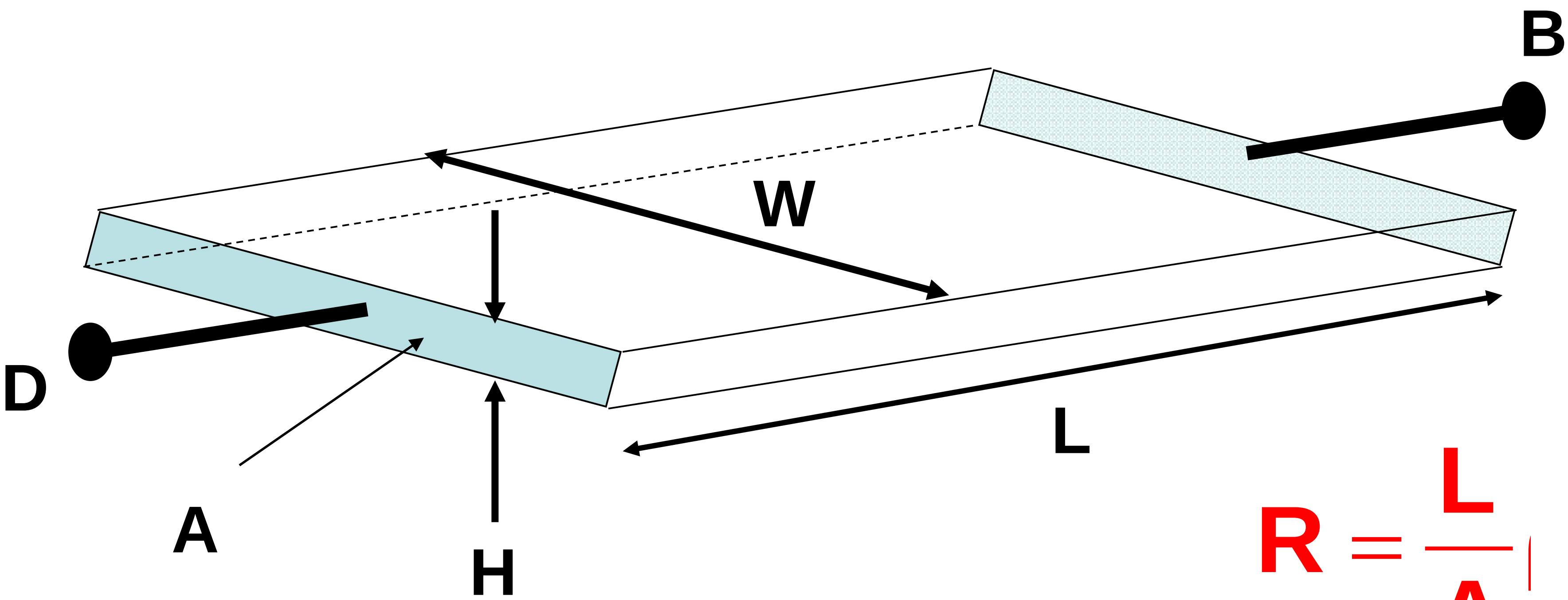
Resistance in Interconnects



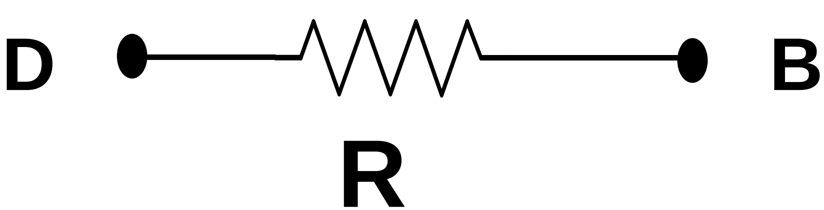


Resistance in Interconnects



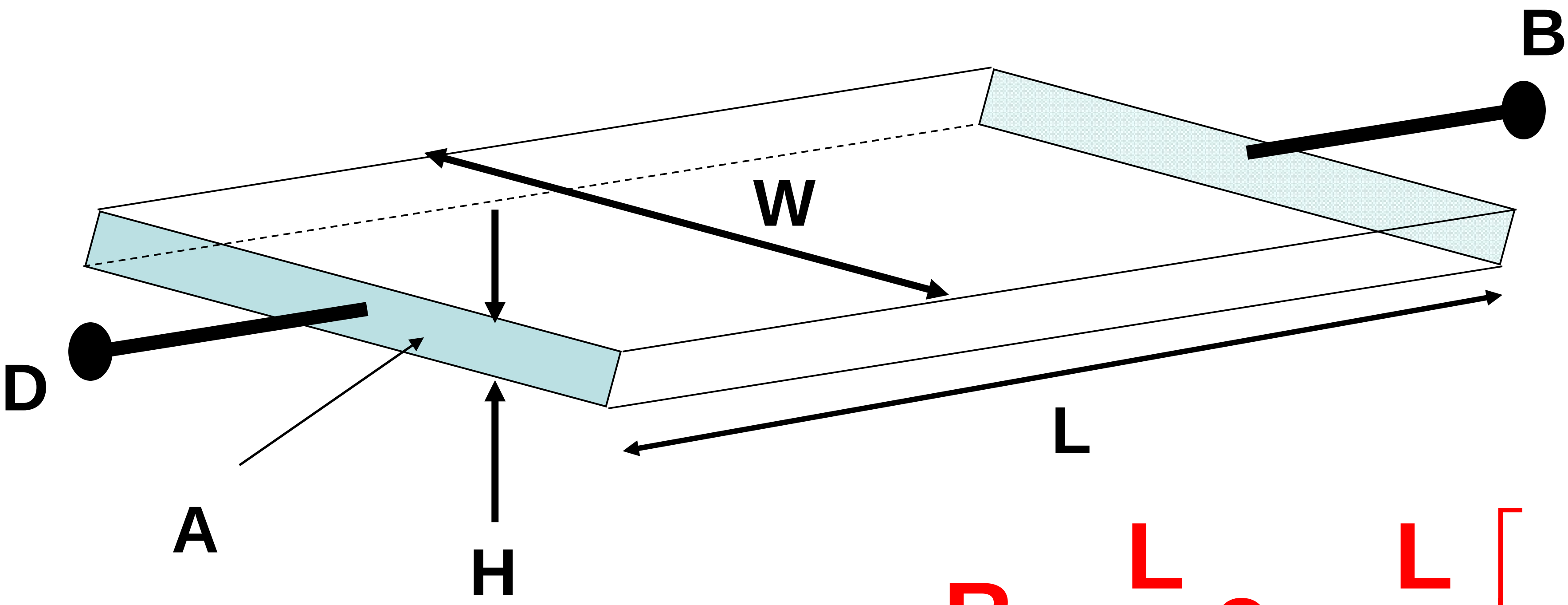
$$R = \frac{L}{A}$$

A=HW



ρ independent of geometry and characteristic of the process

Resistance in Interconnects



$$R = \frac{L}{A}\rho = \frac{L}{W}$$

H << W and H << L in most processes

Interconnect behaves as a “thin” film

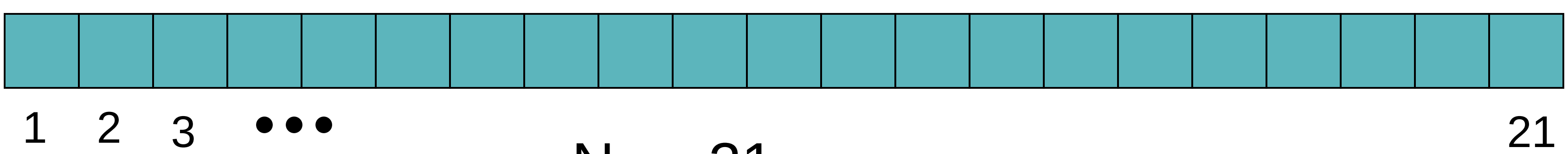
Sheet resistance often used instead of conductivity to characterize film

$R_{\square} = \rho / H$ $R = R_{\square}[L / W]$

Resistance in Interconnects

$$R = R_{\square}[L / W]$$

The “Number of Squares” approach to resistance determination in thin films

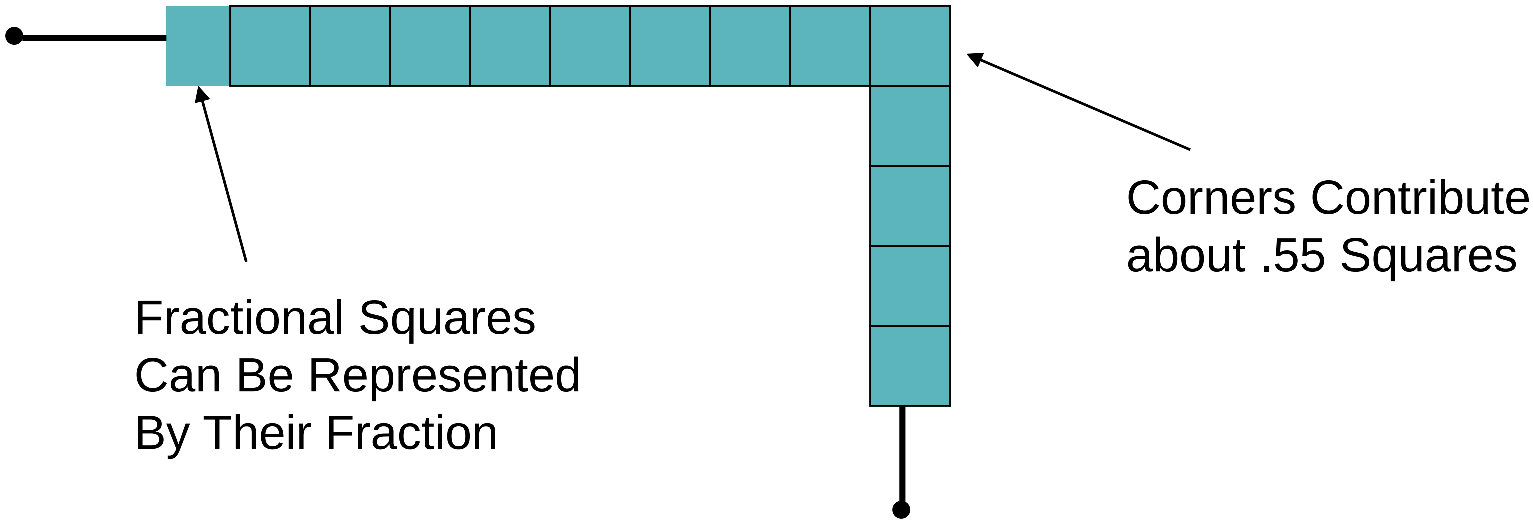


$$N_S = 21$$

$$L / W = 21$$

$$R = R_{\square} N_S$$

Resistance in Interconnects



The "squares" approach is not exact but is good enough for calculating resistance in almost all applications

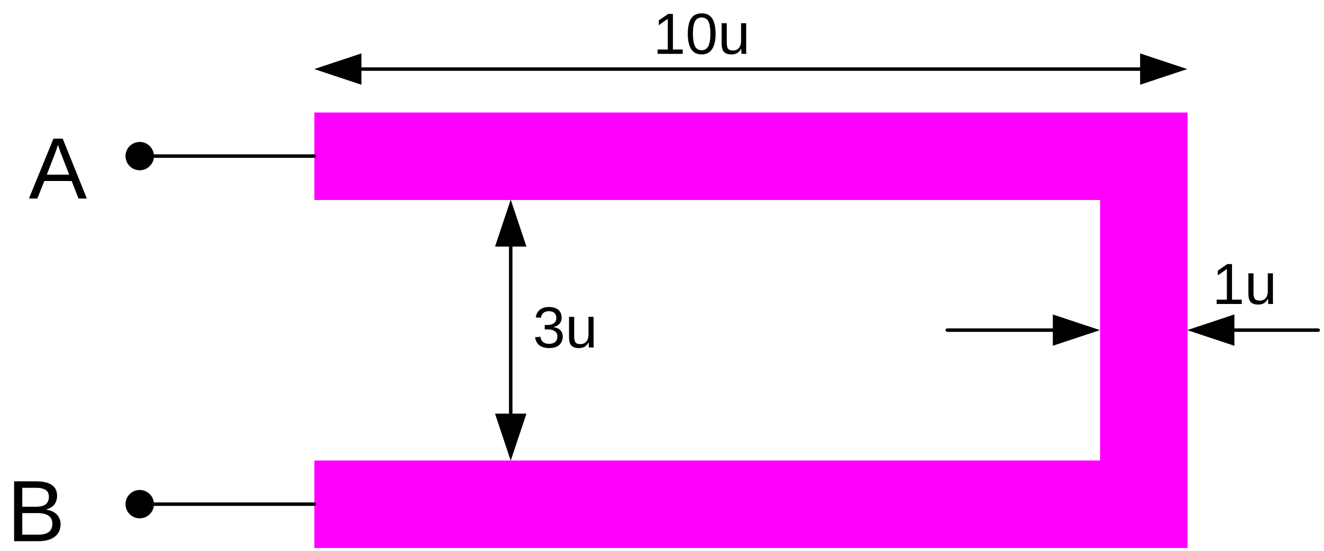
In this example:

$$N_S = 12 + .55 + .7 = 13.25$$

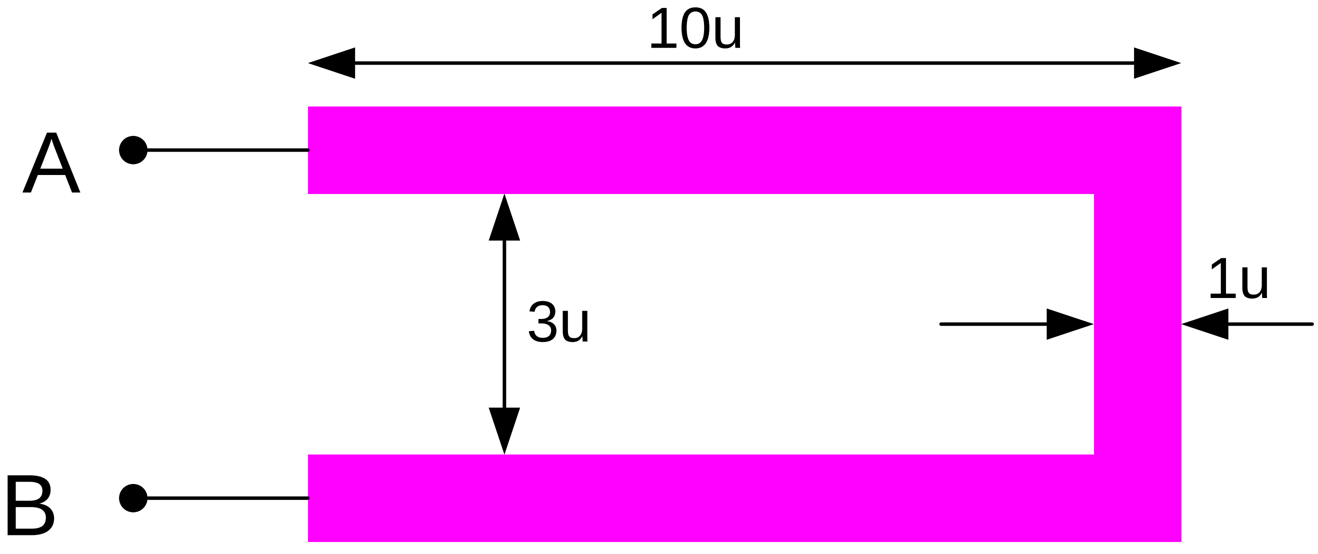
$$\mathbf{R = R_{\square} 13.25}$$

Example:

The layout of a film resistor with electrodes A and B is shown. If the sheet resistance of the film is 40 Ω/☐, determine the resistance between nodes A and B.



Solution

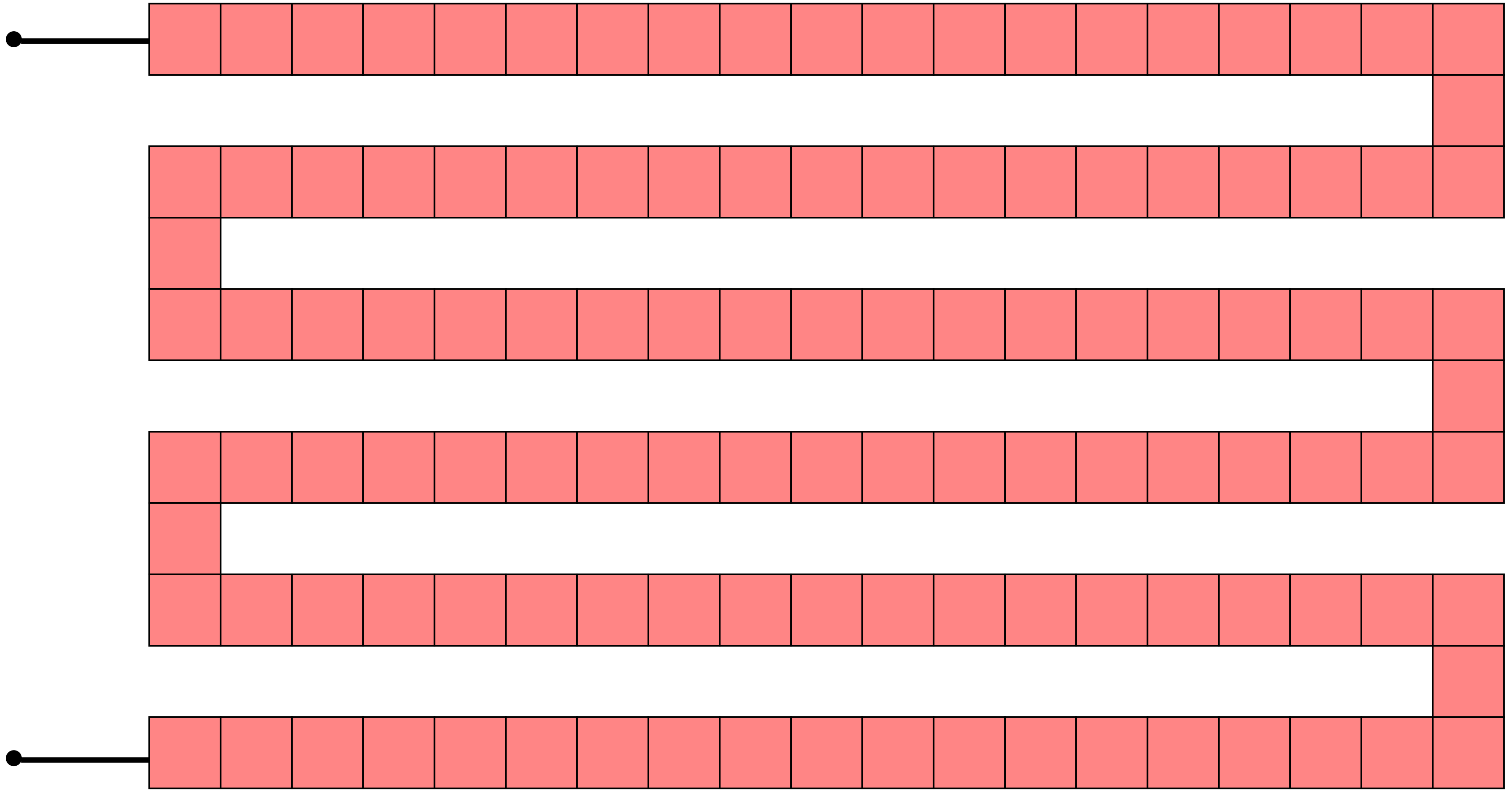


$N_S = 9+9+3+2(.55) = 22.1$

$R_{AB} = R_{\square} N_S = 40 \times 22.1 = 884\Omega$

Resistance in Interconnects

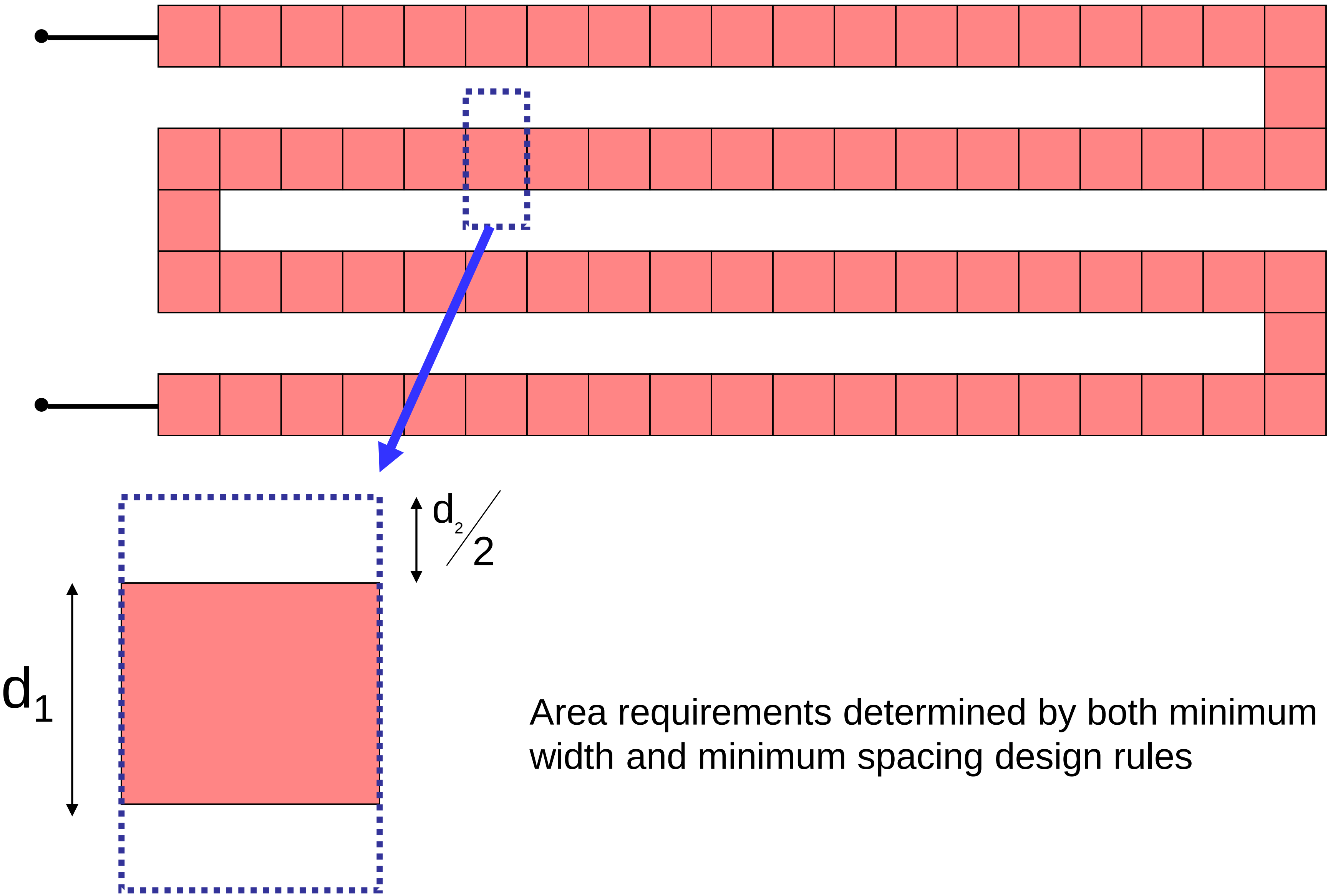
(can be used to build resistors!)



- Serpentine often used when large resistance required
- Polysilicon or diffusion often used for resistor creation
- Effective at managing the aspect ratio of large resistors
- May include hundreds or even thousands of squares

Resistance in Interconnects

(can be used to build resistors!)



Area requirements determined by both minimum width and minimum spacing design rules

End of Lecture 10