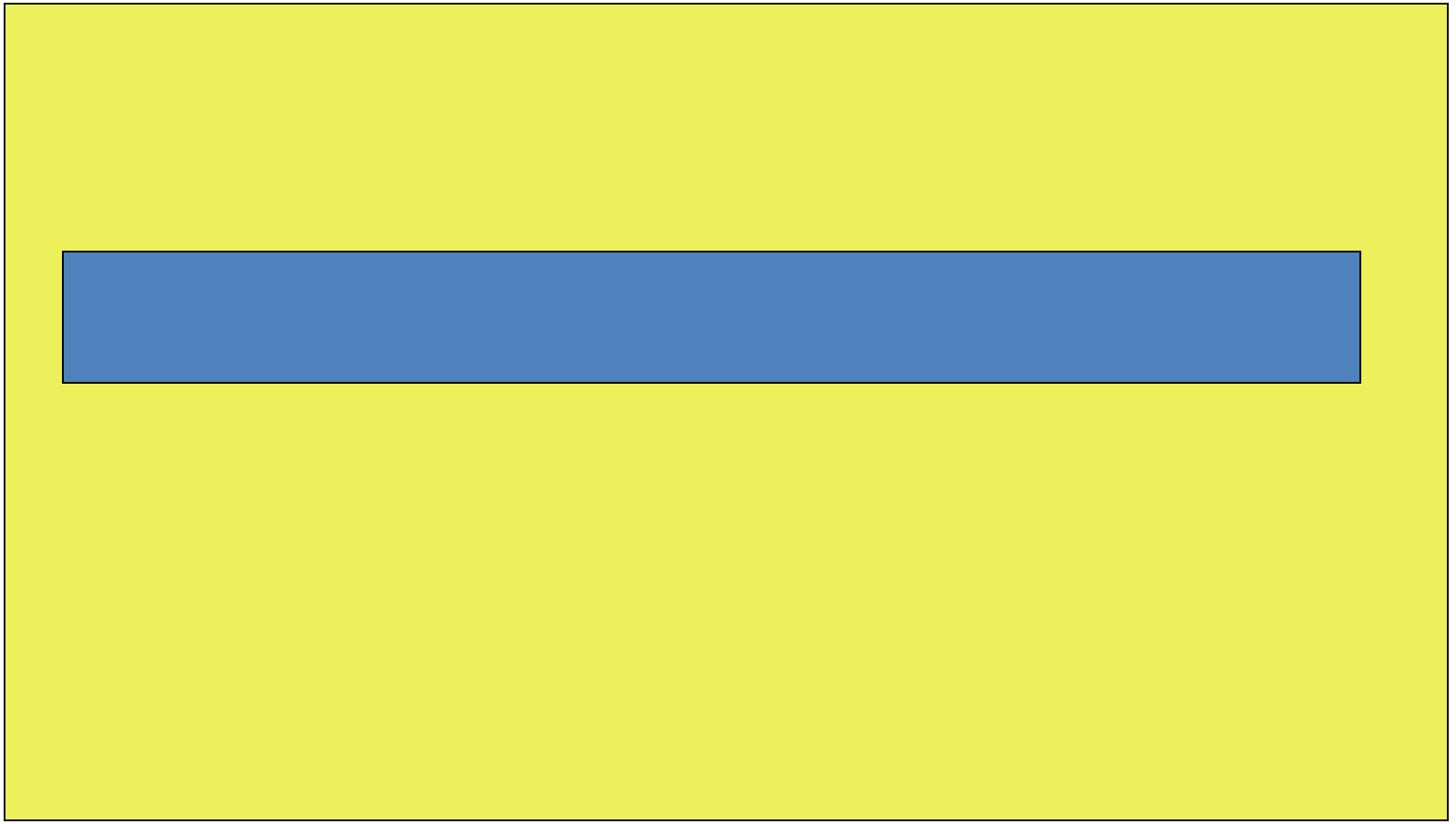
EE 330
Lecture 11

Capacitances in Interconnects

Back-end Processing

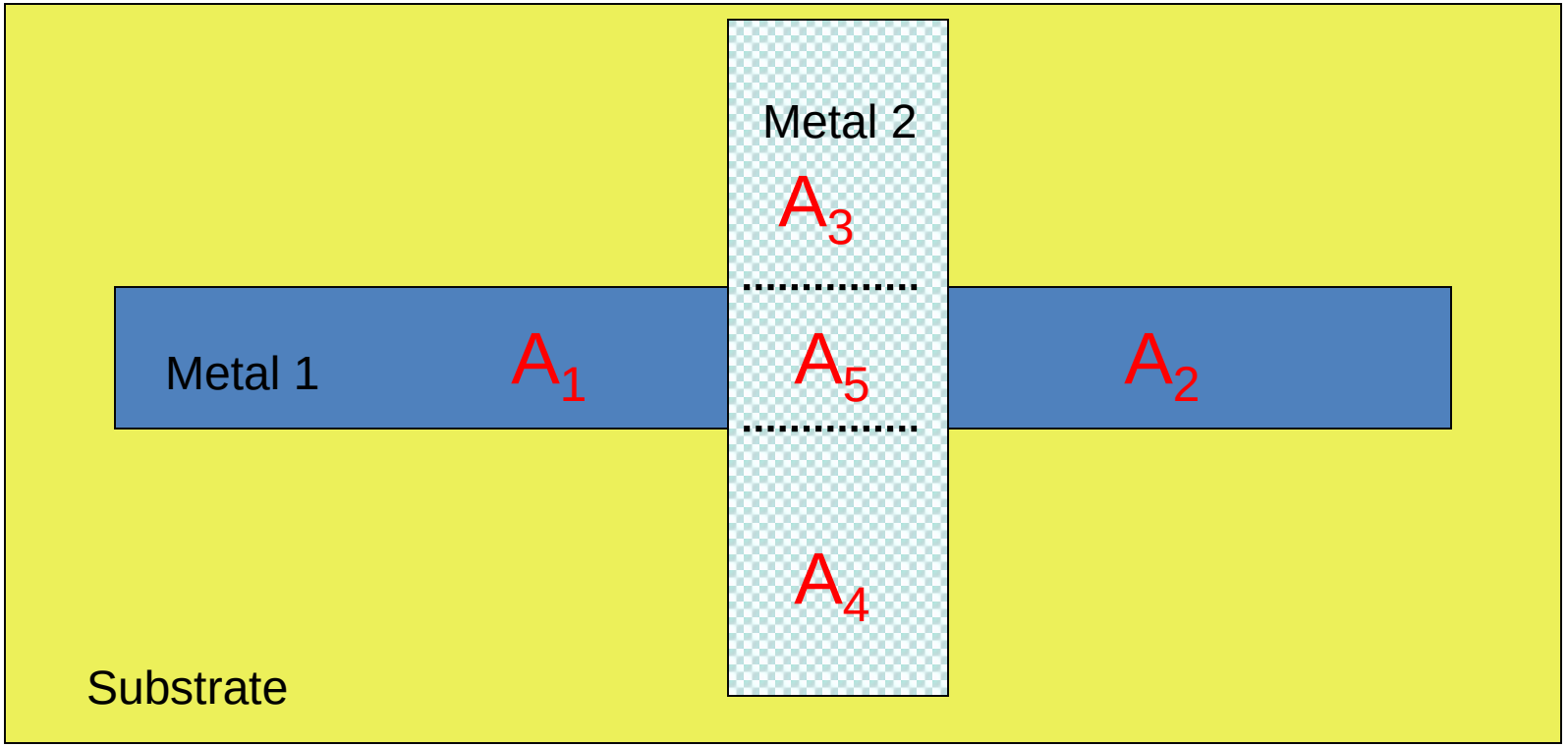
Capacitance in Interconnects

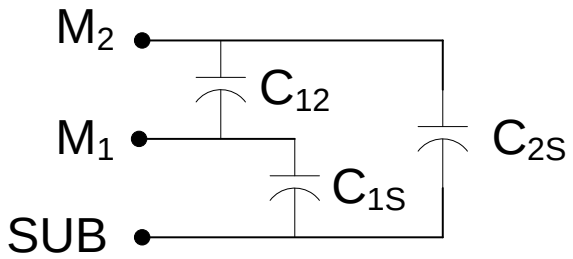


$$C=C_DA$$

C_D is the capacitance density and A is the area of the overlap

Capacitance in Interconnects





Equivalent Circuit

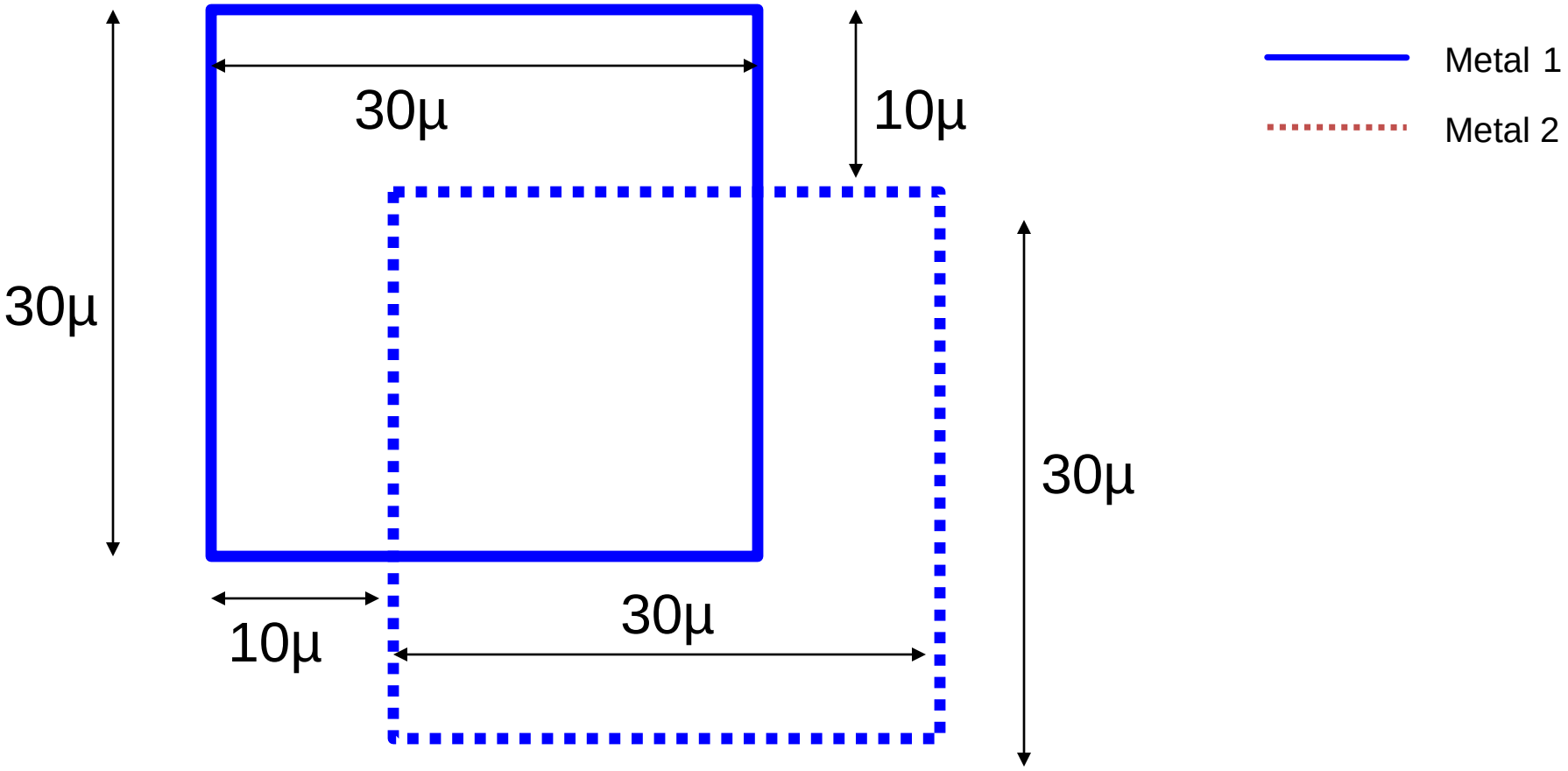
$$C_{12}=C_{D12}\,A_5$$

$$C_{1S}=C_{D1S}\,(A_1+A_2+A_5)$$

$$C_{2S}=C_{D2S}\,(A_3+A_4)$$

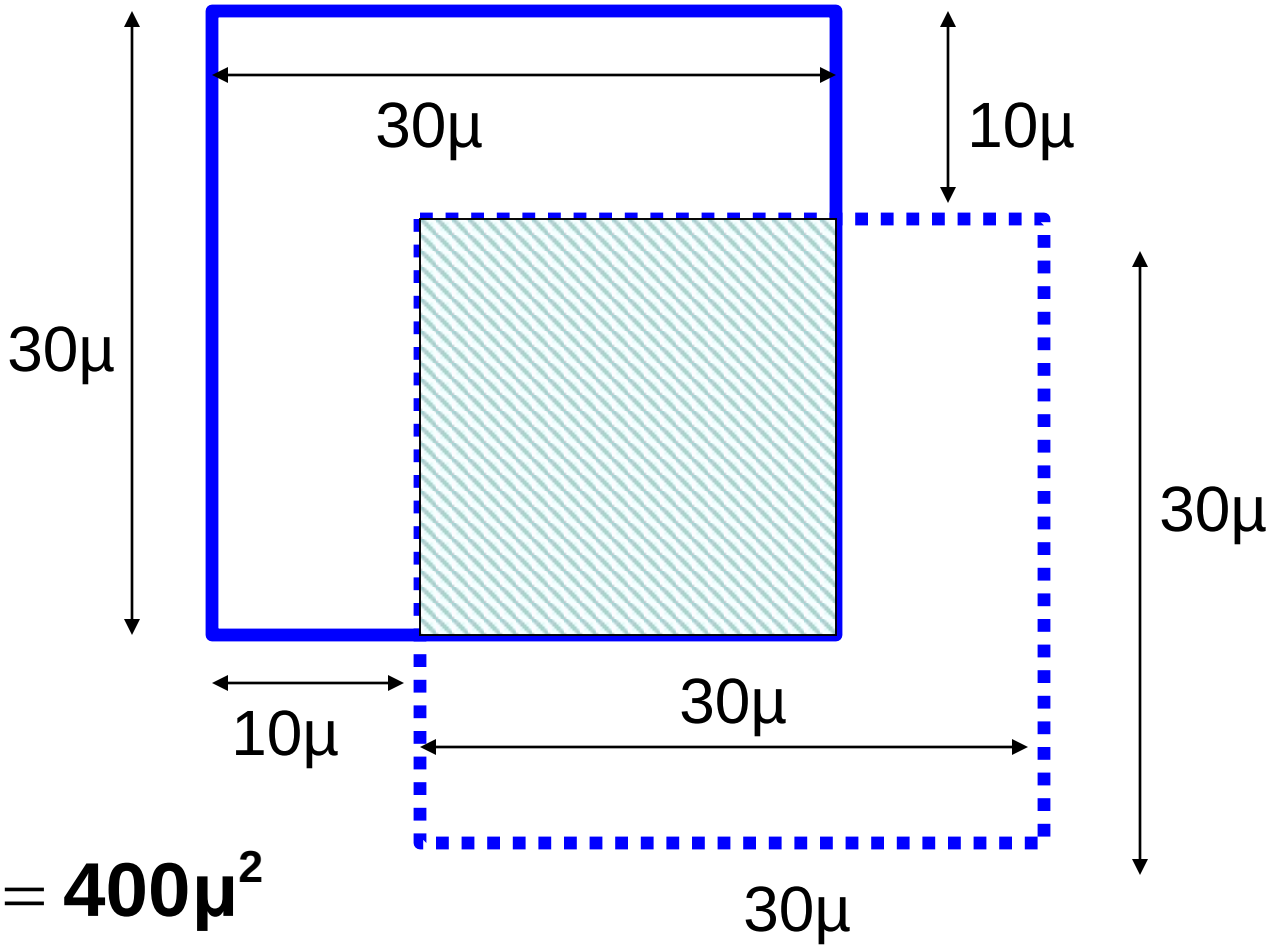
Example

Two metal layers, Metal 1 and Metal 2, are shown. Both are above field oxide. Determine the capacitance between Metal 1 and Metal 2. Assume the process has capacitance densities from M_1 to substrate of .05fF/u^2, from M_1 to M_2 of .07fF/u^2 and from M_2 to substrate of .025fF/u^2.



Example

Solution



$$A_{C1C2} = (20\mu)^2 = 400\mu^2$$

The capacitance density from M_1 to M_2 is .07fF/u^2

$$C_{12} = A_{C1C2} \bullet C_{D12} = 400\mu^2 \bullet 0.07\text{fF}/\mu^2 = 28\text{fF}$$

Capacitance and Resistance in Interconnects

- See MOSIS WEB site for process parameters that characterize parasitic resistances and capacitances

www.mosis.org

MOSIS WAFER ACCEPTANCE TESTS

RUN: T4BK (MM_NON-EPI_THK-MTL) VENDOR: TSMC
TECHNOLOGY: SCN018 FEATURE SIZE: 0.18 microns

INTRODUCTION: This report contains the lot average results obtained by MOSIS from measurements of MOSIS test structures on each wafer of this fabrication lot. SPICE parameters obtained from similar measurements on a selected wafer are also attached.

COMMENTS: DSCN6M018_TSMC

TRANSISTOR PARAMETERS	W/L	N-CHANNEL	P-CHANNEL	UNITS
MINIMUM	0.27/0.18			
Vth		0.50	-0.53	volts
SHORT	20.0/0.18			
Idss		571	-266	uA/um
Vth		0.51	-0.53	volts
Vpt		4.7	-5.5	volts
WIDE	20.0/0.18			
Ids0		22.0	-5.6	pA/um
LARGE	50/50			
Vth		0.42	-0.41	volts
Vjbkd		3.1	-4.1	volts
Ijlk		<50.0	<50.0	pA
K' (Uo*Cox/2)		171.8	-36.3	uA/V^2
Low-field Mobility		398.02	84.10	cm^2/V*s

COMMENTS: Poly bias varies with design technology. To account for mask bias use the appropriate value for the parameters XL and XW in your SPICE model card.

FOX TRANSISTORS	GATE	N+ACTIVE	P+ACTIVE	UNITS
Vth	Poly	>6.6	<-6.6	volts

PROCESS PARAMETERS	N+	P+	POLY	N+BLK	PLY+BLK	M1	M2	UNITS
Sheet Resistance	6.6	7.5	7.7	61.0	317.1	0.08	0.08	ohms/sq
Contact Resistance	10.1	10.6	9.3				4.18	ohms

PROCESS PARAMETERS	M3	POLY_HRI	M4	M5	M6	N_W	UNITS
Sheet Resistance	0.08	991.5	0.08	0.08	0.01	941	ohms/sq
Contact Resistance	8.97		14.09	18.84	21.44		ohms

COMMENTS: BLK is silicide block.

CAPACITANCE PARAMETERS	N+	P+	POLY	M1	M2	M3	M4	M5	M6	R_W	D_N_W	M5P	N_W	UNITS
Area (substrate)	998	1152	103	39	19	13	9	8	3		129		127	aF/um^2
Area (N+active)			8566	54	21	14	11	10	9					aF/um^2
Area (P+active)			8324											aF/um^2
Area (poly)				64	18	10	7	6	5					aF/um^2
Area (metal1)					44	16	10	7	5					aF/um^2
Area (metal2)						38	15	9	7					aF/um^2
Area (metal3)							40	15	9					aF/um^2
Area (metal4)								37	14					aF/um^2
Area (metal5)									36			1003		aF/um^2
Area (r well)	987													aF/um^2
Area (d well)										574				aF/um^2
Area (no well)	139													aF/um^2
Fringe (substrate)	244	201		18	61	55	43	25						aF/um
Fringe (poly)				69	39	29	24	21	19					aF/um
Fringe (metal1)					61	35		23	21					aF/um
Fringe (metal2)						54	37	27	24					aF/um
Fringe (metal3)							56	34	31					aF/um
Fringe (metal4)								58	40					aF/um
Fringe (metal5)									61					aF/um
Overlap (P+active)			652											aF/um

T4BK SPICE BSIM3 VERSION 3.1 PARAMETERS

SPICE 3f5 Level 8, Star-HSPICE Level 49, UTMOST Level 8

* DATE: Jan 21/05
* LOT: T4BK WAF: 3004

```
* Temperature_parameters=Default
.MODEL CMOSN NMOS (                                LEVEL   = 49
+VERSION = 3.1           TNOM    = 27              TOX     = 4E-9
+XJ      = 1E-7          NCH     = 2.3549E17       VTH0    = 0.3662648
+K1      = 0.5802748     K2      = 3.124029E-3     K3      = 1E-3
+K3B     = 3.3886871     W0      = 1E-7            NLX     = 1.766159E-7
+DVT0W   = 0             DVT1W   = 0               DVT2W   = 0
+DVT0    = 1.2312416     DVT1    = 0.3849841       DVT2    = 0.0161351
+U0      = 265.1889031   UA      = -1.506402E-9    UB      = 2.489393E-18
+UC      = 5.621884E-11  VSAT    = 1.017932E5      A0      = 2
+AGS     = 0.4543117     B0      = 3.433489E-7     B1      = 5E-6
+KETA    = -0.0127714    A1      = 1.158074E-3     A2      = 1
+RDSW    = 136.5582806   PRWG    = 0.5             PRWB    = -0.2
+WR      = 1             WINT    = 0               LINT    = 1.702415E-8
+XL      = 0             XW      = -1E-8           DWG     = -4.211574E-9
+DWB     = 1.107719E-8   VOFF    = -0.0948017      NFACTOR = 2.1860065
+CIT     = 0             CDSC    = 2.4E-4          CDSCD   = 0
+CDSCB   = 0             ETA0    = 3.335516E-3     ETAB    = 6.028975E-5
+DSUB    = 0.0214781     PCLM    = 0.6602119       PDIBLC1 = 0.1605325
+PDIBLC2 = 3.287142E-3   PDIBLCB = -0.1            DROUT   = 0.7917811
+PSCBE1  = 6.420235E9    PSCBE2  = 4.122516E-9     PVAG    = 0.0347169
+DELTA   = 0.01          RSH     = 6.6             MOBMOD  = 1
+PRT     = 0             UTE     = -1.5            KT1     = -0.11
+KT1L    = 0             KT2     = 0.022           UA1     = 4.31E-9
+UB1     = -7.61E-18     UC1     = -5.6E-11        AT      = 3.3E4
+WL      = 0             WLN     = 1               WW      = 0
+WWN     = 1             WWL     = 0               LL      = 0
+LLN     = 1             LW      = 0               LWN     = 1
+LWL     = 0             CAPMOD  = 2               XPART   = 0.5
+CGDO    = 8.06E-10      CGSO    = 8.06E-10        CGBO    = 1E-12
+CJ      = 9.895609E-4   PB      = 0.8             MJ      = 0.3736889
+CJSW    = 2.393608E-10  PBSW    = 0.8             MJSW    = 0.1537892
+CJSWG   = 3.3E-10       PBSWG   = 0.8             MJSWG   = 0.1537892
+CF      = 0             PVTH0   = -1.73163E-3     PRDSW   = -1.4173554
+PK2     = 1.600729E-3   WKETA   = 1.601517E-3     LKETA   = -3.255127E-3
+PU0     = 5.2024473     PUA     = 1.584315E-12    PUB     = 7.446142E-25
+PVSAT   = 1.686297E3    PETA0   = 1.001594E-4     PKETA   = -2.039532E-3    )
*
```

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+VERSION = 3.1           TNOM    = 27              TOX     = 4E-9
+XJ      = 1E-7          NCH     = 4.1589E17       VTH0    = -0.3708038
+K1      = 0.5895473     K2      = 0.0235946       K3      = 0
+K3B     = 13.8642028    W0      = 1E-6            NLX     = 1.517201E-7
+DVT0W   = 0             DVT1W   = 0               DVT2W   = 0
+DVT0    = 0.7885088     DVT1    = 0.2564577       DVT2    = 0.1
+U0      = 103.0478426   UA      = 1.049312E-9     UB      = 2.545758E-21
+UC      = -1E-10        VSAT    = 1.645114E5      A0      = 1.627879
+AGS     = 0.3295499     B0      = 5.207699E-7     B1      = 1.370868E-6
+KETA    = 0.0296157     A1      = 0.4449009       A2      = 0.3
+RDSW    = 306.5789827   PRWG    = 0.5             PRWB    = 0.5
+WR      = 1             WINT    = 0               LINT    = 2.761033E-8
+XL      = 0             XW      = -1E-8           DWG     = -2.433889E-8
+DWB     = -9.34648E-11  VOFF    = -0.0867009      NFACTOR = 2
+CIT     = 0             CDSC    = 2.4E-4          CDSCD   = 0
+CDSCB   = 0             ETA0    = 1.018318E-3     ETAB    = -3.206319E-4
+DSUB    = 1.094521E-3   PCLM    = 1.3281073       PDIBLC1 = 2.394169E-3
+PDIBLC2 = -3.255915E-6  PDIBLCB = -1E-3           DROUT   = 0
+PSCBE1  = 4.881933E10   PSCBE2  = 5E-10           PVAG    = 2.0932623

+DELTA   = 0.01          RSH     = 7.5             MOBMOD  = 1
+PRT     = 0             UTE     = -1.5            KT1     = -0.11
+KT1L    = 0             KT2     = 0.022           UA1     = 4.31E-9
+UB1     = -7.61E-18     UC1     = -5.6E-11        AT      = 3.3E4
+WL      = 0             WLN     = 1               WW      = 0
+WWN     = 1             WWL     = 0               LL      = 0
+LLN     = 1             LW      = 0               LWN     = 1
+LWL     = 0             CAPMOD  = 2               XPART   = 0.5
+CGDO    = 6.52E-10      CGSO    = 6.52E-10        CGBO    = 1E-12
+CJ      = 1.157423E-3   PB      = 0.8444261       MJ      = 0.4063933
+CJSW    = 1.902456E-10  PBSW    = 0.8             MJSW    = 0.3550788
+CJSWG   = 4.22E-10      PBSWG   = 0.8             MJSWG   = 0.3550788
+CF      = 0             PVTH0   = 1.4398E-3       PRDSW   = 0.5073407
+PK2     = 2.190431E-3   WKETA   = 0.0442978       LKETA   = -2.936093E-3
+PU0     = -0.9769623    PUA     = -4.34529E-11    PUB     = 1E-21
+PVSAT   = -50           PETA0   = 1.002762E-4     PKETA   = -6.740436E-3    )
*
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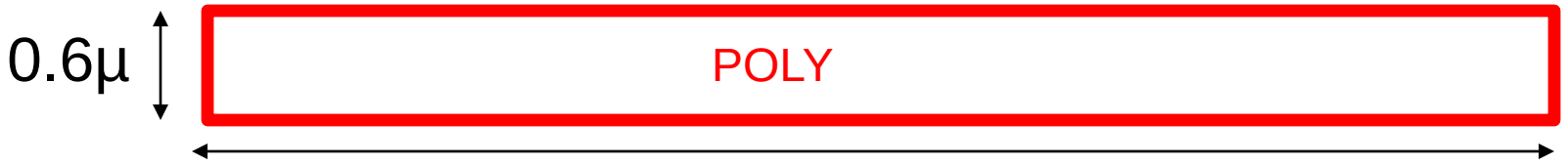
Example

Determine the resistance and capacitance of a Poly interconnect that is 0.6u wide and 800u long and compare that with the same interconnect if M_1 were used. Assume a 0.18u process.



800µ

$$R_{POLY} = n_{SQ} R_{SH}$$

$$C_{P\text{-}SUB} = A \bullet C_{DPS}$$

$$R_{SH} = ?$$

$$R_{DPS} = ?$$

For 0.18u process

PROCESS PARAMETERS	N+	P+	POLY	N+BLK	PLY+BLK	M1	M2	UNITS
Sheet Resistance	6.6	7.5	7.7	61.0	317.1	0.08	0.08	ohms/sq
Contact Resistance	10.1	10.6	9.3				4.18	ohms

R_{SH}=7.7Ω/□

PROCESS PARAMETERS	M3	POLY_HRI	M4	M5	M6	N_W	UNITS
Sheet Resistance	0.08	991.5	0.08	0.08	0.01	941	ohms/sq
Contact Resistance	8.97		14.09	18.84	21.44		ohms

COMMENTS: BLK is silicide block.

C_{DPS}=103 af/μ²

CAPACITANCE PARAMETERS	N+	P+	POLY	M1	M2	M3	M4	M5	M6	R_W	D_N_W	M5P	N_W	UNITS
Area (substrate)	998	1152	103	39	19	13	9	8	3		129		127	aF/um^2
Area (N+active)			8566	54	21	14	11	10	9					aF/um^2
Area (P+active)			8324											aF/um^2
Area (poly)				64	18	10	7	6	5					aF/um^2
Area (metal1)					44	16	10	7	5					aF/um^2
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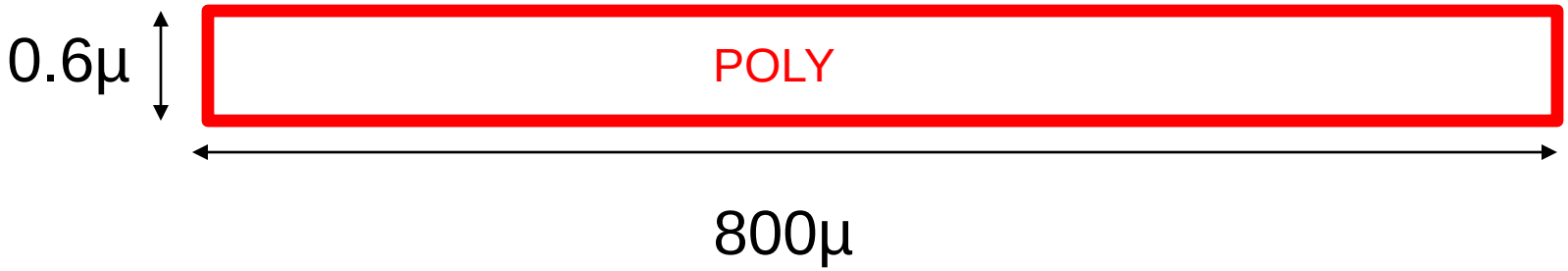
Area (metal4)								37	14					aF/um^2
Area (metal5)									36			1003		aF/um^2
Area (r well)	987													aF/um^2
Area (d well)										574				aF/um^2
Area (no well)	139													aF/um^2
Fringe (substrate)	244	201		18	61	55	43	25						aF/um
Fringe (poly)				69	39	29	24	21	19					aF/um
Fringe (metal1)					61	35		23	21					aF/um
Fringe (metal2)						54	37	27	24					aF/um
Fringe (metal3)							56	34	31					aF/um
Fringe (metal4)								58	40					aF/um
Fringe (metal5)									61					aF/um
Overlap (P+active)			652											aF/um

Example

For 0.18u process

Determine the resistance and capacitance of a Poly interconnect that is 0.6u wide and 800u long and compare that with the same interconnect if M_1 were used.



$$n_{SQ} = \frac{800\mu}{0.6\mu} = 1333$$

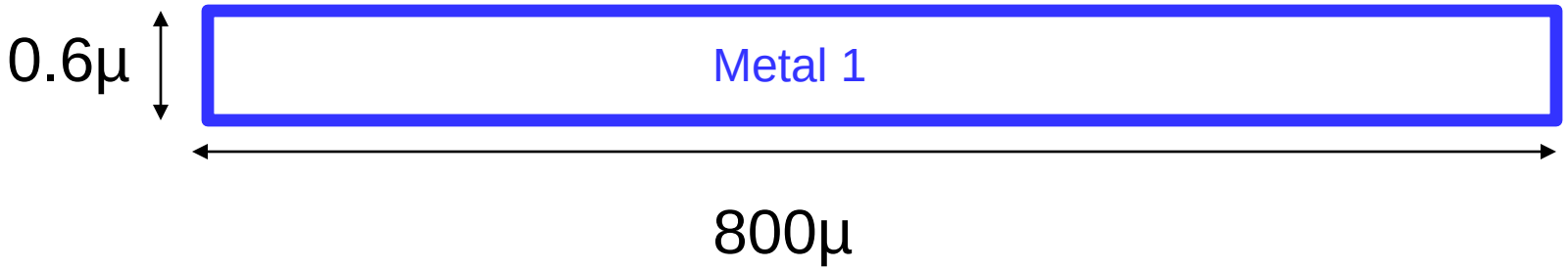
$$A = (0.6\mu)(800\mu) = 480\mu^2$$

$$R_{POLY} = n_{SQ} R_{SH} = 23.5 \bullet 1333 = 31.3K\Omega$$

$$C_{P\text{-}SUB} = A \bullet C_{DPS} = 480\mu^2 \bullet 84aF\mu^{-2} = 40.3fF$$

Example

Determine the resistance and capacitance of a Poly interconnect that is 0.6u wide and 800u long and compare that with the same interconnect if M_1 were used.



For 0.18u process

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Sheet Resistance	6.6	7.5	7.7	61.0	317.1	0.08	0.08	ohms/sq
Contact Resistance	10.1	10.6	9.3				4.18	ohms

R_{SH}=0.08Ω/

PROCESS PARAMETERS	M3	POLY_HRI	M4	M5	M6	N_W	UNITS
Sheet Resistance	0.08	991.5	0.08	0.08	0.01	941	ohms/sq
Contact Resistance	8.97		14.09	18.84	21.44		ohms

COMMENTS: BLK is silicide block.

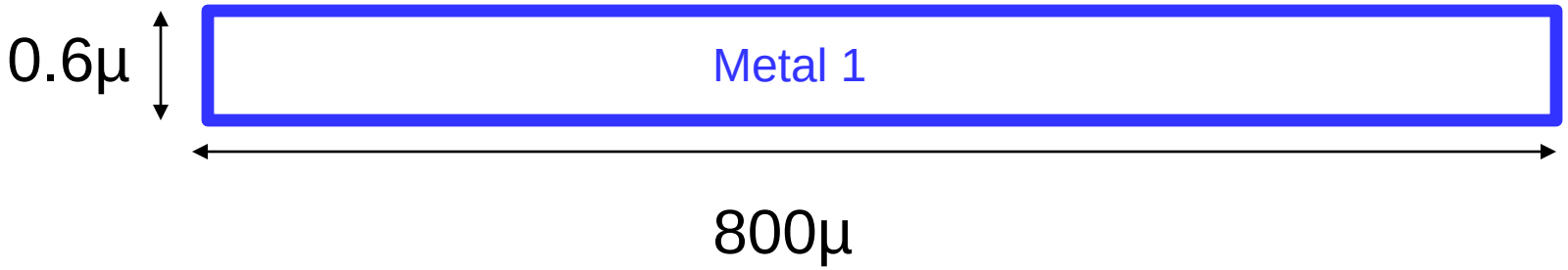
C_{DPS}=39 af/μ^2

CAPACITANCE PARAMETERS	N+	P+	POLY	M1	M2	M3	M4	M5	M6	R_W	D_N_W	M5P	N_W	UNITS
Area (substrate)	998	1152	103	39	19	13	9	8	3		129		127	aF/um^2
Area (N+active)			8566	54	21	14	11	10	9					aF/um^2
Area (P+active)			8324											aF/um^2
Area (poly)				64	18	10	7	6	5					aF/um^2
Area (metal1)					44	16	10	7	5					aF/um^2
Area (metal2)						38	15	9	7					aF/um^2
Area (metal3)							40	15	9					aF/um^2
Area (metal4)								37	14					aF/um^2
Area (metal5)									36			1003		aF/um^2
Area (r well)	987													aF/um^2
Area (d well)										574				aF/um^2
Area (no well)	139													aF/um^2
Fringe (substrate)	244	201		18	61	55	43	25						aF/um
Fringe (poly)				69	39	29	24	21	19					aF/um
Fringe (metal1)					61	35		23	21					aF/um
Fringe (metal2)						54	37	27	24					aF/um
Fringe (metal3)							56	34	31					aF/um
Fringe (metal4)								58	40					aF/um
Fringe (metal5)									61					aF/um
Overlap (P+active)			652											aF/um

Example

For 0.18u process

Determine the resistance and capacitance of a Poly interconnect that is 0.6u wide and 800u long and compare that with the same interconnect if M_1 were used.



$$n_{SQ} = \frac{800\mu}{0.6\mu} = 1333$$

$$A = (0.6\mu)(800\mu) = 480\mu^2$$

$$R_{M1} = n_{SQ} R_{SH} = 0.08 \bullet 1333 = 107\Omega$$

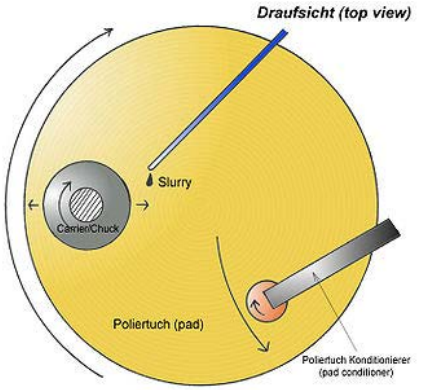
$$C_{M1\text{-}SUB} = A \bullet C_{DM1S} = 480\mu^2 \bullet 39aF\mu^{-2} = 18.7fF$$

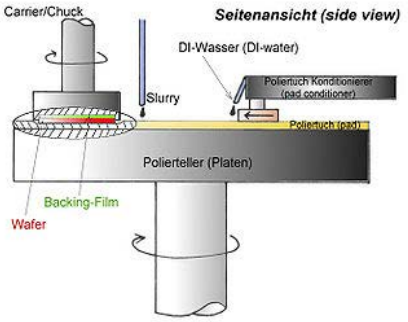
IC Fabrication Technology

- Crystal Preparation
- Masking
- Photolithographic Process
- Deposition
- Etching
- Diffusion
- Ion Implantation
- Oxidation
- Epitaxy
- Polysilicon
- Contacts, Interconnect and Metalization
- Planarization

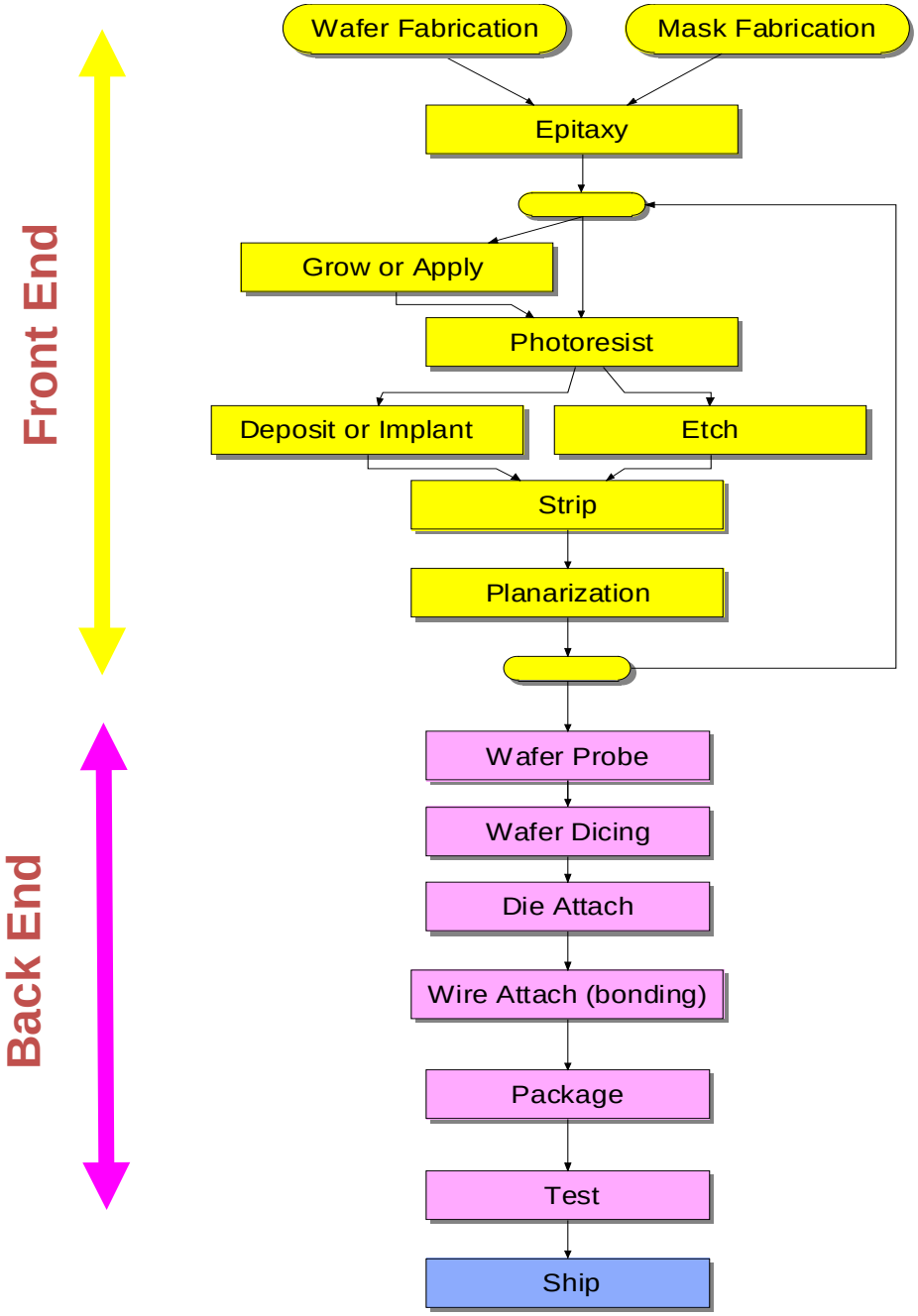
Planarization

- Planarization used to keep surface planar during subsequent processing steps
  - Important for creating good quality layers in subsequent processing steps
  - Mechanically planarized

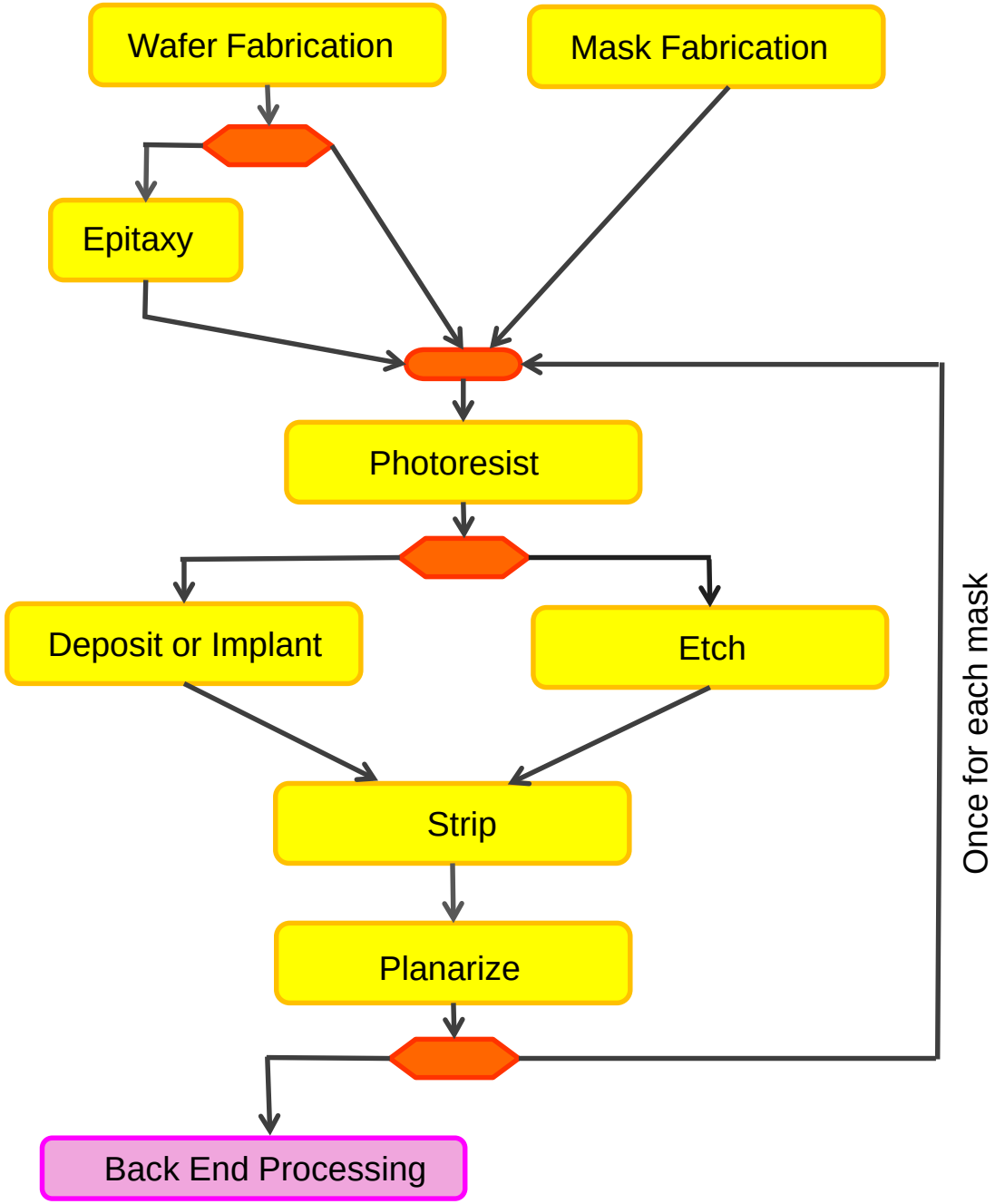




Generic Process Flow



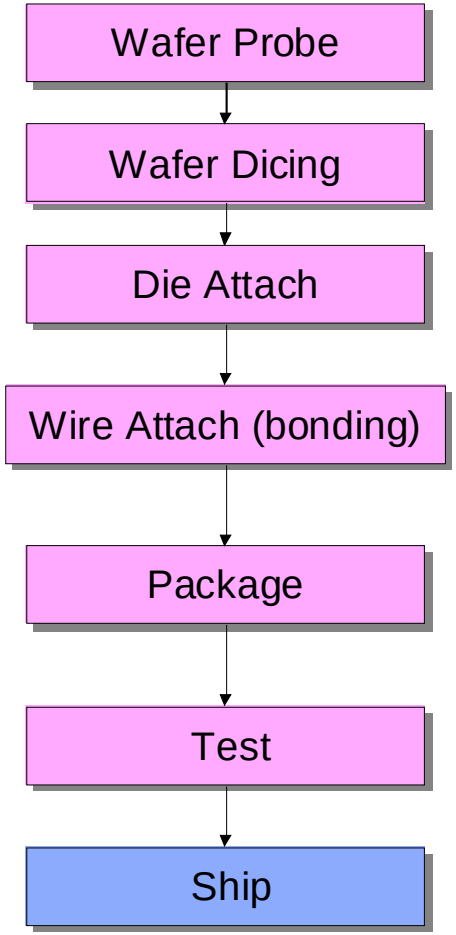
Front End Process Integration for Fabrication of ICs



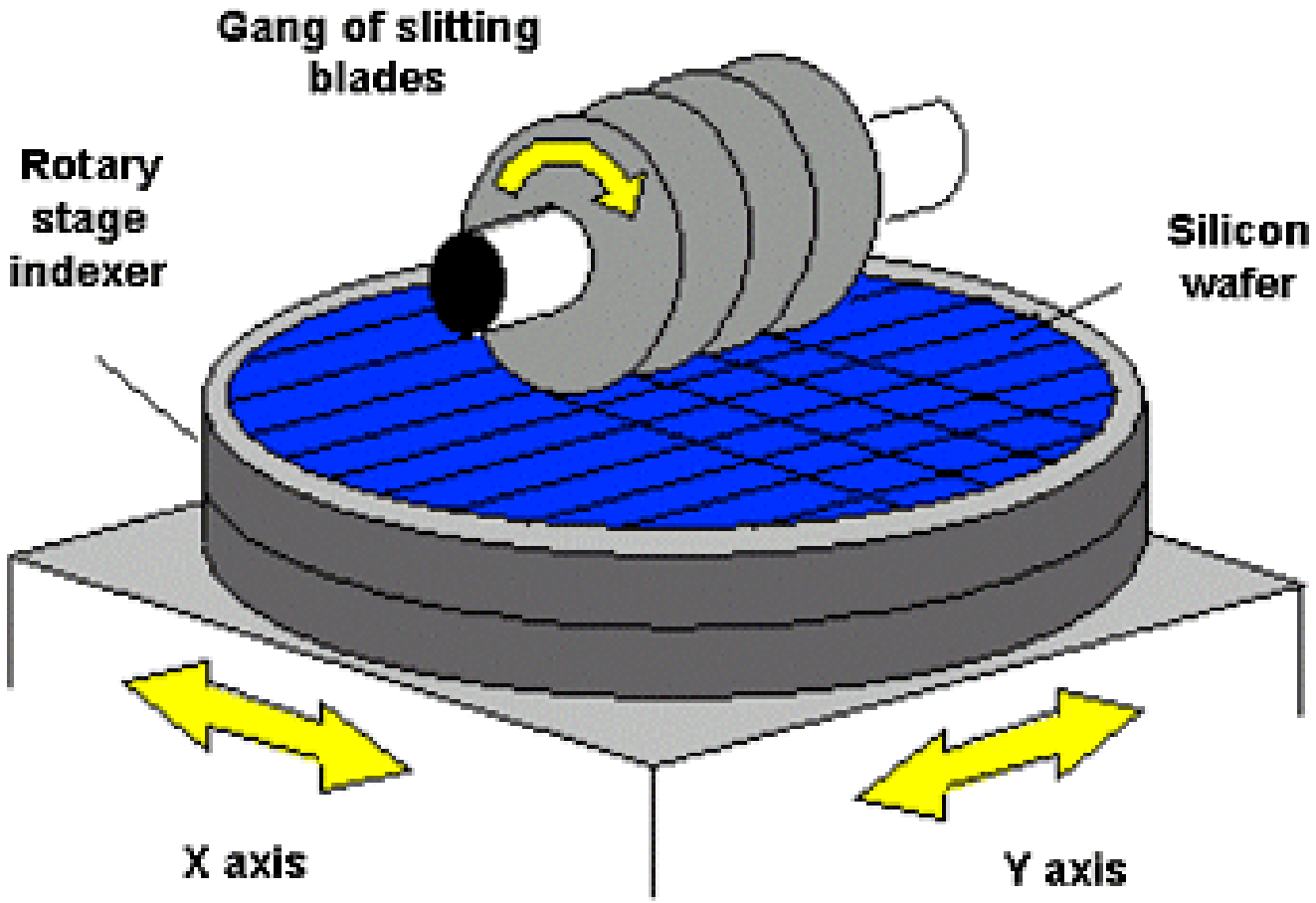
Front-End Process Flow

- Front-end processing steps analogous to a “recipe” for manufacturing an integrated circuit
- Recipes vary from one process to the next but the same basic steps are used throughout the industry
- Details of the recipe are generally considered proprietary

Back-End Process Flow



Wafer Dicing



www.renishaw.com

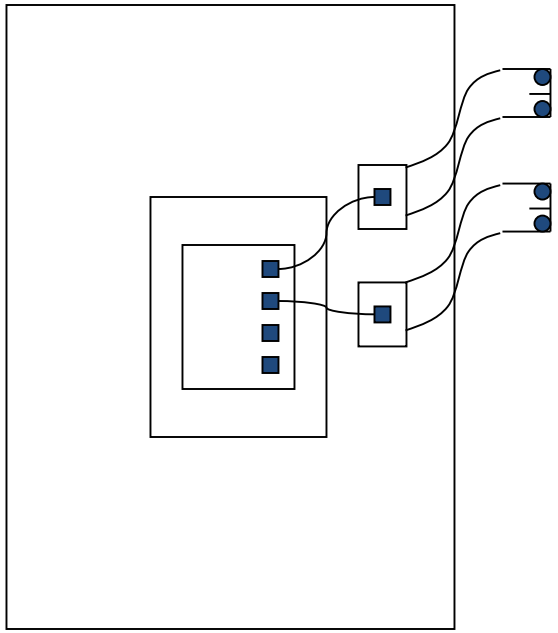
Die Attach

1. Eutectic
2. Pre-form
3. Conductive Epoxy

Electrical Connections (Bonding)

- Wire Bonding
- Bump Bonding

Wire Bonding



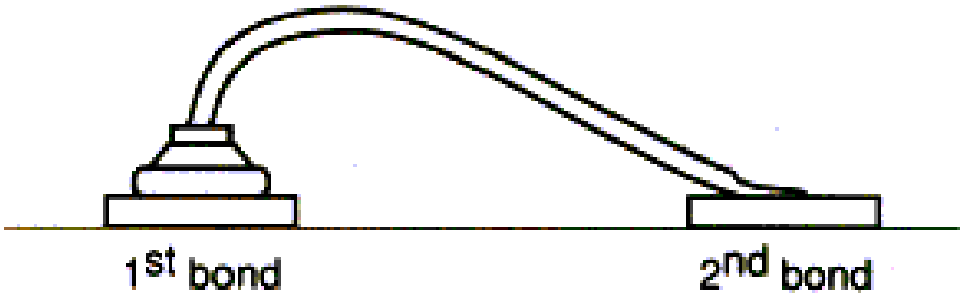
Wire – gold or aluminum
25 μ in diameter

Wire Bonding

Excellent Annimation showing process at :

http://www.kns.com/_Flash/CAP_BONDING_CYCLE.swf

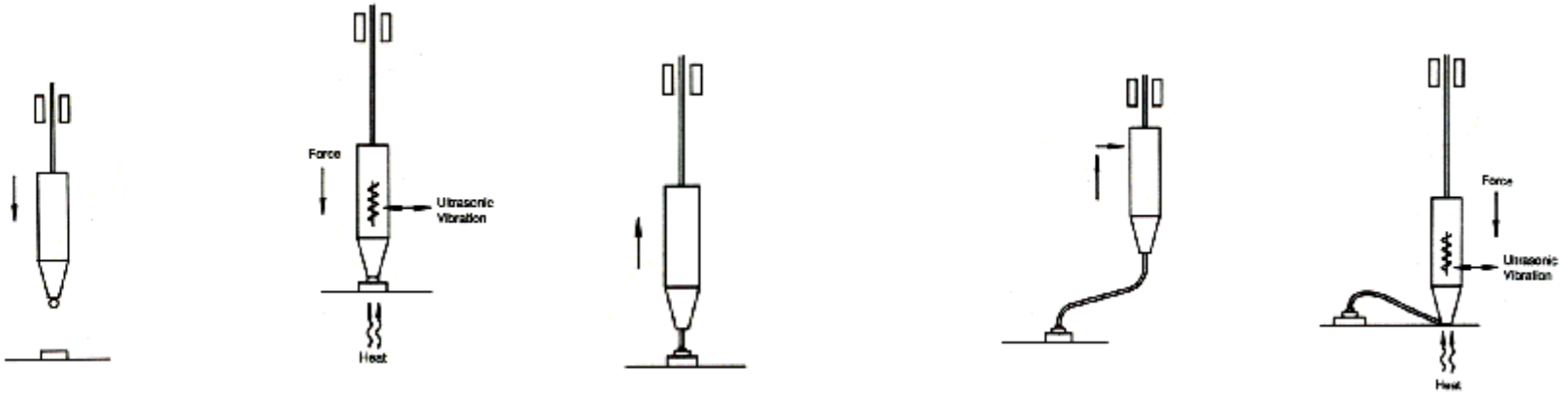
Wire Bonding



Ball Bond

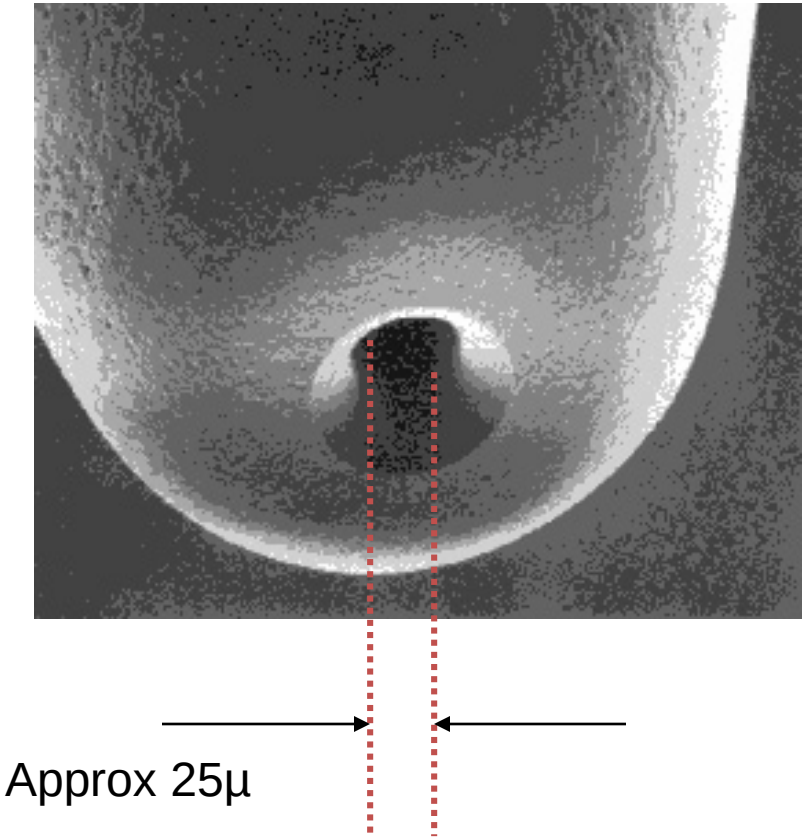
Wedge Bond

Ball Bonding Steps



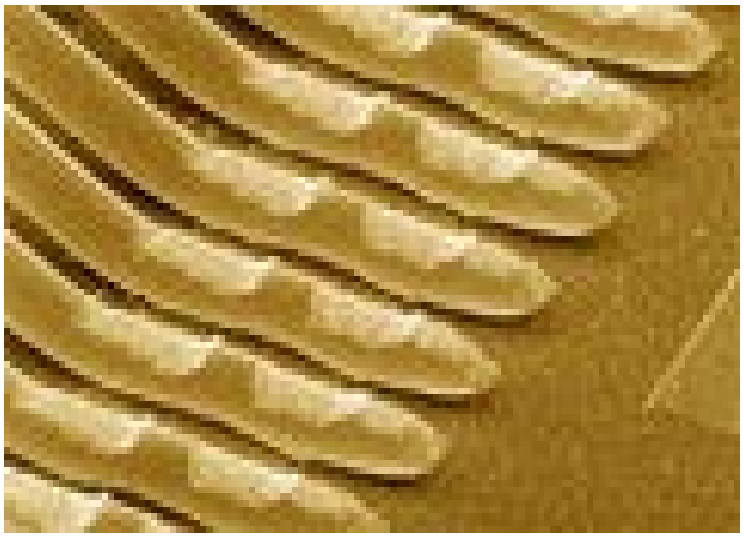
www.kns.com

Ball Bonding Tip

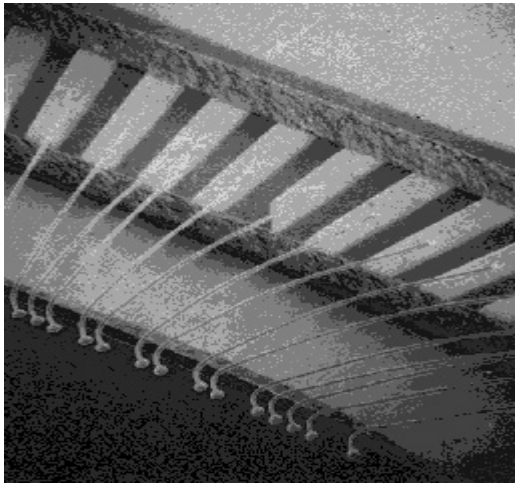


Wire Bonding

Ball Bond

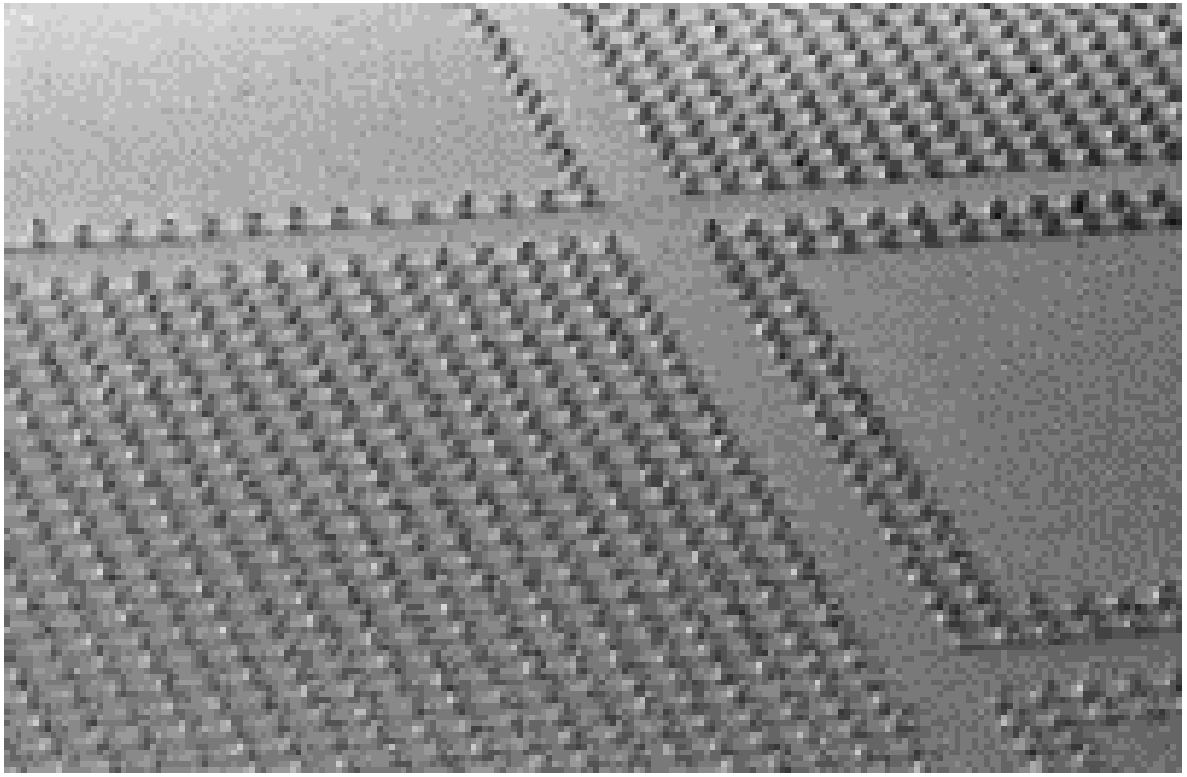


Termination Bond



Ball Bond Photograph

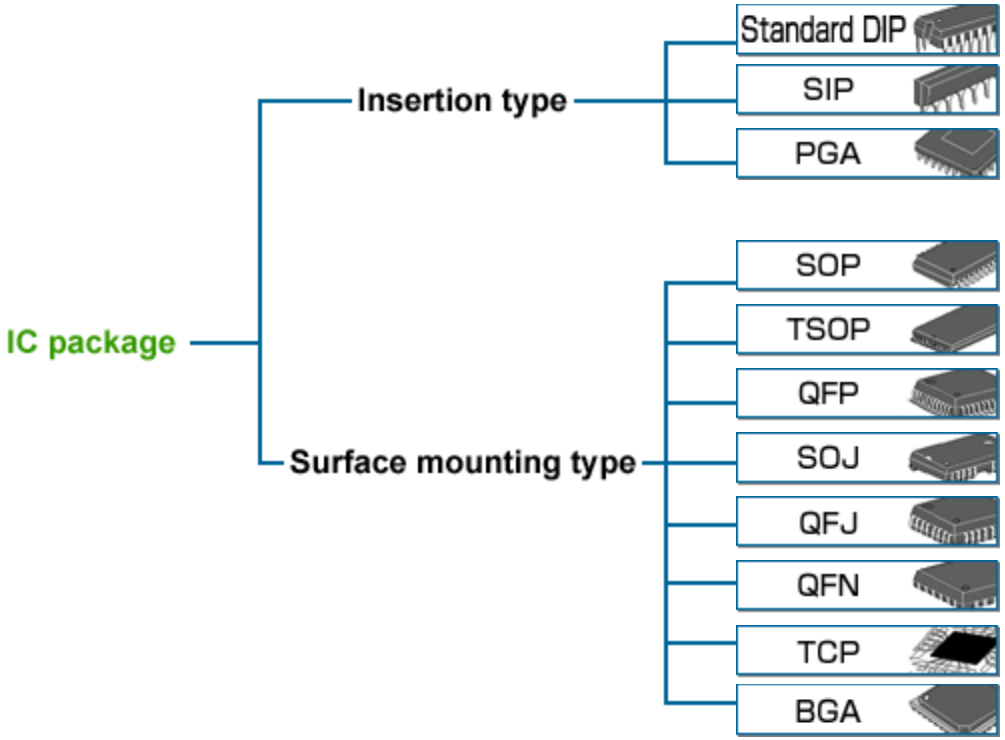
Bump Bonding



Packaging

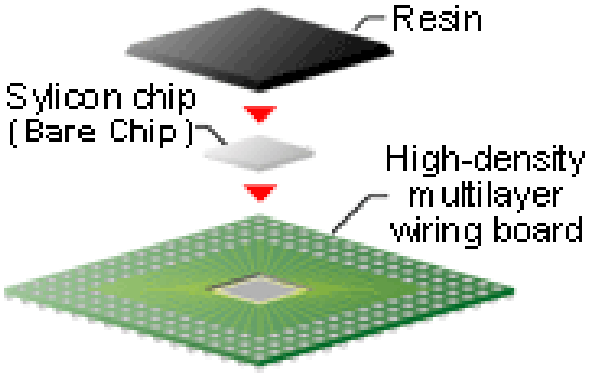
1. Many variants in packages now available
2. Considerable development ongoing on developing packaging technology
3. Cost can vary from few cents to tens of dollars
4. Must minimize product loss after packaged
5. Choice of package for a product is serious business
6. Designer invariably needs to know packaging plans and package models

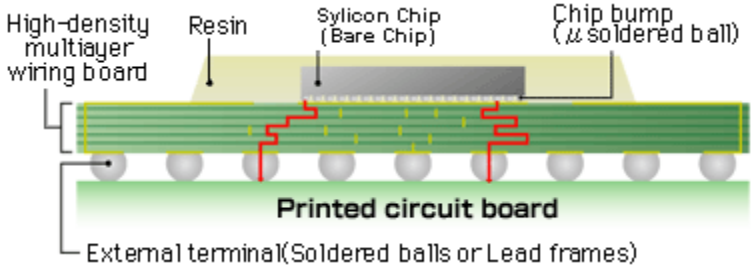
Packaging



www.necel.com

Packaging



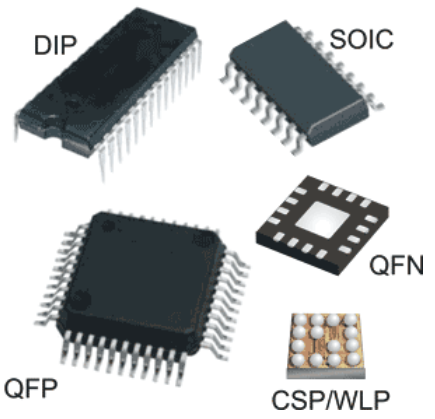


www.necel.com

Pin Pitch Varies with Package Technology

All measurements are nominal in [mm].

Name	Pin pitch	Size	Height
DIP or DIL	2.54		
SOIC-16	1.27	3.9 x 10	1.72
SSOP	0.635		
TSSOP54-II	0.8	12.7 x 22.22	~1
PLCC44	1.27		
PQ208[1]	0.50	28 x 28	3.4
TQFP64	0.40	7 x 7	1.0
TQFP144[2]	0.50	20 x 20	1.0
128PQFP	0.50	23.23 x 14.0	3.15



http://www.electroiq.com/index/display/packaging-article-display/234467/articles/advanced-packaging/volume-14/issue-8/features/the-back-end-process/materials-and-methods-for-ic-package-assemblies.htm

From Wikipedia, Sept 20, 2010

http://en.wikipedia.org/wiki/List_of_chip_carriers

Many standard packages available today:

http://www.interfacebus.com/Design_Pack_types.html

BCC: Bump Chip Carrier
BGA: Ball Grid Array; BGA graphic
BQFP: Bumpered Quad Flat Pack
CABGA/SSBGA: Chip Array/Small Scale Ball Grid Array
CBGA: Ceramic Ball Grid Array
CFP: Ceramic Flat Pack
CPGA: Ceramic Pin Grid Array, CPGA Graphic
CQFP: Ceramic Quad Flat Pack, CQFP Graphic
TBD: Ceramic Lead-Less Chip Carrier
DFN: Dual Flat Pack, No Lead
DLCC: Dual Lead-Less Chip Carrier (Ceramic)
ETQFP: Extra Thin Quad Flat Package
FBGA: Fine-pitch Ball Grid Array
fpBGA: Fine Pitch Ball Grid Array
HSBGA: Heat Slug Ball Grid Array
JLCC: J-Leaded Chip Carrier (Ceramic) J-Lead Picture
LBGA: Low-Profile Ball Grid Array
LCC: Leaded Chip Carrier LCC Graphic
LCC: Leaded Chip Carrier Un-formed LCC Graphic
LCCC: Leaded Ceramic Chip Carrier;
LFBGA: Low-Profile, Fine-Pitch Ball Grid Array
LGA: Land Grid Array, LGA uP [Pins are on the Motherboard, not the socket]
LLCC: Leadless Leaded Chip Carrier LLCC Graphic
LQFP: Low Profile Quad Flat Package
MCMBGA: Multi Chip Module Ball Grid Array
MCMCABGA: Multi Chip Module-Chip Array Ball Grid Array
MLCC: Micro Lead-frame Chip Carrier

PBGA: Plastic Ball Grid Array
PLCC: Plastic Leaded Chip Carrier
PQFD: Plastic Quad Flat Pack
PQFP: Plastic Quad Flat Pack
PSOP: Plastic Small-Outline Package PSOP graphic
QFP: Quad Flatpack QFP Graphics
QSOP: Quarter Size Outline Package [Quarter Pitch Small Outline Package]
SBGA: Super BGA - above 500 Pin count
SOIC: Small Outline IC
SO Flat Pack: Small Outline Flat Pack IC
SOJ: Small-Outline Package [J-Lead]; J-Lead Picture
SOP: Small-Outline Package; SOP IC, Socket
SSOP: Shrink Small-Outline Package
TBGA: Thin Ball Grid Array
TQFP: Thin Quad Flat Pack TQFP Graphic
TSOP: Thin Small-Outline Package
TSSOP: Thin Shrink Small-Outline Package
TVSOP: Thin Very Small-Outline Package
VQFB: Very-thin Quad Flat Pack

Considerable activity today and for years to come on improving packaging technology

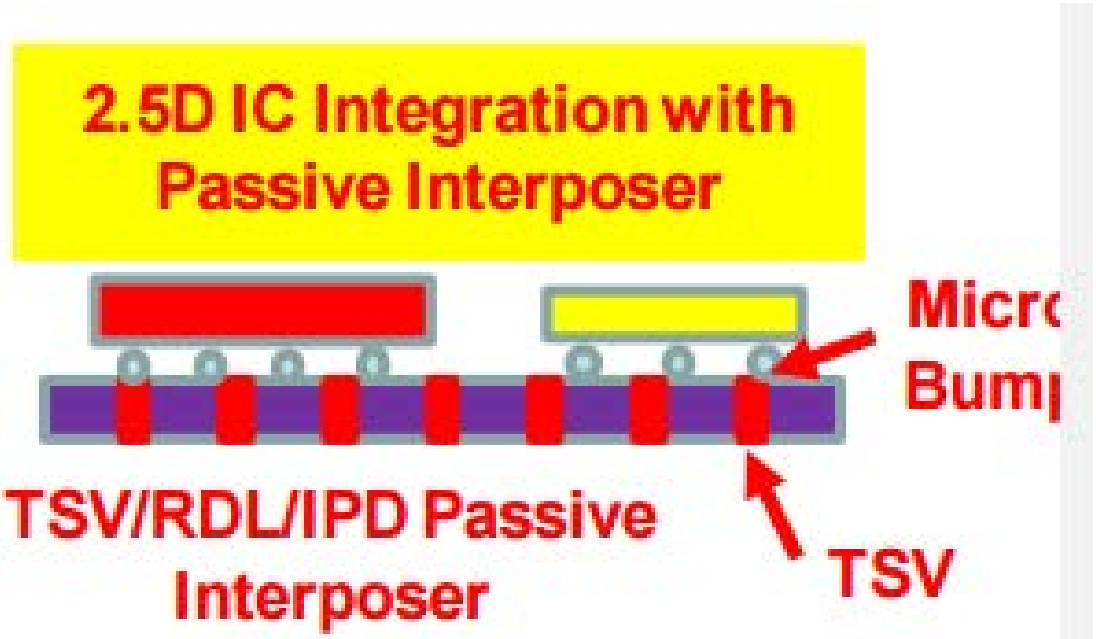
- Multiple die in a package
- Three-dimensional chip stacking
- Multiple levels of interconnect in stacks
- Through silicon via technology
- Power and heat management
- Cost driven and cost constrained

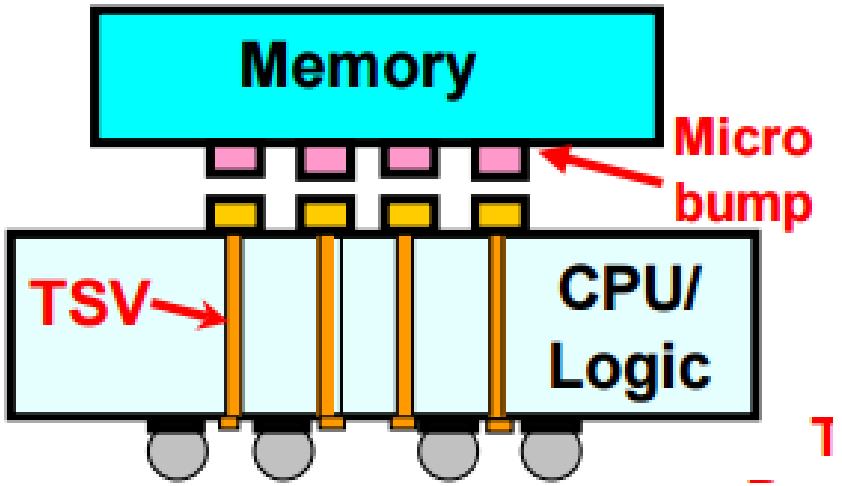
The following few slides come from a John Lau presentation

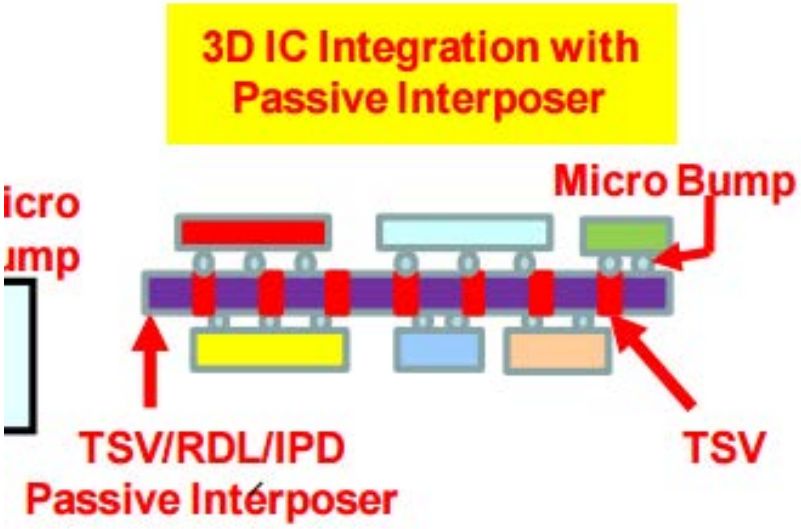
www.sematech.org/meetings/archives/symposia/10187/Session2/04_Lau.pdf

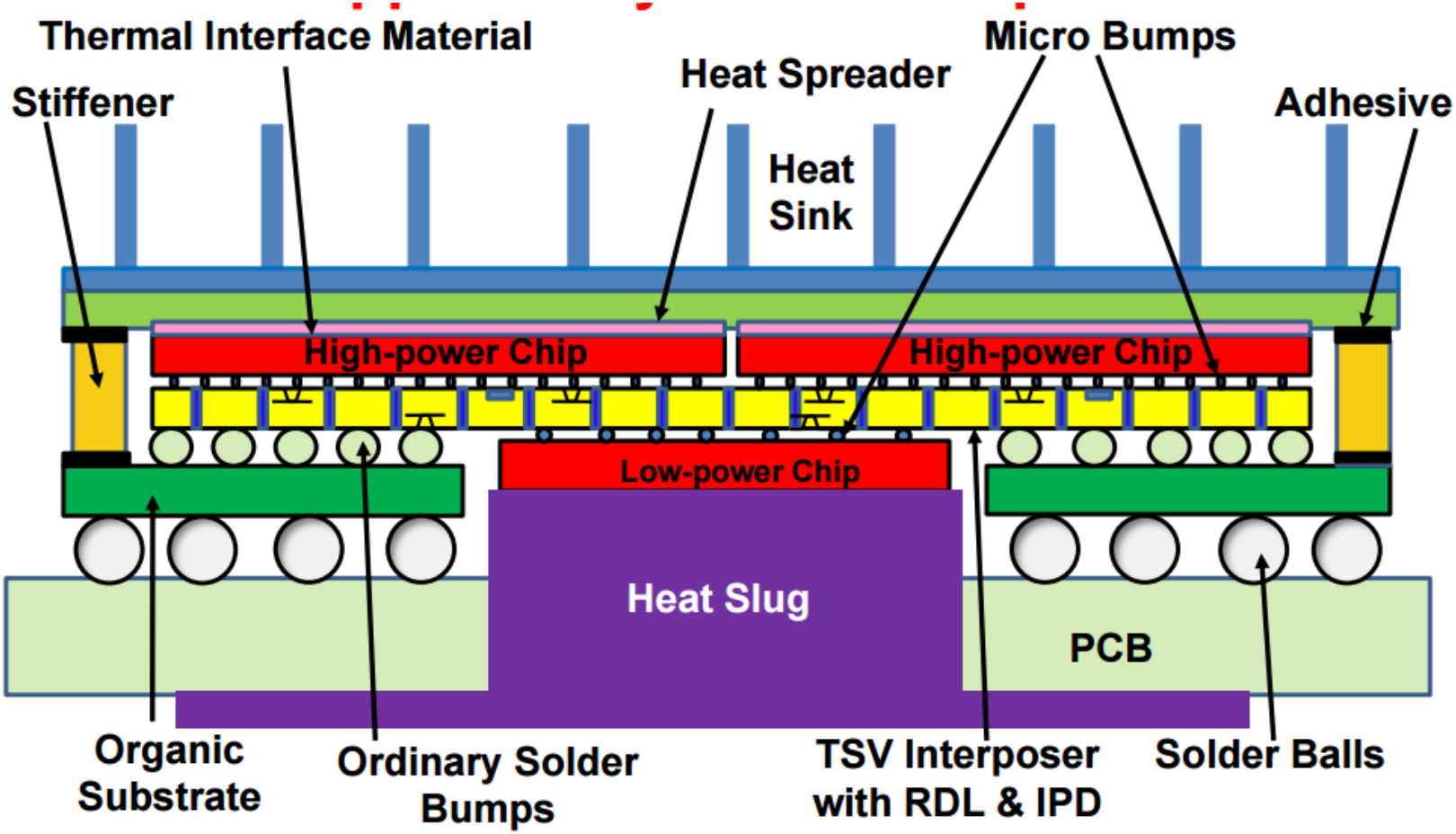
TSV Interposer: The Most Cost-Effective Integrator for 3D IC Integration

John H. Lau
Electronics & Optoelectronics Research Laboratories
Industrial Technology Research Institute (ITRI)
Chutung, Hsinchu, Taiwan 310, R.O.C.
886-3591-3390, johnlau@itri.org.tw

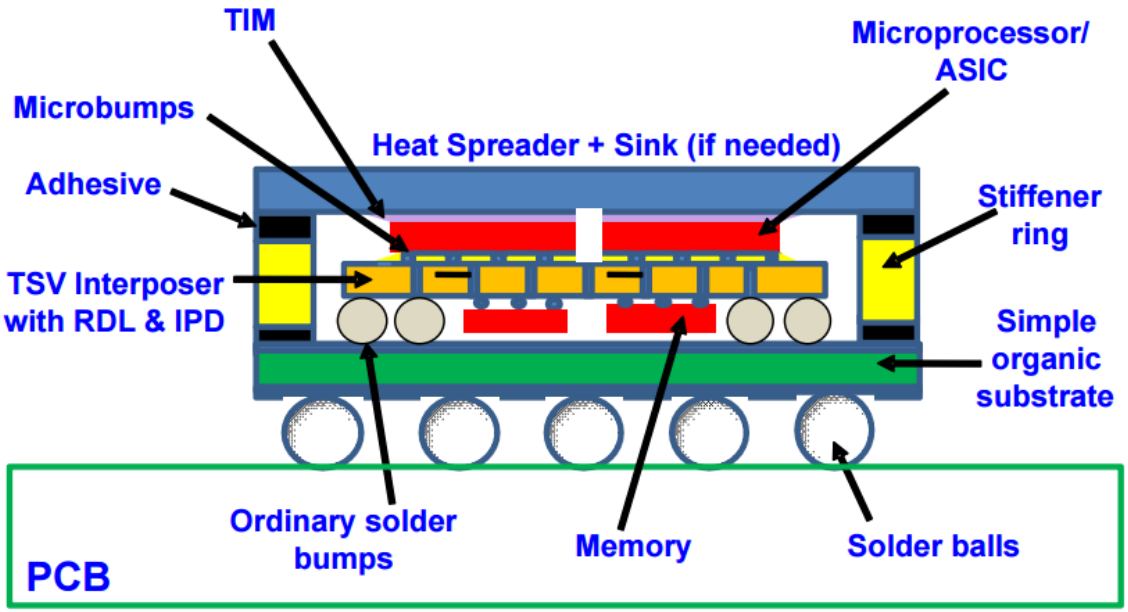

2.5D IC Integration with Passive Interposer
Micro Bump
TSV/RDL/IPD Passive Interposer
TSV


Memory
Micro
bump
TSV
CPU/
Logic


3D IC Integration with
Passive Interposer
Micro Bump
TSV/RDL/IPD
Passive Intérposer
TSV

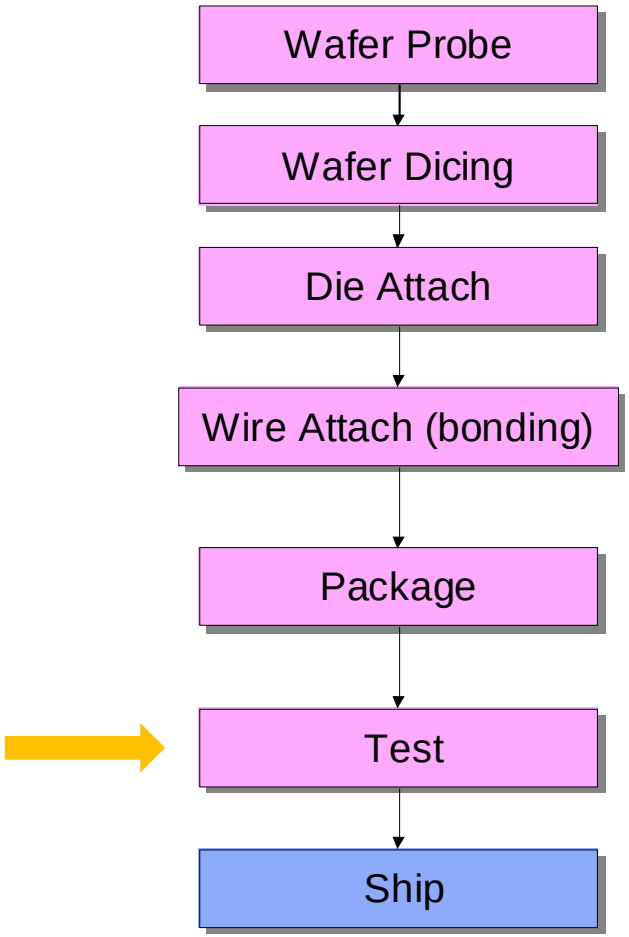

Thermal Interface Material
Stiffener
Heat Spreader
Micro Bumps
Adhesive
Heat
Sink
High-power Chip
High-power Chip
Low-power Chip
Heat Slug
PCB
Organic
Substrate
Ordinary Solder
Bumps
TSV Interposer
with RDL & IPD
Solder Balls

TSV passive interposer supporting high-power chips (e.g., microprocessor and logic) on its top side and low-power chips (e.g., memory) on its bottom side



Special underfills are needed between the Cu -filled interposer and all the chips. Ordinary underfills are needed between the interposer and the organic substrate.

Back-End Process Flow



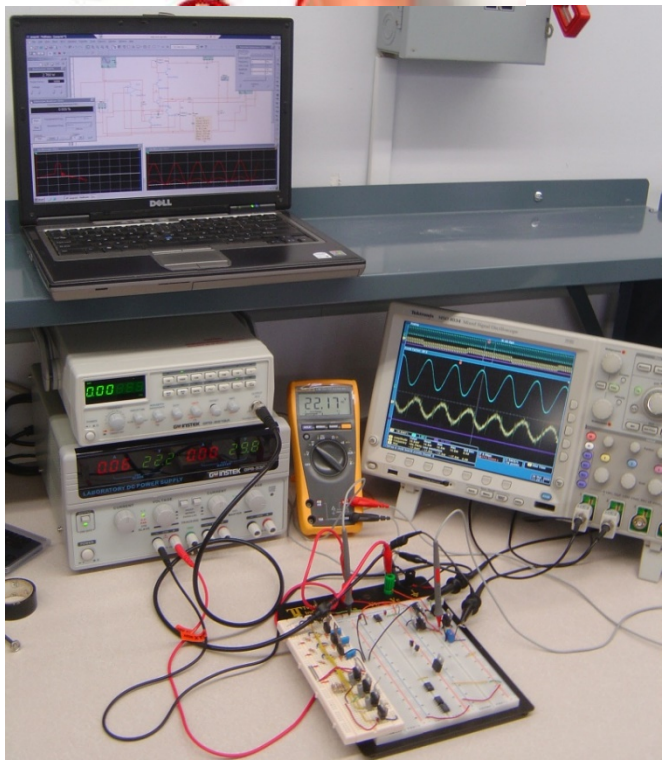
Testing of Integrated Circuits

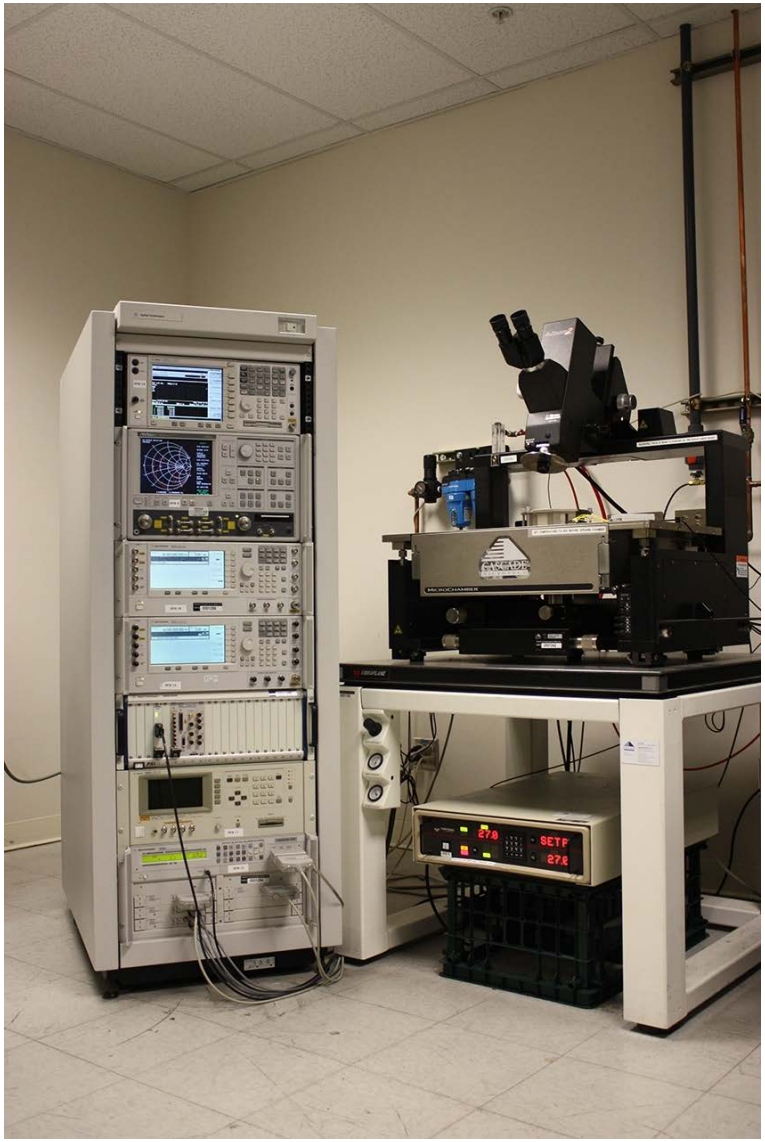
Bench testing used to qualify parts for production

Most integrated circuits are tested twice during production

- Wafer Probe Testing
  - Quick test for functionality
  - Usually does not include much parametric testing
  - Relatively fast and low cost test
  - Package costs often quite large
  - Critical to avoid packaging defective parts
- Packaged Part Testing
  - Testing costs for packaged parts can be high
  - Extensive parametric tests done at package level for many parts
  - Data sheet parametrics with Max and Min values are usually tested on all Ics
  - Data sheet parametrics with Typ values are seldom tested
  - Occasionally require testing at two or more temperatures but this is costly
  - Critical to avoid packaging defective parts

Bench Test Environment



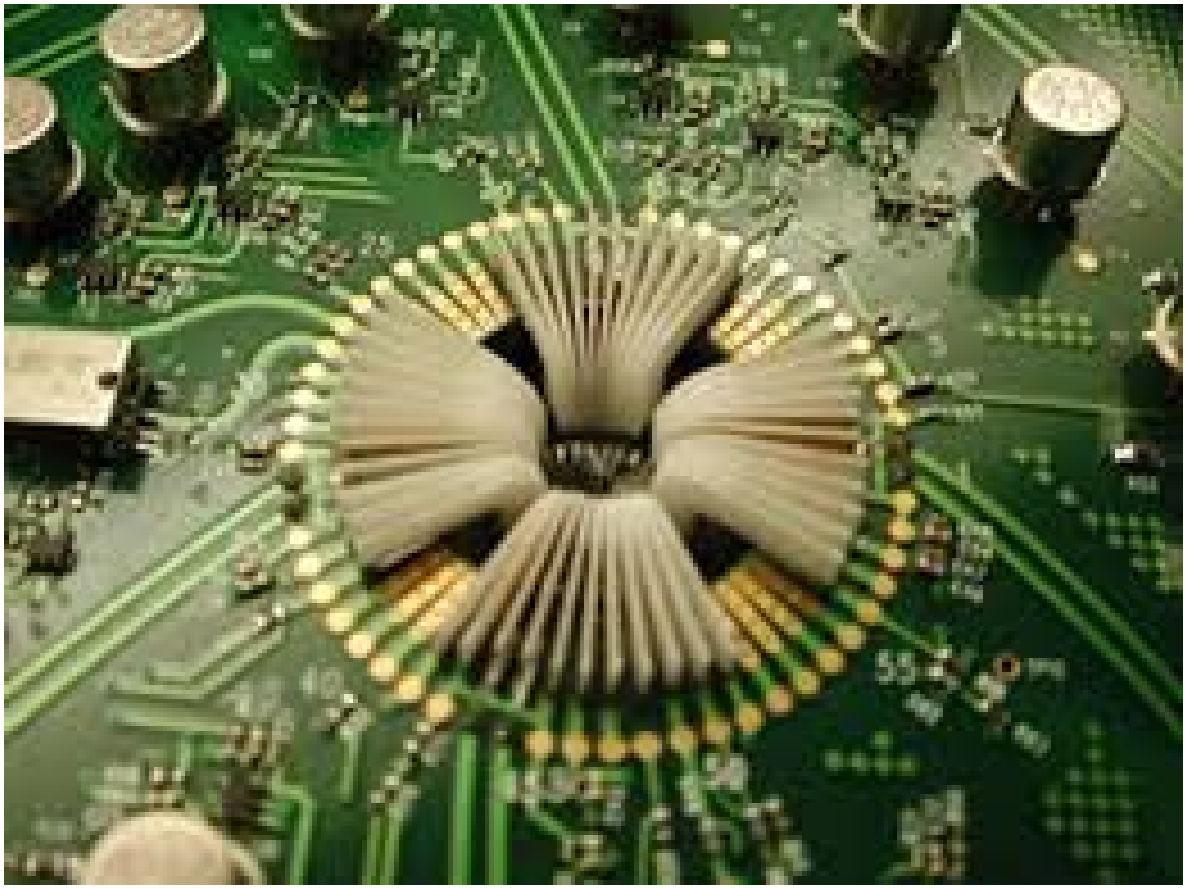


Photos from www postings and Google image search

Bench Test Environment

Photo courtesy of Texas Instruments

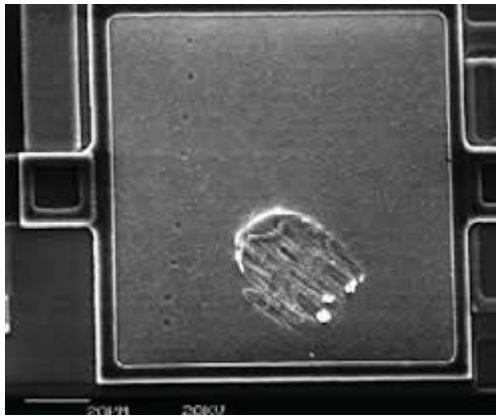
Probe Test



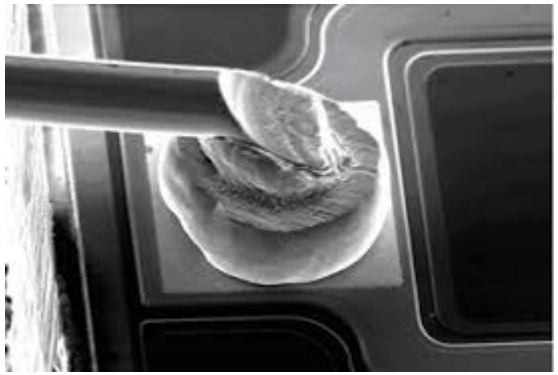
Probes on section of probe card

Photos from www postings and Google image search

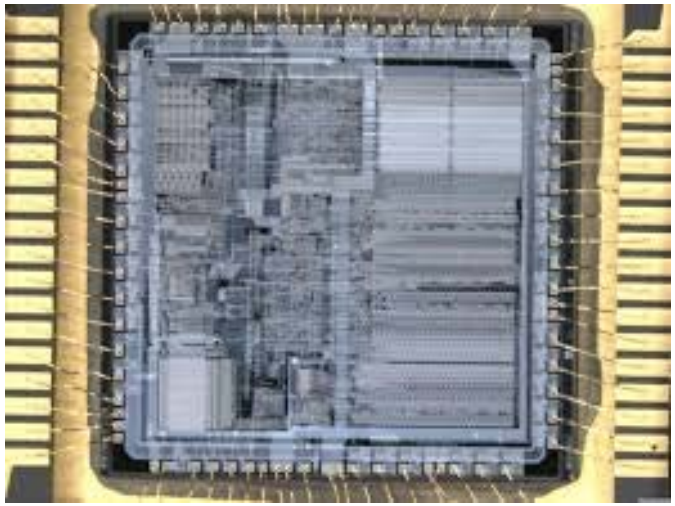
Probe Test



Pad showing probe marks



Pad showing bonding wire



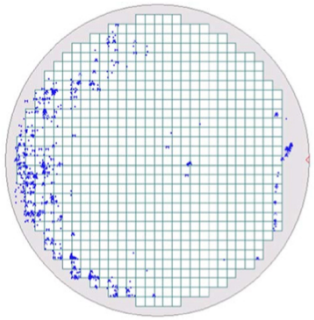
Die showing wire bonds to package cavity

Photos from www postings and Google image search

Probe Test

Production probe test facility

Goal to Identify
defective die on wafer



Photos from www postings and Google image search

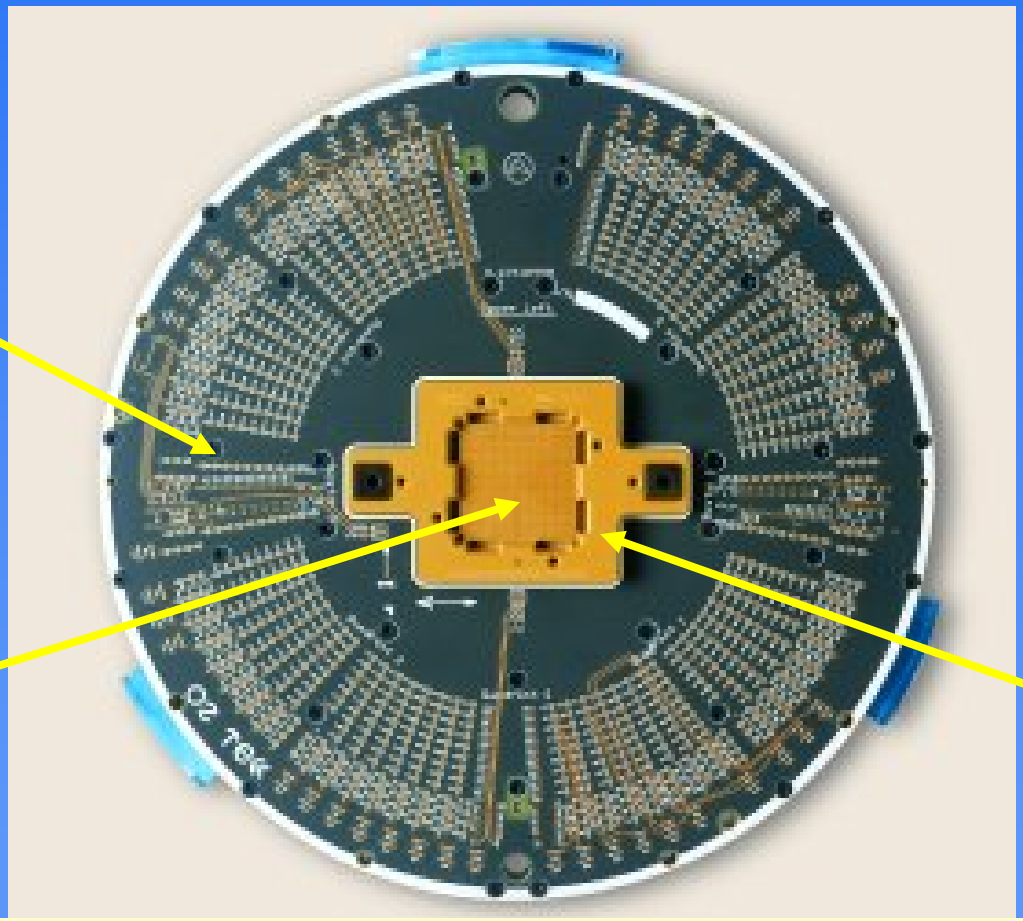
Final Test

Typical ATE System (less handler)

Automated Test Equipment (ATE)

Device Interface Board - DIB

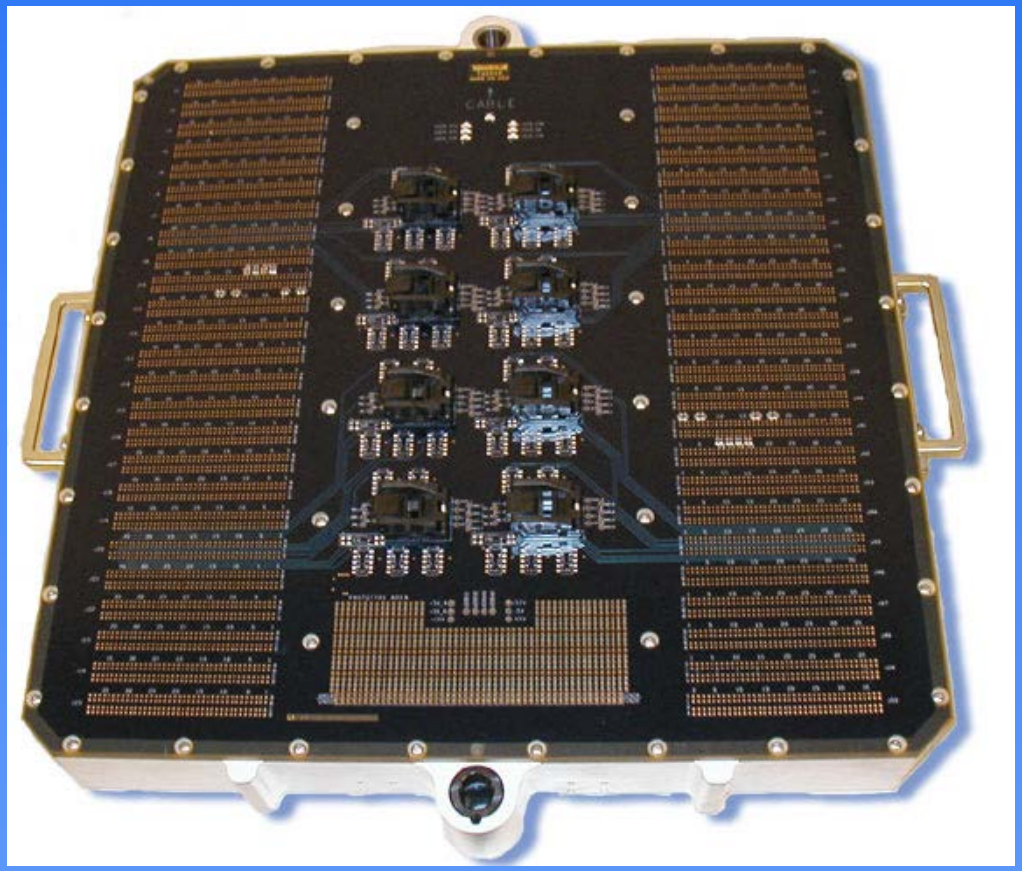
(Load Board)



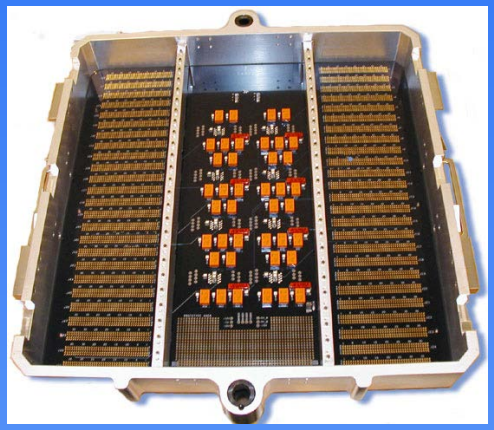
DIBs Vary Considerably from one ATE Platform to another and are often personalized for a particular DUT

Octal Site DIB

Flex Octal (Teradyne)



Top



Bottom

Final Test

Typical ATE Configuration

Handler

Tester

Test Head

Atlas (SSI Robotics)

End of Lecture 11