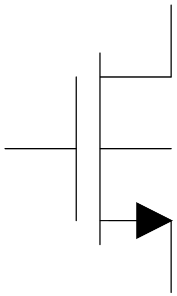
EE 330
Lecture 17

MOSFET Modeling
CMOS Process Flow

Model Extension Summary

$$\mathbf{I_G = 0}$$

$$\mathbf{I_B = 0}$$



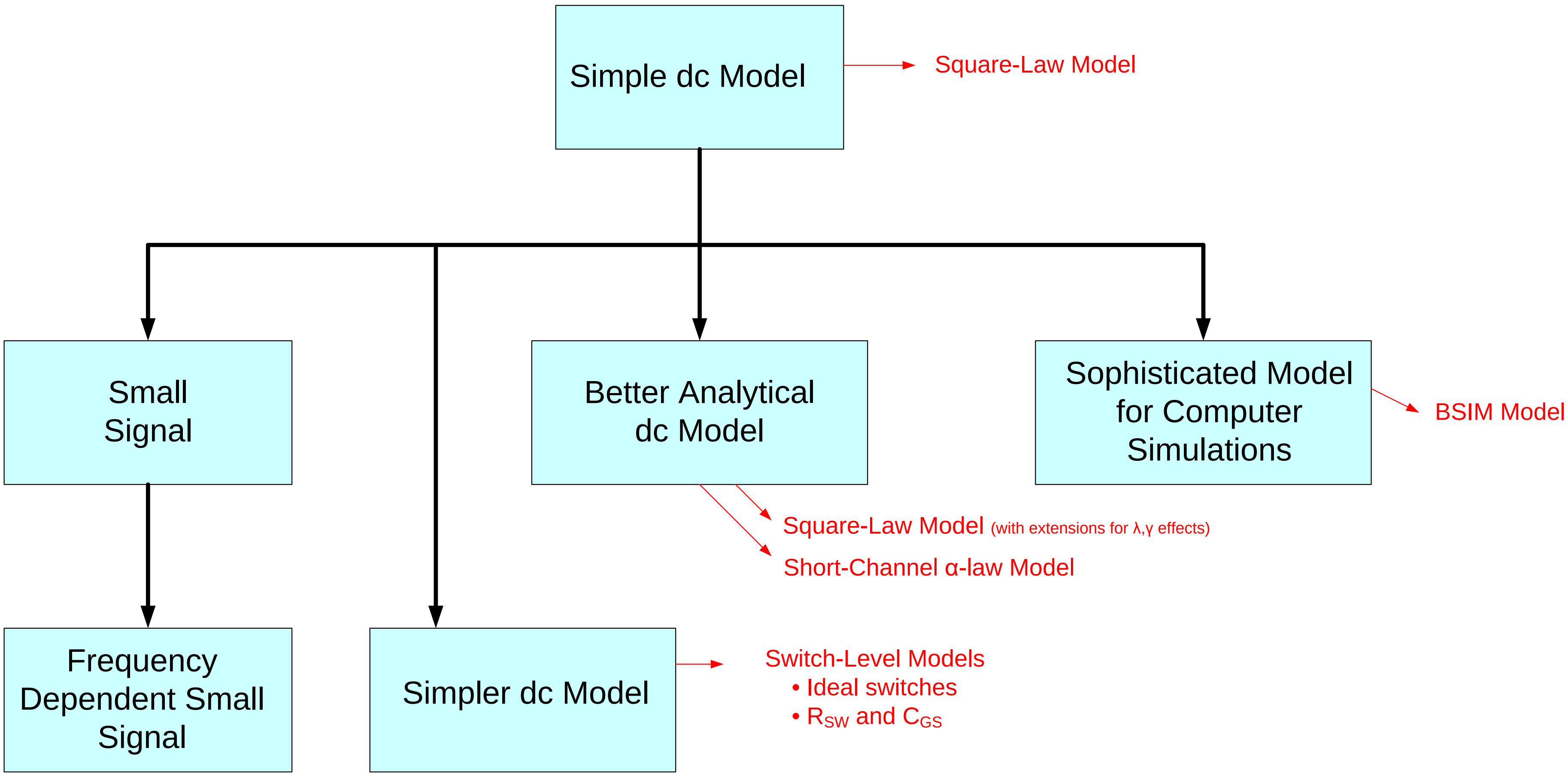
$$I_D = \begin{cases} 0 & V_{GS} \le V_T \\ \mu C_{OX} \dfrac{W}{L}\left(V_{GS} - V_T - \dfrac{V_{DS}}{2}\right)V_{DS} & V_{GS} \ge V_T \quad V_{DS} < V_{GS} - V_T \\ \mu C_{OX} \dfrac{W}{2L}\left(V_{GS} - V_T\right)^2 \bullet \left(1 + \lambda V_{DS}\right) & V_{GS} \ge V_T \quad V_{DS} \ge V_{GS} - V_T \end{cases}$$

$$V_T = V_{T0} + \gamma\left(\sqrt{\phi - V_{BS}} - \sqrt{\phi}\right)$$

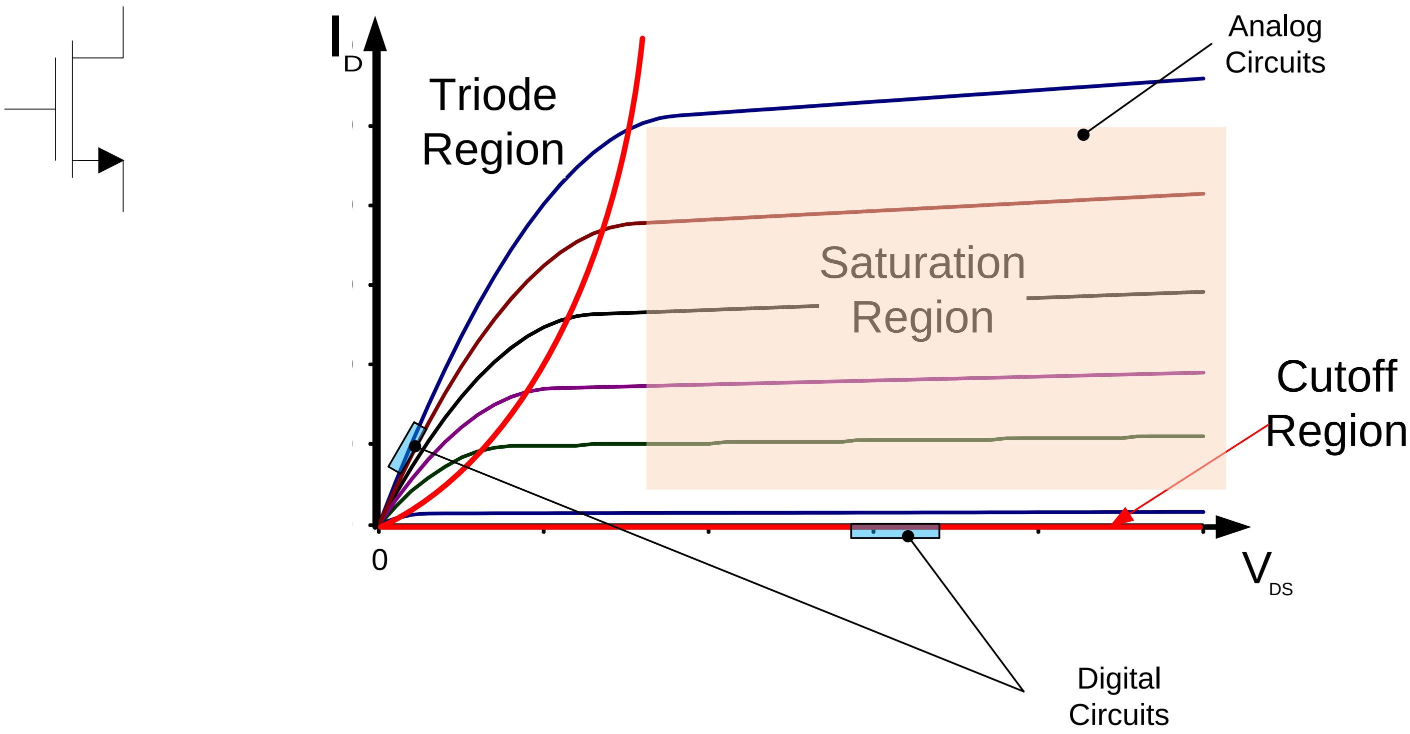
Model Parameters : $\{\mu, C_{OX}, V_{T0}, \varphi, \gamma, \lambda\}$

Design Parameters : {W,L}   but only one degree of freedom W/L

Model Status



Operation Regions by Applications

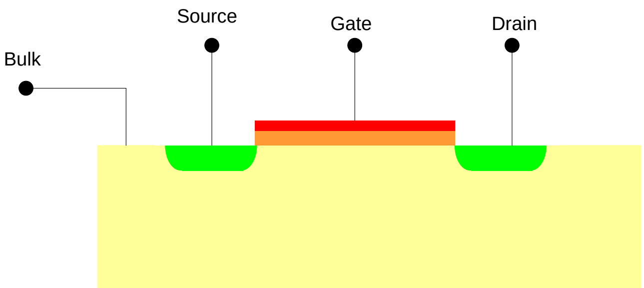


Most analog circuits operate in the saturation region

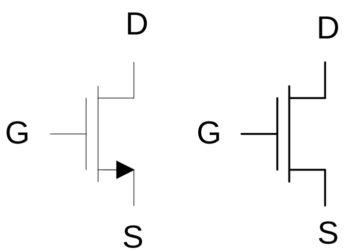
(basic VVR operates in triode and is an exception)

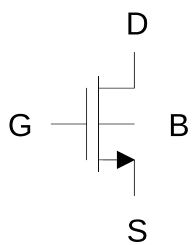
Most digital circuits operate in triode and cutoff regions and switch between these two with Boolean inputs

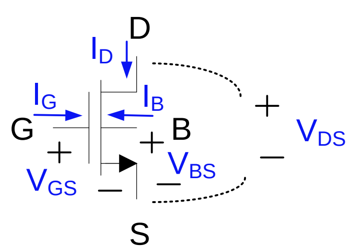
n-channel …. p-channel modeling

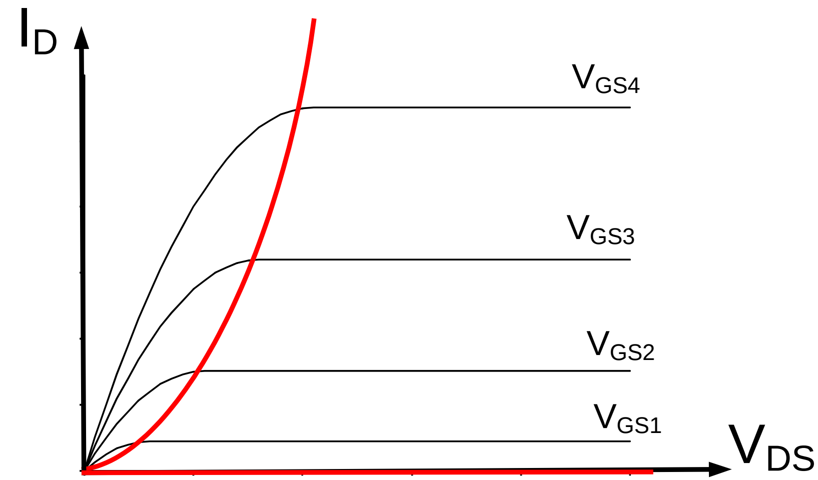


n-channel MOSFET









$V_{GS4} > V_{GS3} > V_{GS2} > V_{GS1} > 0$

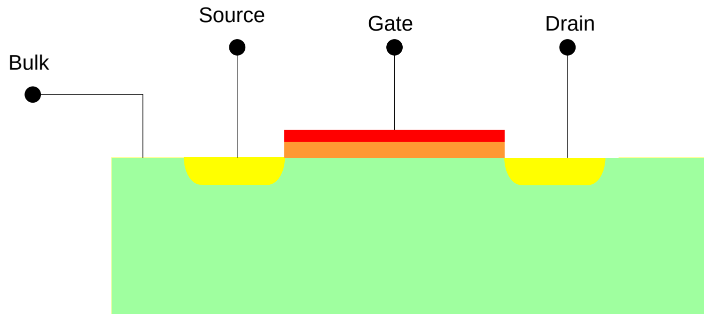
(for enhancement devices)

$$I_D = \begin{cases} 0 & V_{GS} \le V_{Tn} \\ \mu_n C_{OX} \dfrac{W}{L}\left(V_{GS} - V_{Tn} - \dfrac{V_{DS}}{2}\right)V_{DS} & V_{GS} \ge V_{Tn} \quad V_{DS} < V_{GS} - V_{Tn} \\ \mu_n C_{OX} \dfrac{W}{2L}\left(V_{GS} - V_{Tn}\right)^2 & V_{GS} \ge V_{Tn} \quad V_{DS} \ge V_{GS} - V_{Tn} \end{cases}$$

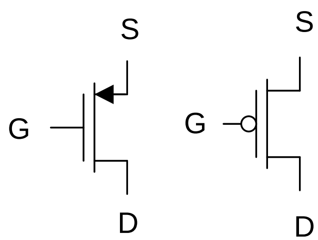
$I_G = I_B = 0$

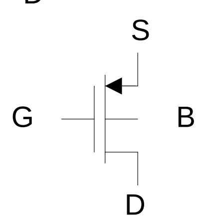
Positive V_{DS} and V_{GS} cause a positive I_D

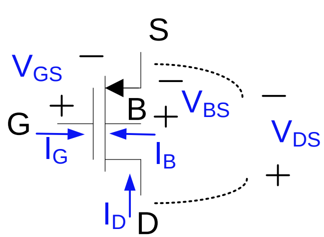
n-channel …. p-channel modeling

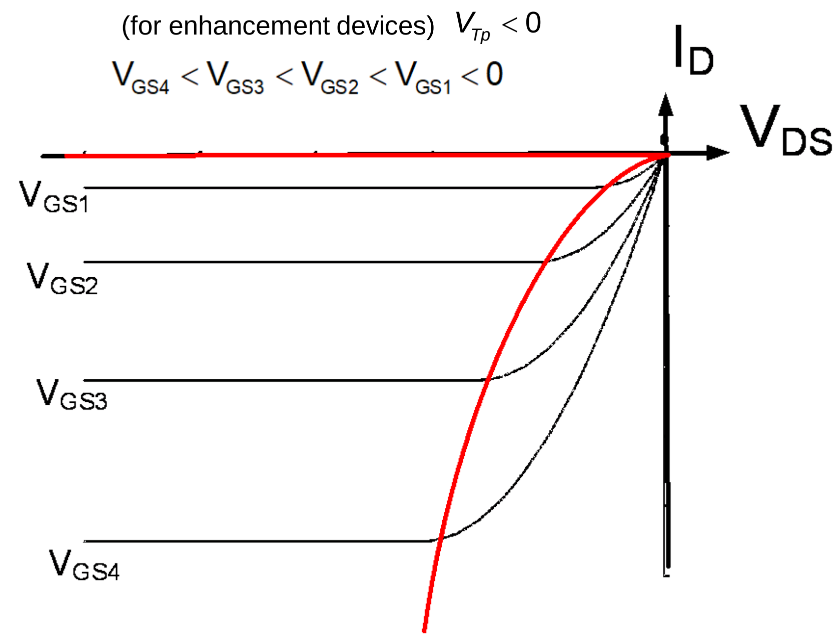


p-channel MOSFET









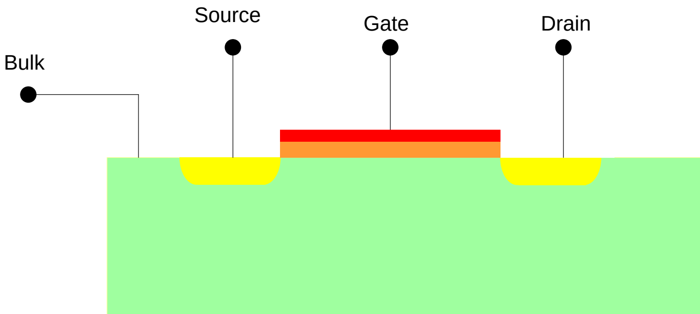
$$I_D = \begin{cases} 0 & V_{GS} \geq V_{Tp} \\ -\mu_p C_{OX} \dfrac{W}{L}\left(V_{GS} - V_{Tp} - \dfrac{V_{DS}}{2}\right)V_{DS} & V_{GS} \leq V_{Tp} \quad V_{DS} > V_{GS} - V_{Tp} \\ -\mu_p C_{OX} \dfrac{W}{2L}\left(V_{GS} - V_{Tp}\right)^2 & V_{GS} \leq V_{Tp} \quad V_{DS} \leq V_{GS} - V_{Tp} \end{cases}$$

$$I_G = I_B = 0$$

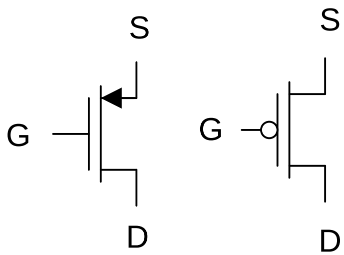
Negative V_{DS} and V_{GS} cause a negative I_D

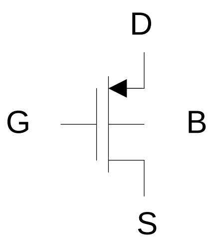
Functional form of models are the same, just sign differences and some parameter differences (usually mobility is the most important)

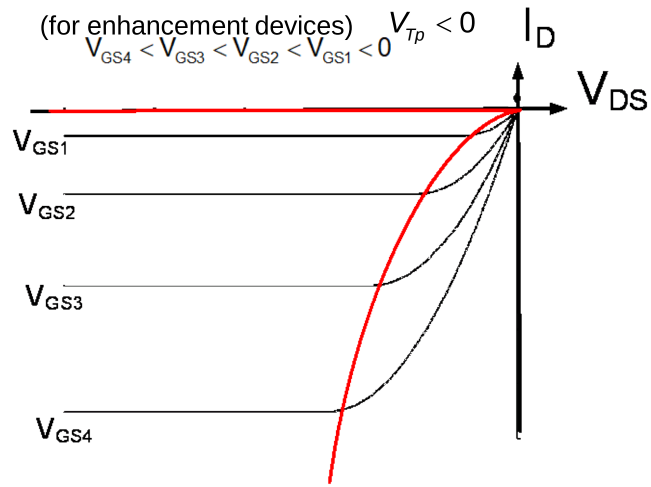
n-channel …. p-channel modeling



p-channel MOSFET

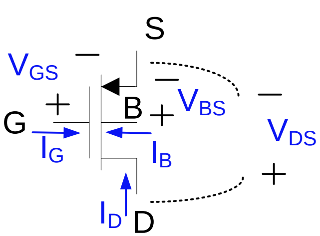


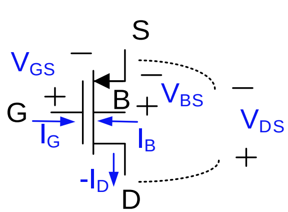




$$
I_D = \begin{cases} 0 & V_{GS} \geq V_{Tp} \\ -\mu_p C_{OX} \dfrac{W}{L}\left(V_{GS} - V_{Tp} - \dfrac{V_{DS}}{2}\right)V_{DS} & V_{GS} \leq V_{Tp} \quad V_{DS} > V_{GS} - V_{Tp} \\ -\mu_p C_{OX} \dfrac{W}{2L}\left(V_{GS} - V_{Tp}\right)^2 & V_{GS} \leq V_{Tp} \quad V_{DS} \leq V_{GS} - V_{Tp} \end{cases}
$$

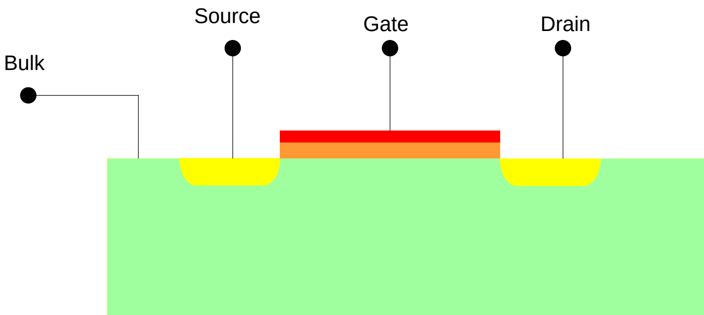
$I_G = I_B = 0$



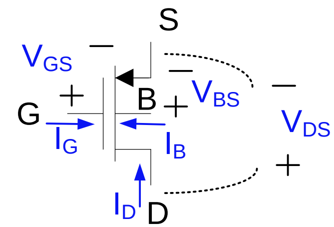


- Actually should use C_{OXp} and C_{OXn} but they are usually almost identical in most processes
- $\mu_n \approx 3\mu_p$
- May choose to model $-I_D$ which will be non-negative

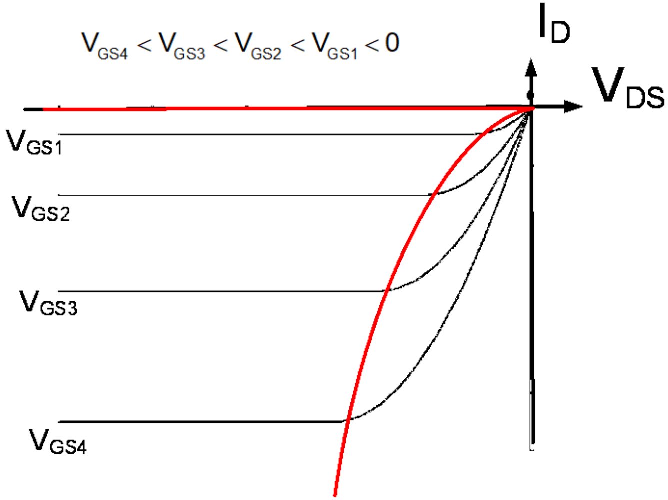
n-channel …. p-channel modeling



p-channel MOSFET



(for enhancement devices)



$$I_D = \begin{cases} 0 & V_{GS} \geq V_{Tp} \\ -\mu_p C_{OX} \dfrac{W}{L}\left(V_{GS} - V_{Tp} - \dfrac{V_{DS}}{2}\right)V_{DS} & V_{GS} \leq V_{Tp} \quad V_{DS} > V_{GS} - V_{Tp} \\ -\mu_p C_{OX} \dfrac{W}{2L}\left(V_{GS} - V_{Tp}\right)^2 & V_{GS} \leq V_{Tp} \quad V_{DS} \leq V_{GS} - V_{Tp} \end{cases}$$

$$I_G = I_B = 0$$

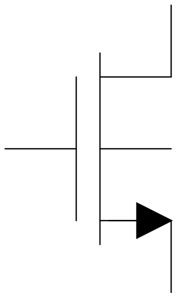
Alternate equivalent representation

$$|I_D| = \begin{cases} 0 & |V_{GS}| \leq |V_{Tp}| \\ \mu_p C_{OX} \dfrac{W}{L}\left(V_{GS} - V_{Tp} - \dfrac{V_{DS}}{2}\right)V_{DS} & |V_{GS}| \geq |V_{Tp}| \quad |V_{DS}| < |V_{GS} - V_{Tp}| \\ \mu_p C_{OX} \dfrac{W}{2L}\left(V_{GS} - V_{Tp}\right)^2 & |V_{GS}| \geq |V_{Tp}| \quad |V_{DS}| \geq |V_{GS} - V_{Tp}| \end{cases}$$

$$I_G = I_B = 0$$

These look like those for the n-channel device but with ||

Model Extension Summary



$$I_G = 0$$

$$I_B = 0$$

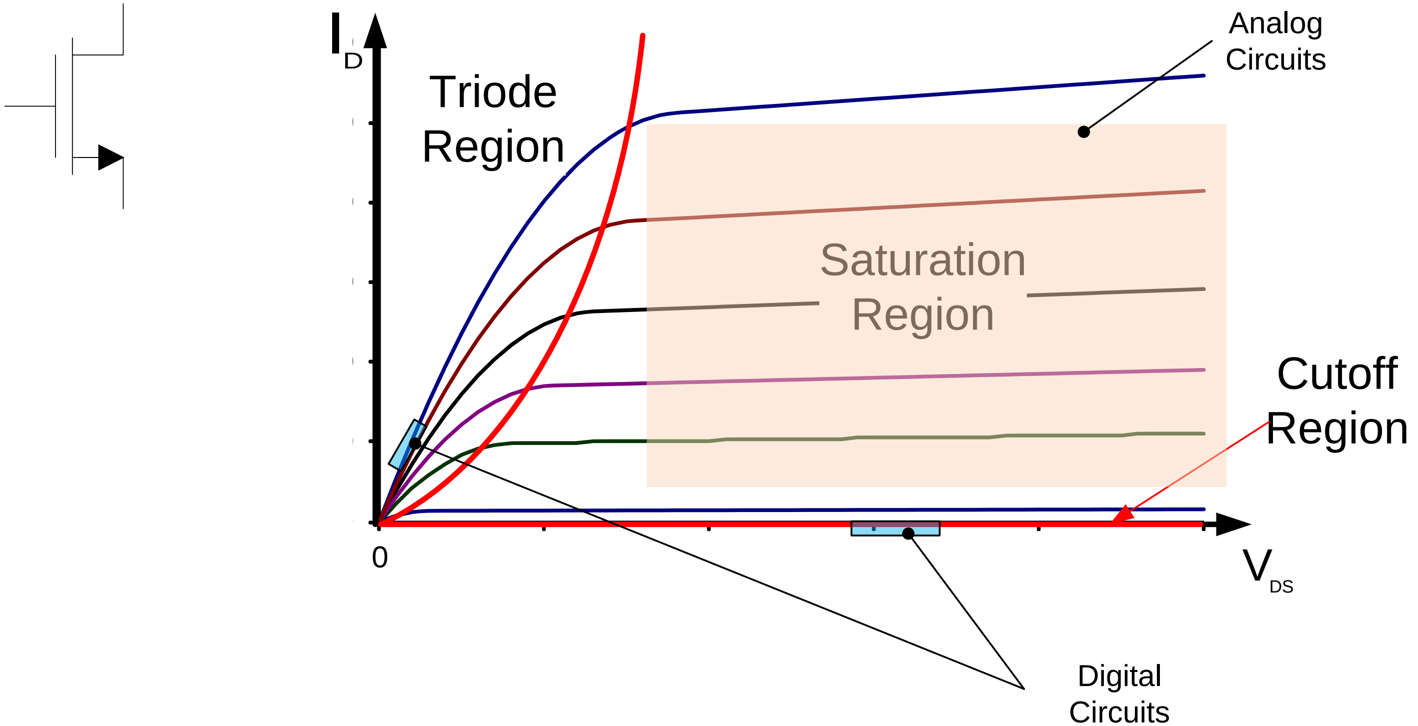
$$I_D = \begin{cases} 0 & V_{GS} \le V_T \\ \mu C_{OX} \dfrac{W}{L}\left(V_{GS} - V_T - \dfrac{V_{DS}}{2}\right)V_{DS} & V_{GS} \ge V_T \quad V_{DS} < V_{GS} - V_T \\ \mu C_{OX} \dfrac{W}{2L}\left(V_{GS} - V_T\right)^2 \bullet \left(1 + \lambda V_{DS}\right) & V_{GS} \ge V_T \quad V_{DS} \ge V_{GS} - V_T \end{cases}$$

$$V_T = V_{T0} + \gamma\left(\sqrt{\phi - V_{BS}} - \sqrt{\phi}\right)$$

Model Parameters : {μ,C_{OX},V_{T0},φ,γ,λ}

Design Parameters : {W,L}   but only one degree of freedom W/L

Operation Regions by Applications

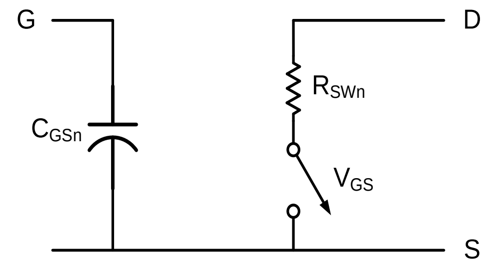


Most analog circuits operate in the saturation region

(basic VVR operates in triode and is an exception)

Most digital circuits operate in triode and cutoff regions and switch between these two with Boolean inputs

Model Relationships



Determine R_{SW} and C_{GS} for an n-channel MOSFET from square-law model in the 0.5u ON CMOS process if L=0.6u, W=0.9u

(Assume μC_{OX}=100μAV^{-2}, C_{OX}=2.5fFu^{-2}, V_{T0}=0.7V, V_{DD}=5V, V_{SS}=0)

When on operating in deep triode, V_high =0.8VDD = 4V

$$I_D = \mu C_{OX}\frac{W}{L}\left(V_{GS} - V_T - \frac{V_{DS}}{2}\right)V_{DS} \cong \mu C_{OX}\frac{W}{L}\left(V_{GS} - V_T\right)V_{DS}$$

$$R_{SQ} = \left.\frac{V_{DS}}{I_D}\right|_{V_{GS}=V_{DD}} = \left.\frac{1}{\mu C_{OX}\frac{W}{L}\left(V_{GS} - V_T\right)}\right|_{V_{GS}=3.5V} = \frac{1}{(E-4)\left(\frac{0.9}{0.6}\right)\left(4-0.7\right)} = 2K\Omega$$

$C_{OX}WL$ = (2.5f$F\mu^{-2}$)(0.6*0.9μ^2) = 1.3fF, Cg=1.2X = 1.5fF

For pMOS, ⌠ is 1/3, ➔ R is 3X, Cg is 1.5fF

Technology Files

- Design Rules
- Process Flow (Fabrication Technology)
- Model Parameters

TABLE 2B.1

Process scenario of major process steps in typical n-well CMOS process[a]

1.	Clean wafer	
2.	GROW THIN OXIDE	
3.	Apply photoresist	
4.	PATTERN n-well	(MASK #1)
5.	Develop photoresist	
6.	Deposit and diffus n-type impurities	
7.	Strip photoresist	
8.	Strip thin oxide	
9.	Grow thin oxide	
10.	Apply layer of Si_3N_4	
11.	Apply photoresist	
12.	PATTERN Si_3N_4 (active area definition)	(MASK #2)
13.	Develop photoresist	
14.	Etch Si_3N_4	
15.	Strip photoresist	
	Optional field threshold voltage adjust	
	A.1 Apply photoresist	
	A.2 PATTERN ANTIMOAT IN SUBSTRATE	(MASK #A1)
	A.3 Develop photoresist	
	A.4 FIELD IMPLANT p-type)	
	A.5 Strip photoresist	
16.	GROW FIELD OXIDE	
17.	Strip Si_3N_4	
18.	Strip thin oxide	
19.	GROW GATE OXIDE	
20.	POLYSILICON DEPOSITION (POLY I)	
21.	Apply photoresist	
22.	PATTERN POLYSILICON	(MASK #3)
23.	Develop photoresist	
24.	ETCH POLYSILICON	

25. Strip photoresist

Optional steps for double polysilicon process

B.1 Strip thin oxide
B.2 GROW THIN OXIDE
B.3 POLYSILICON DEPOSITION (POLY II)
B.4 Apply photoresist
B.5 PATTERN POLYSILICON (MASK #B1)
B.6 Develop photoresist
B.7 ETCH POLYSILICON
B.8 Strip photoresist
B.9 Strip thin oxide

26. Apply photoresist
27. PATTERN P-CHANNEL DRAINS AND SOURCES AND P^+ GUARD RINGS (p-well ohmic contacts) (MASK #4)
28. Develop photoresist
29. p^+ IMPLANT
30. Strip photoresist
31. Apply photoresist
32. PATTERN N-CHANNEL DRAINS AND SOURCES AND N^+ GUARD RINGS (top ohmic contact to substrate) (MASK #5)
33. Develop photoresist
34. n^+ IMPLANT
35. Strip photoresist
36. Strip thin oxide
37. Grow oxide
38. Apply photoresist
39. PATTERN CONTACT OPENINGS (MASK #6)
40. Develop photoresist
41. Etch oxide
42. Strip photoresist

43. APPLY METAL
44. Apply photoresist
45. PATTERN METAL (MASK #7)
46. Develop photoresist
47. Etch metal
48. Strip photoresist

Optional steps for double metal process

C.1 Strip thin oxide
C.2 DEPOSIT INTERMETAL OXIDE
C.3 Apply photoresist
C.4 PATTERN VIAS (MASK #C1)
C.5 Develop photoresist
C.6 Etch oxide
C.7 Strip photoresist
C.8 APPLY METAL (Metal 2)
C.9 Apply photoresist
C.10 PATTERN METAL (MASK #C2)
C.11 Develop photoresist
C.12 Etch metal
C.13 Strip photoresist

49. APPLY PASSIVATION
50. Apply photoresist
51. PATTERN PAD OPENINGS (MASK #8)
52. Develop photoresist
53. Etch passivation
54. Strip photoresist
55. ASSEMBLE, PACKAGE AND TEST

Bulk CMOS Process Description

- n-well process
- Single Metal Only Depicted
- Double Poly

  – This type of process dominates what is used for high-volume “low-cost” processing of integrated circuits today

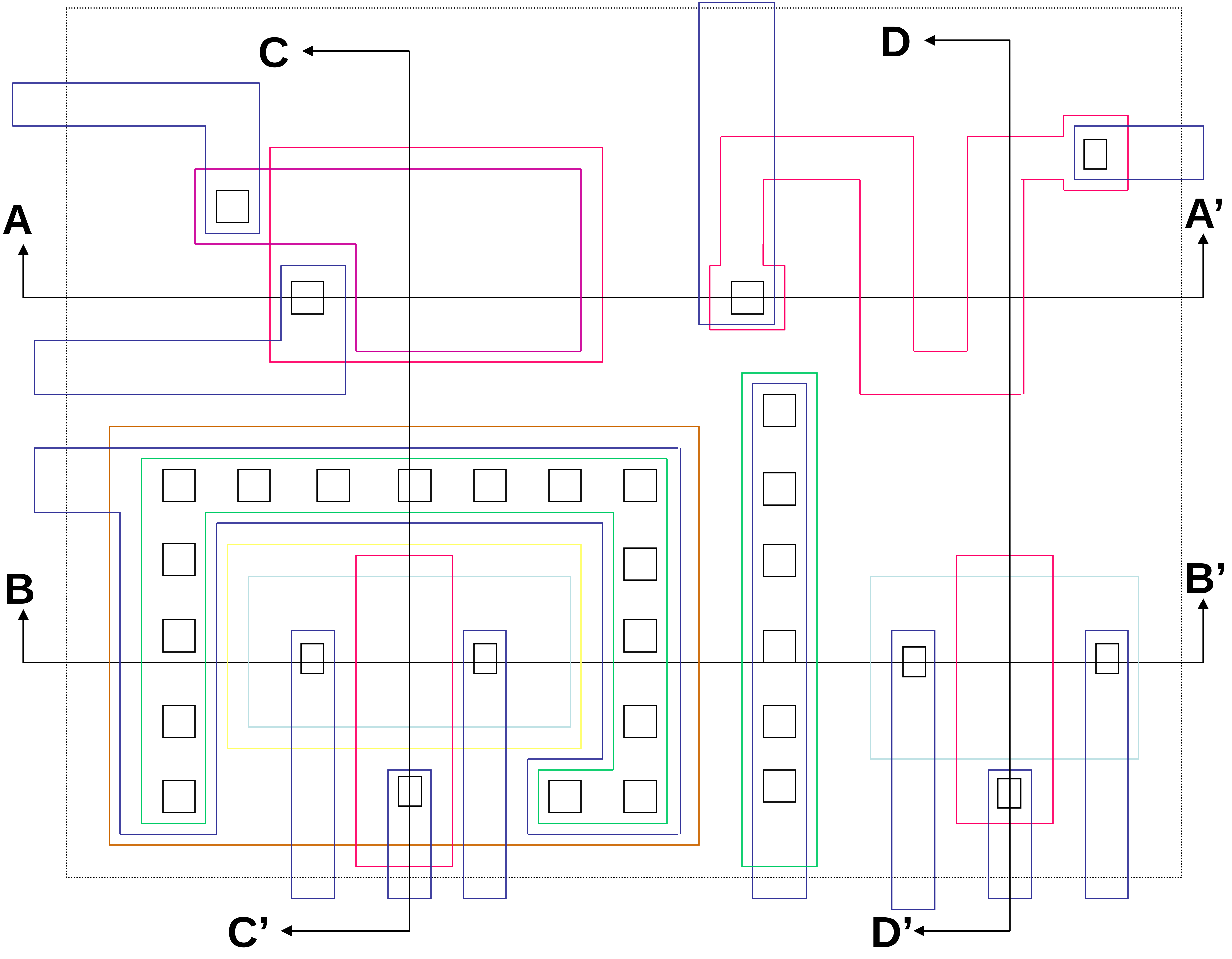
  – Many process variants and specialized processes are used for lower-volume or niche applications

  – Emphasis in this course will be on the electronics associated with the design of integrated electronic circuits in processes targeting high-volume low-cost products where competition based upon price differentiation may be acute

  – Basic electronics concepts, however, are applicable for lower-volume or niche applicaitons

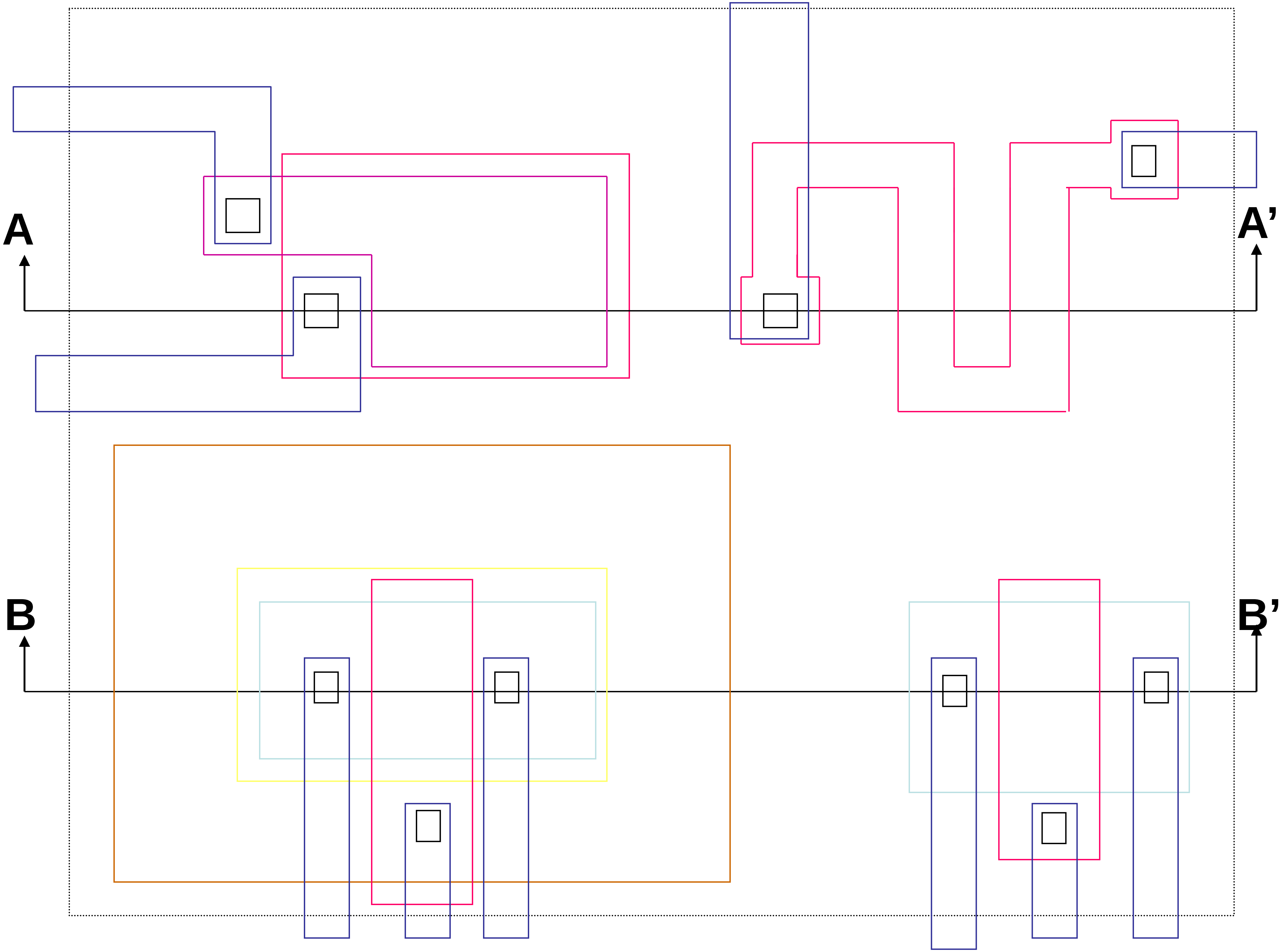
Components Shown

- n-channel MOSFET
- p-channel MOSFET
- Poly Resistor
- Doubly Poly Capacitor

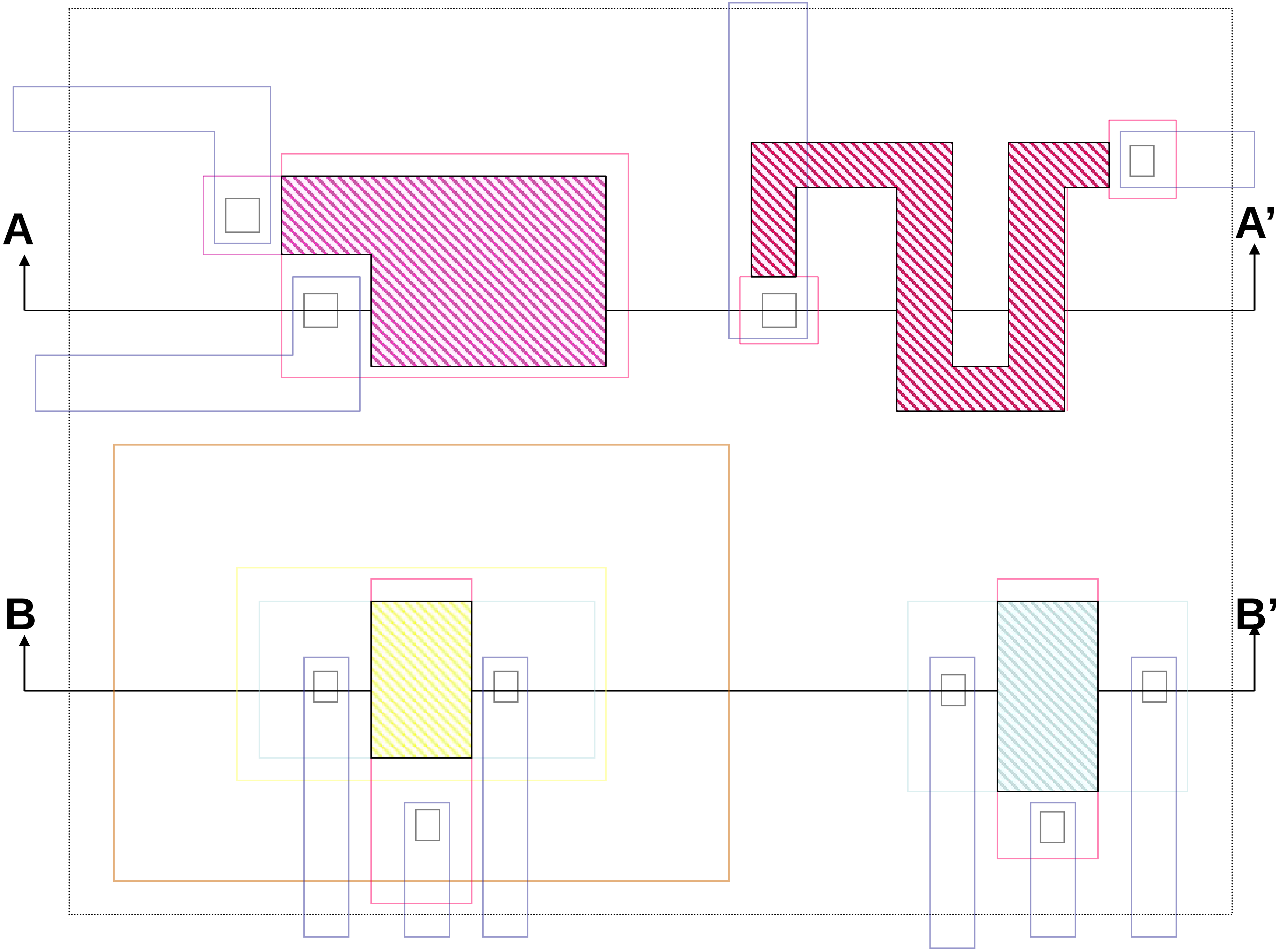

C
D
A
A'
B
B'
C'
D'

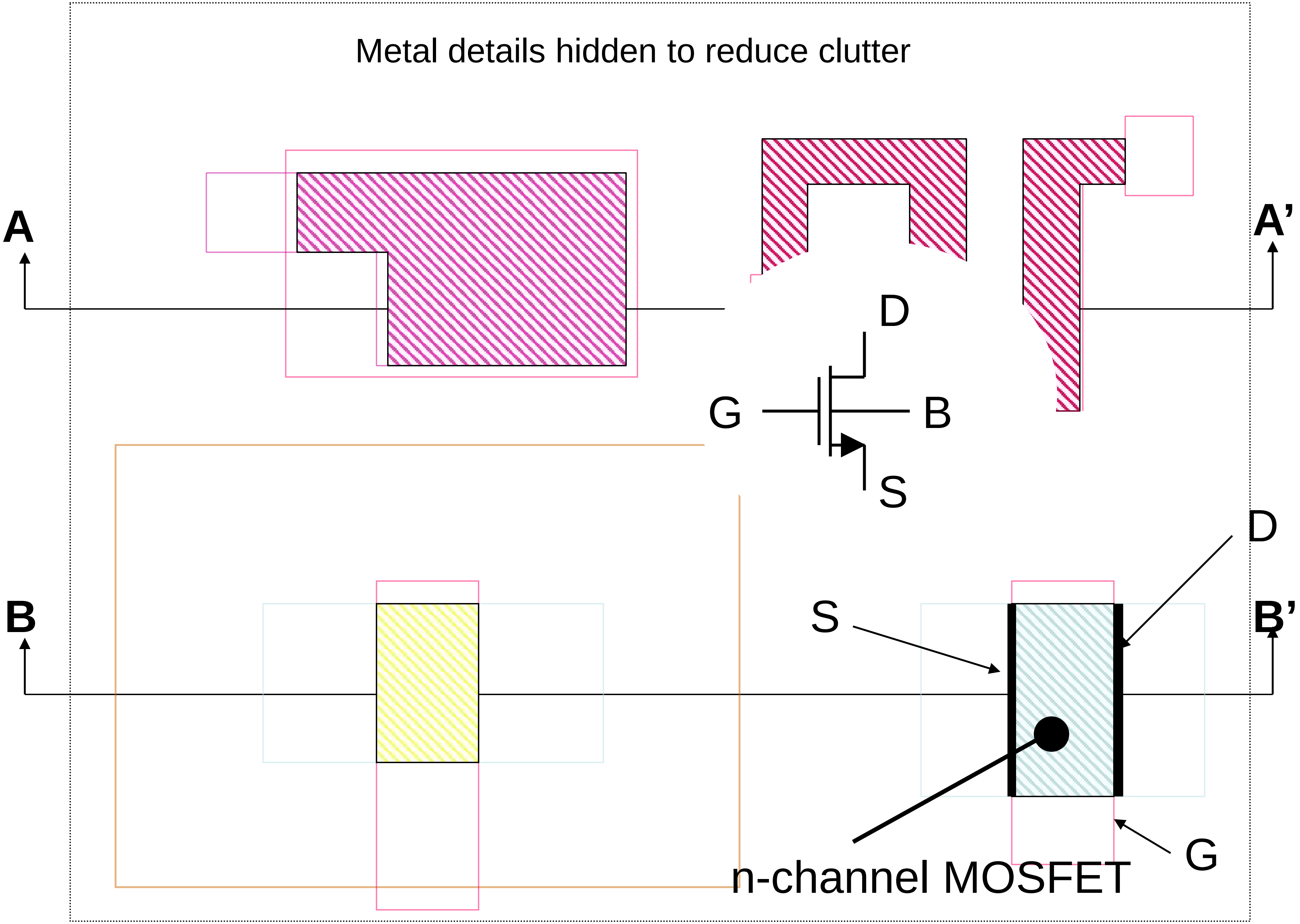
Consider Basic Components Only

Well Contacts and Guard Rings Will be Discussed Later

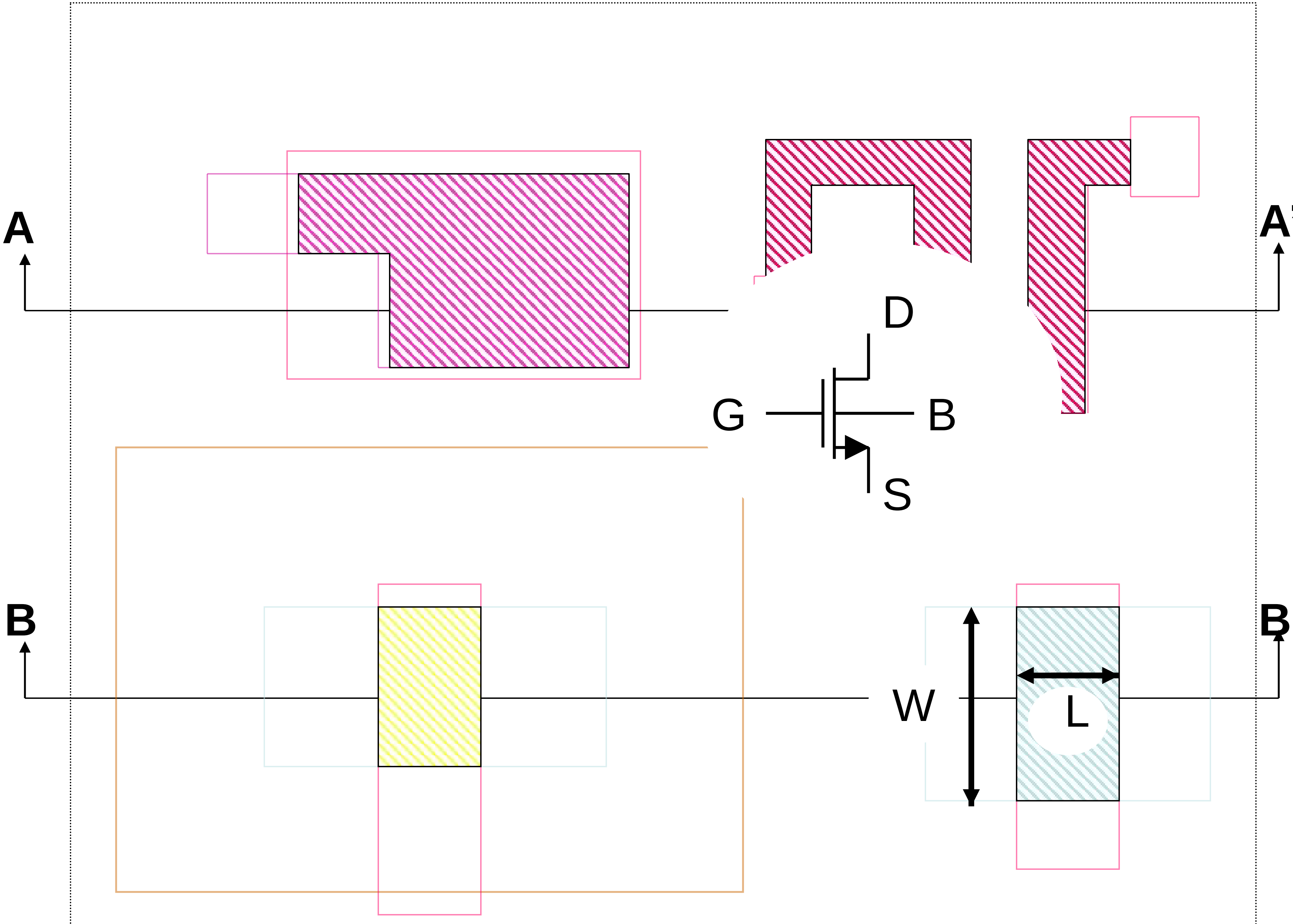


A
A’
B
B’


A
A'
B
B'



Metal details hidden to reduce clutter
A
A'
D
G
B
S
B
B'
S
D
G
n-channel MOSFET


A
A'
D
G
B
S
B
B'
W
L

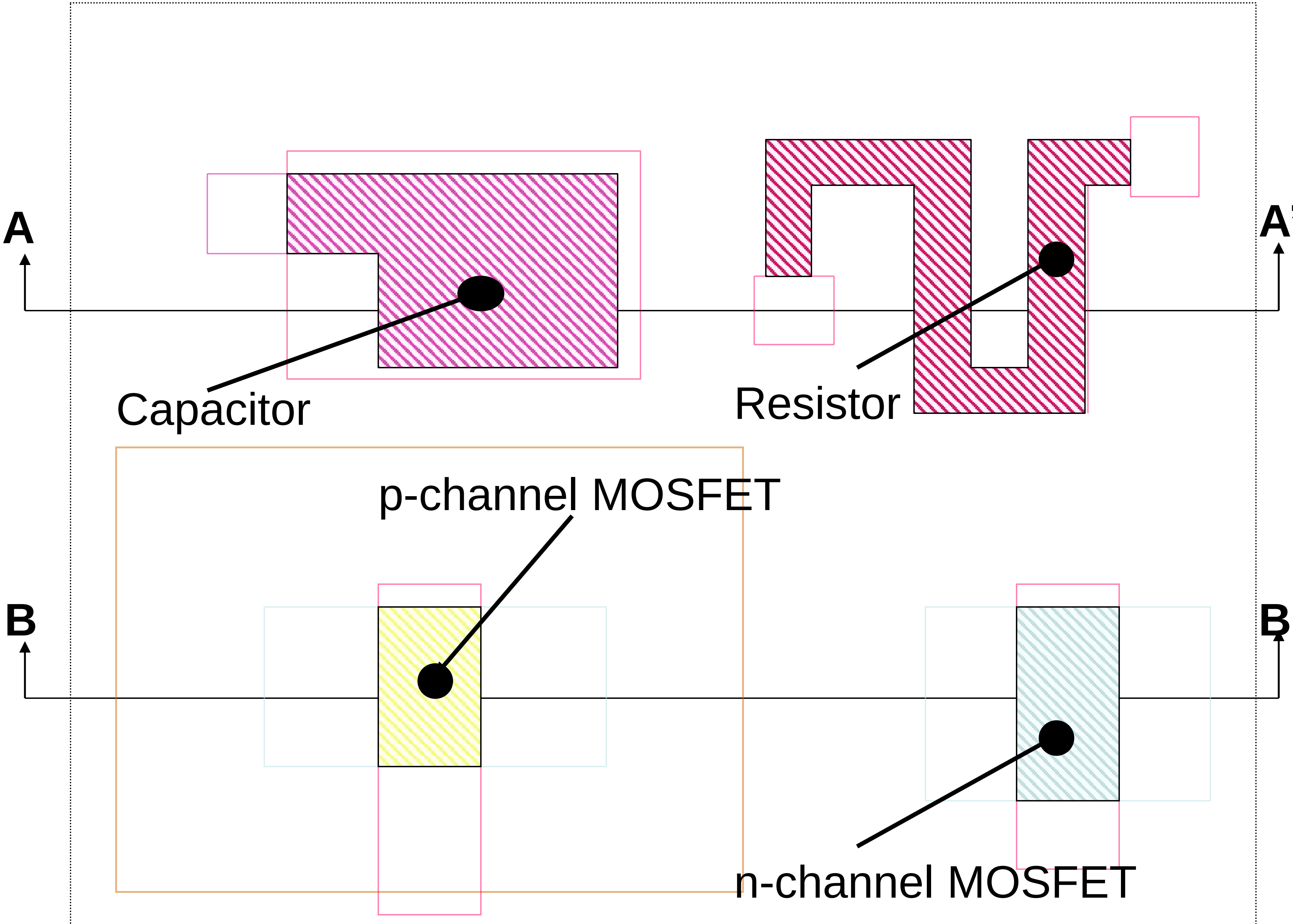
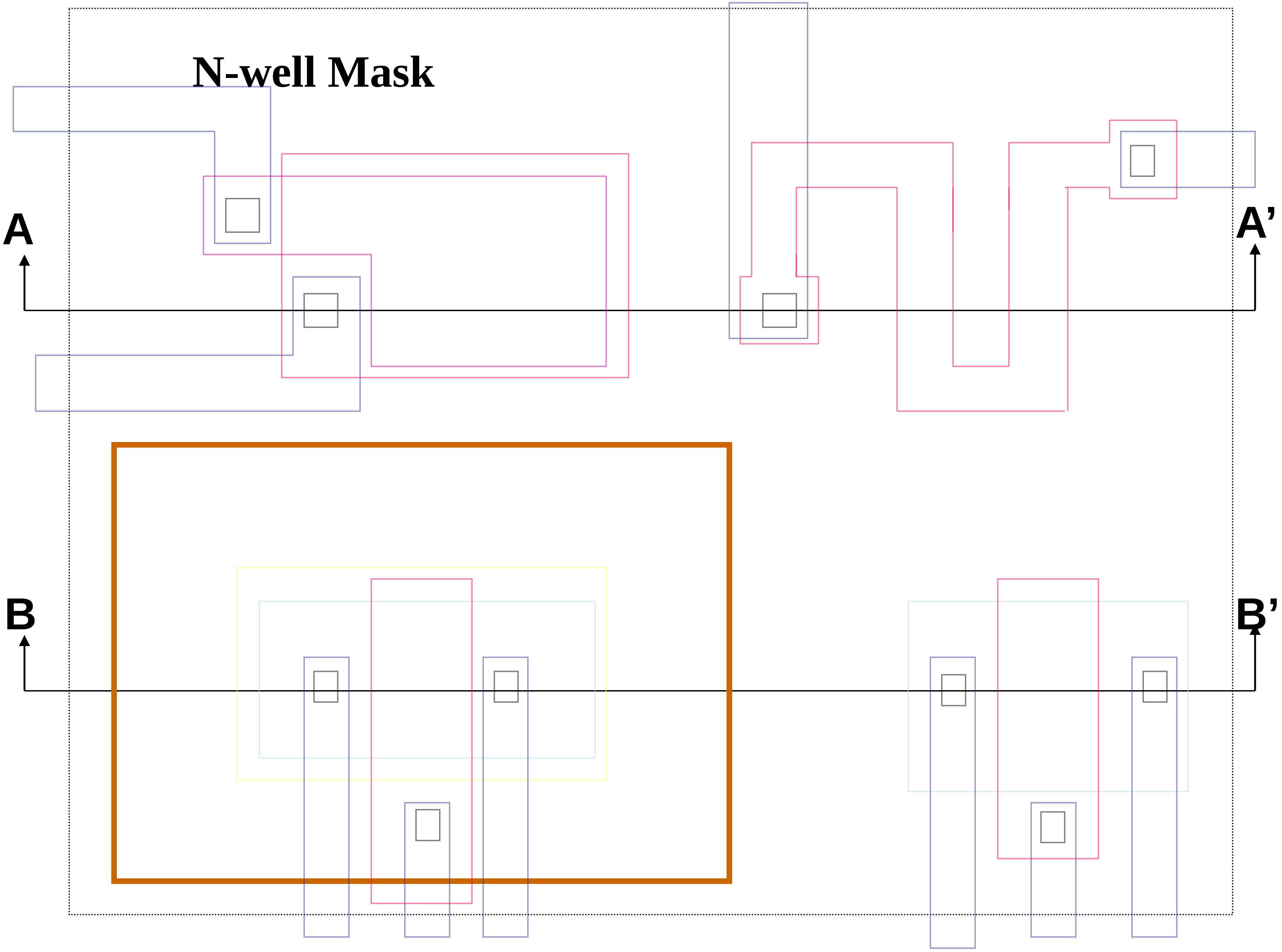

A
A'
Capacitor
Resistor
p-channel MOSFET
B
B'
n-channel MOSFET

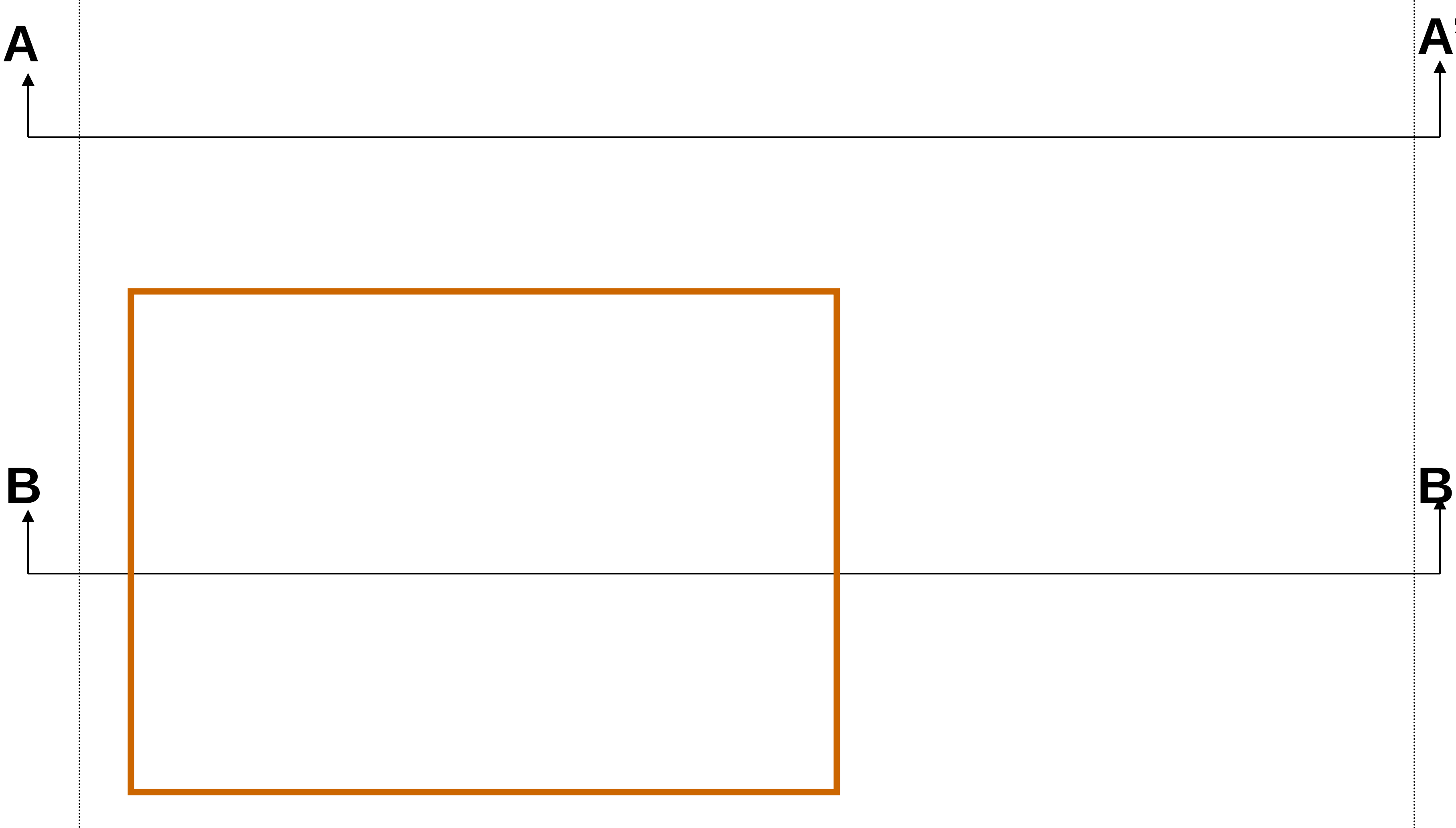
TABLE 2B.1
Process scenario of major process steps in typical n-well CMOS process[a]

1.	Clean wafer	
2.	GROW THIN OXIDE	
3.	Apply photoresist	
4.	PATTERN **n-well**	(MASK #1)
5.	Develop photoresist	
6.	Deposit and diffus n-type impurities	
7.	Strip photoresist	
8.	Strip thin oxide	
9.	Grow thin oxide	
10.	Apply layer of Si_3N_4	
11.	Apply photoresist	
12.	PATTERN Si_3N_4 (active area definition)	(MASK #2)
13.	Develop photoresist	
14.	Etch Si_3N_4	
15.	Strip photoresist	
	Optional field threshold voltage adjust	
	A.1 Apply photoresist	
	A.2 PATTERN ANTIMOAT IN SUBSTRATE	(MASK #A1)
	A.3 Develop photoresist	
	A.4 FIELD IMPLANT p-type)	
	A.5 Strip photoresist	
16.	GROW FIELD OXIDE	
17.	Strip Si_3N_4	
18.	Strip thin oxide	
19.	GROW GATE OXIDE	
20.	POLYSILICON DEPOSITION (POLY I)	
21.	Apply photoresist	
22.	PATTERN POLYSILICON	(MASK #3)
23.	Develop photoresist	
24.	ETCH POLYSILICON	

N-well Mask

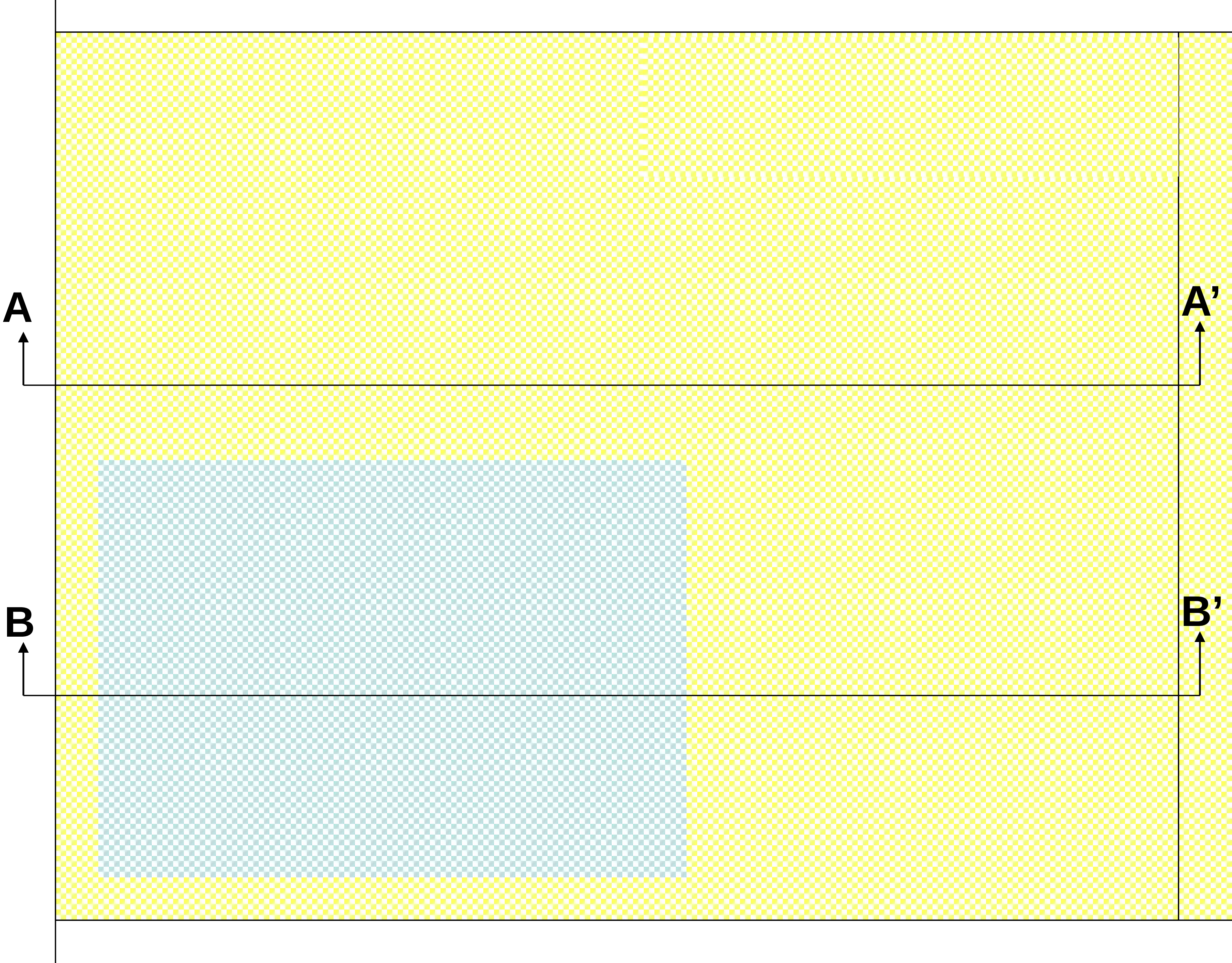


N-well Mask

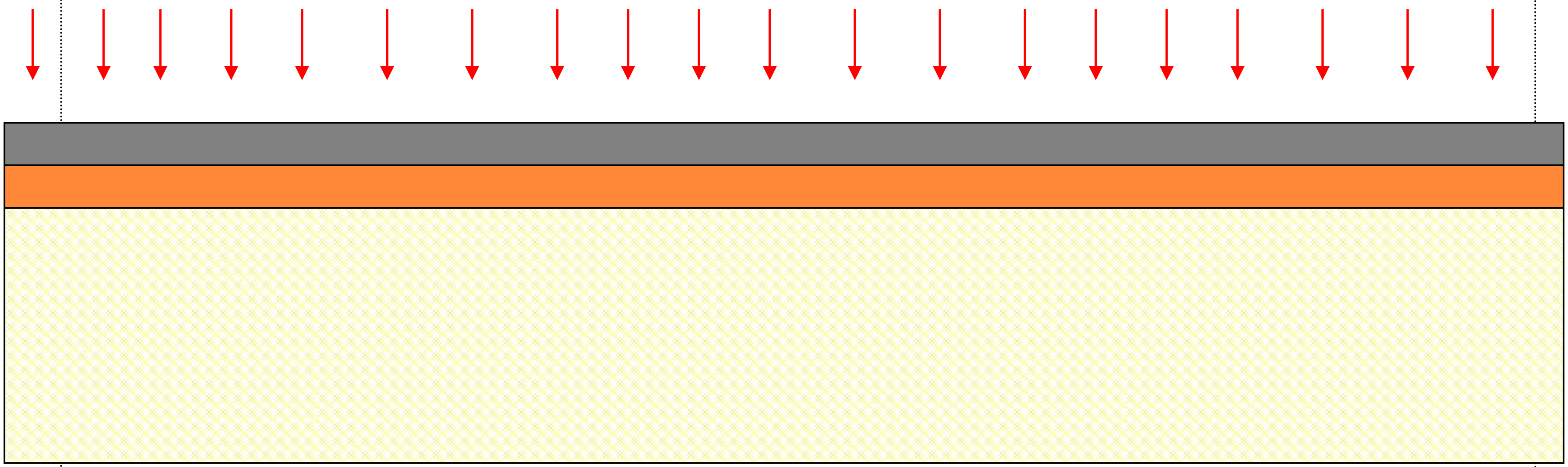


Detailed Description of First Photolithographic Steps Only

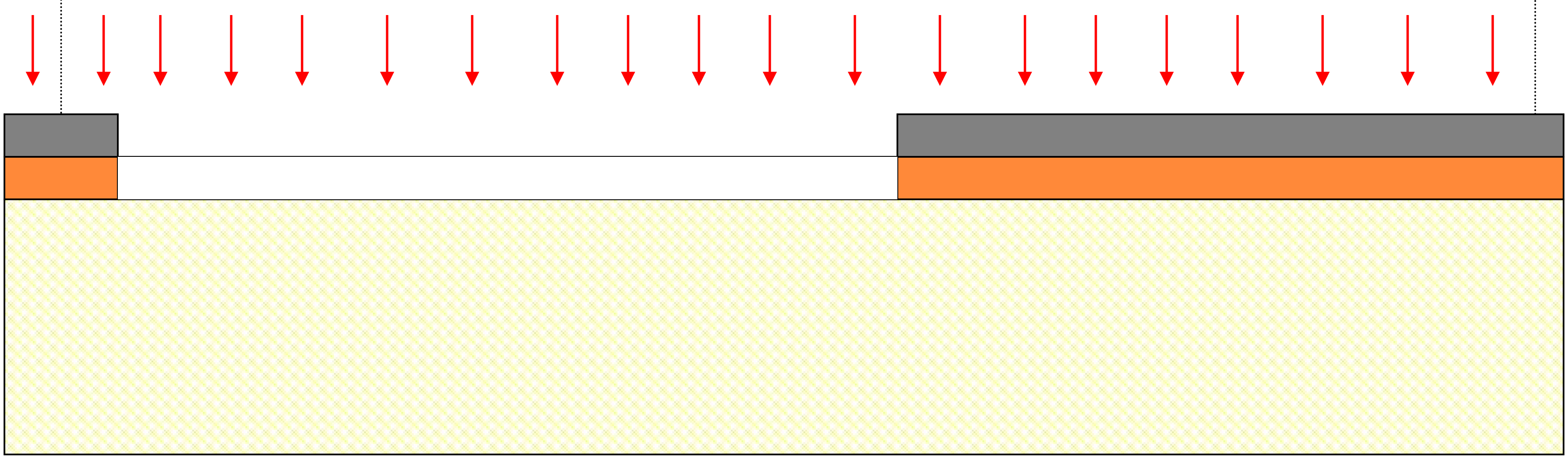
- Top View
- Cross-Section View


A
A’
B
B’

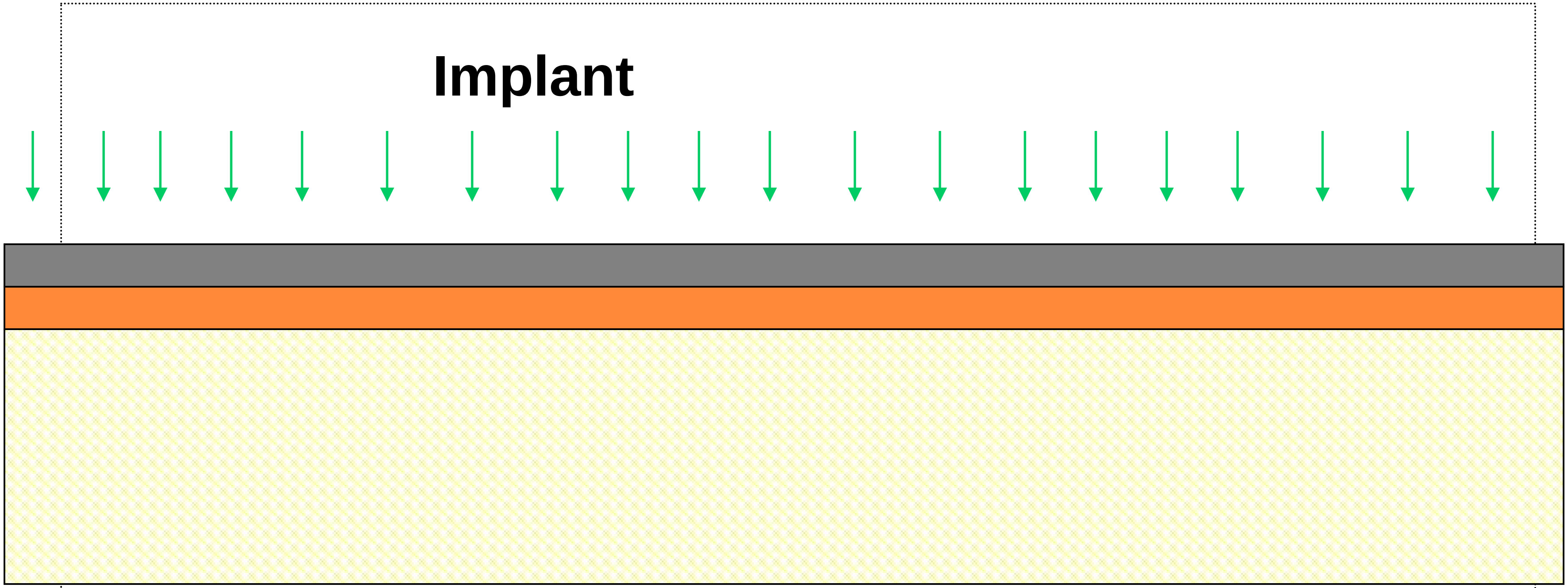
Develop



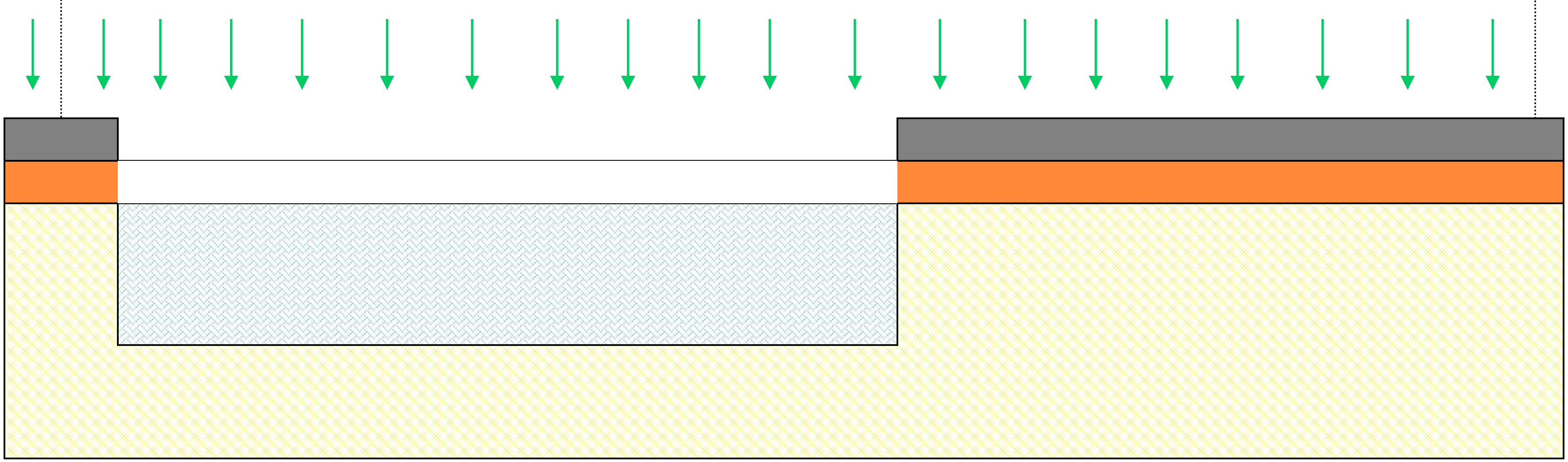
A-A’ Section



B-B’ Section

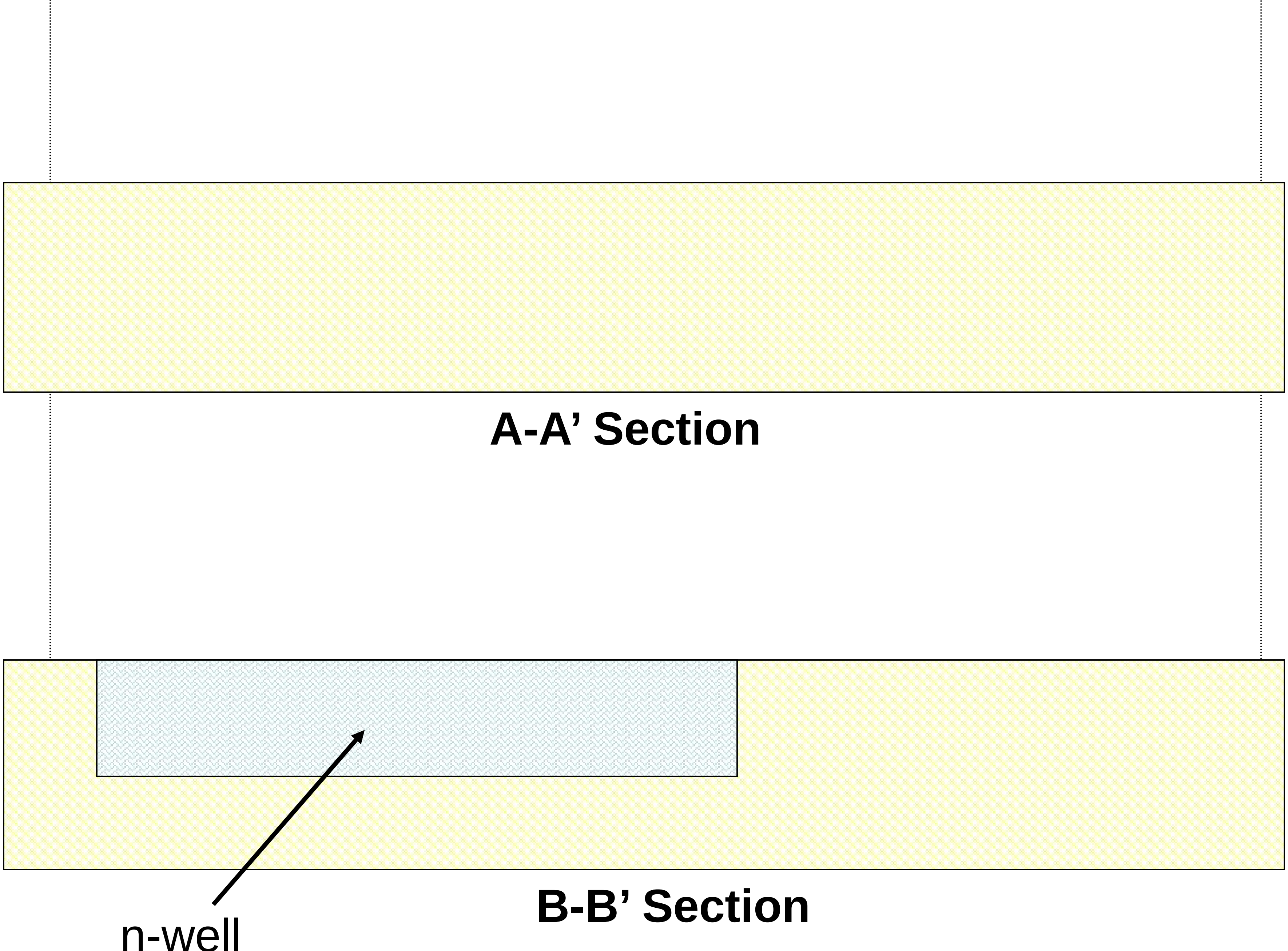


A-A' Section



B-B' Section

N-well Mask



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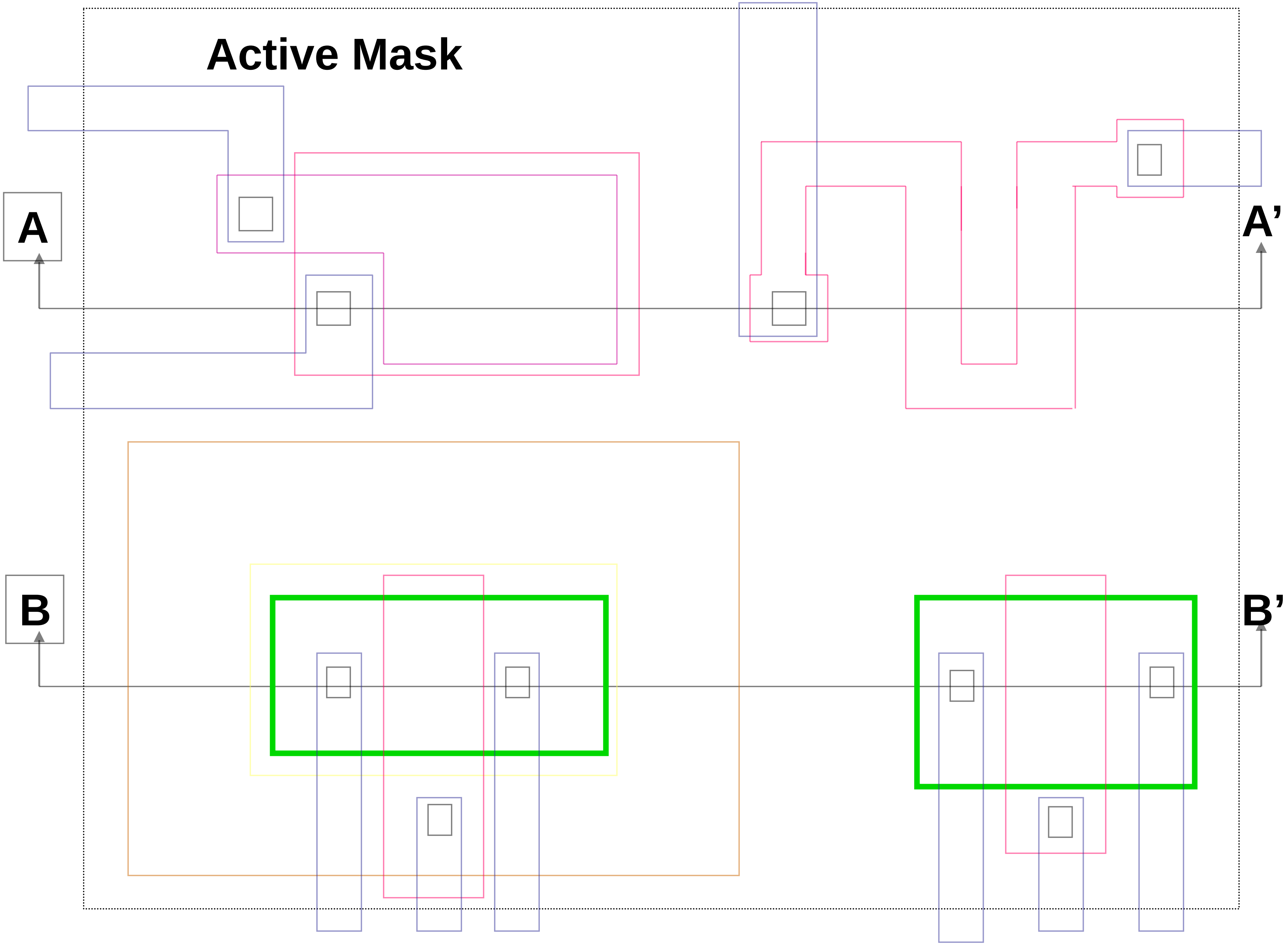
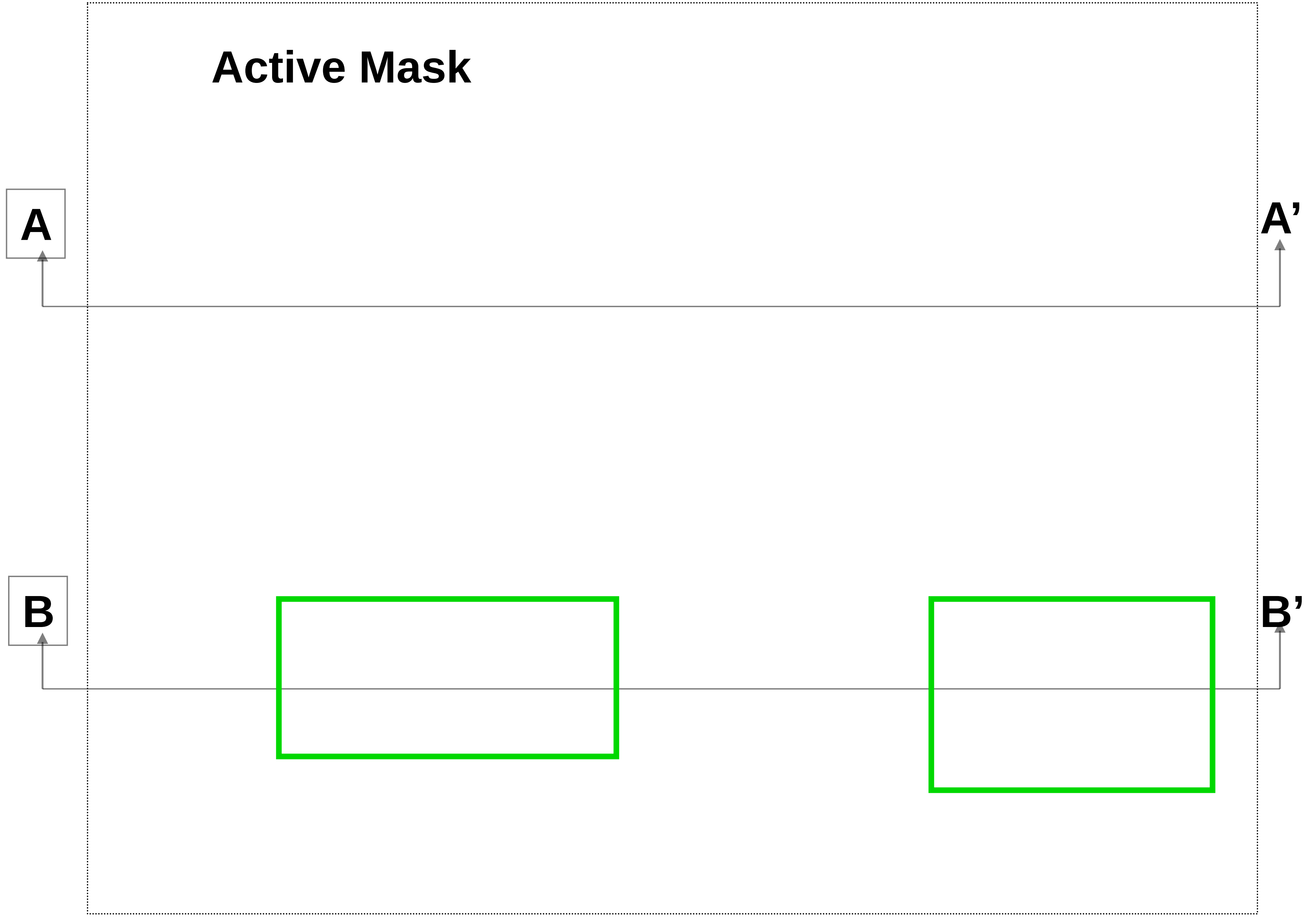
Process scenario of major process steps in typical n-well CMOS process[a]

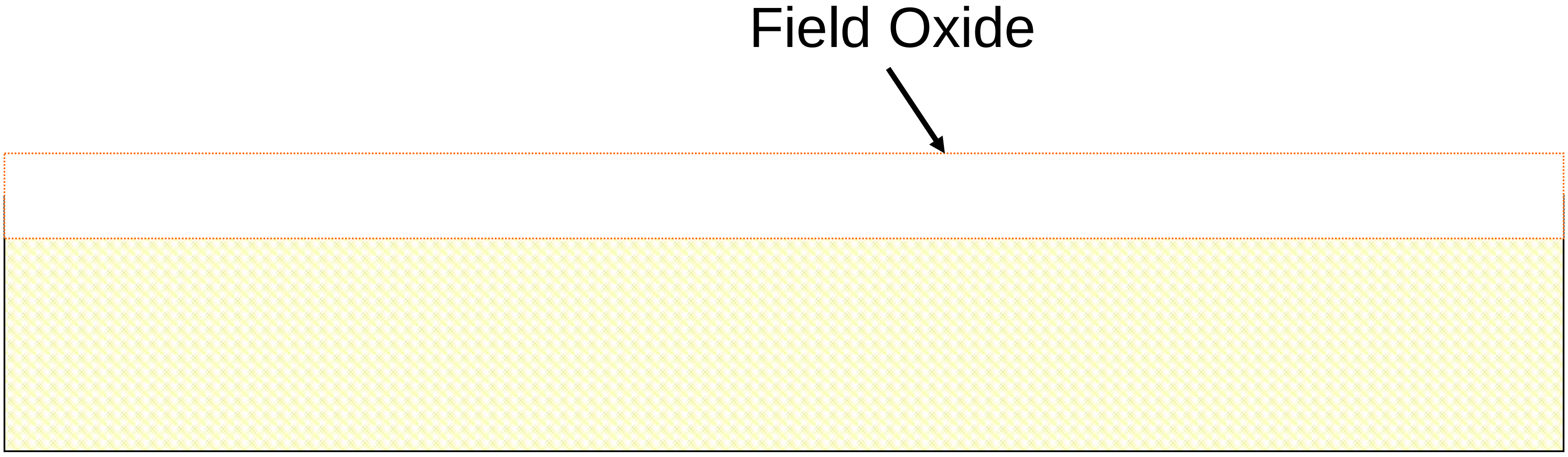
1.	Clean wafer	
2.	GROW THIN OXIDE	
3.	Apply photoresist	
4.	PATTERN n-well	(MASK #1)
5.	Develop photoresist	
6.	Deposit and diffus n-type impurities	
7.	Strip photoresist	
8.	Strip thin oxide	
9.	Grow thin oxide	
10.	Apply layer of Si_3N_4	
11.	Apply photoresist	
12.	PATTERN Si_3N_4 (active area definition)	(MASK #2)
13.	Develop photoresist	
14.	Etch Si_3N_4	
15.	Strip photoresist	
	Optional field threshold voltage adjust	
	A.1 Apply photoresist	
	A.2 PATTERN ANTIMOAT IN SUBSTRATE	(MASK #A1)
	A.3 Develop photoresist	
	A.4 FIELD IMPLANT p-type)	
	A.5 Strip photoresist	
16.	GROW FIELD OXIDE	
17.	Strip Si_3N_4	
18.	Strip thin oxide	
19.	GROW GATE OXIDE	
20.	POLYSILICON DEPOSITION (POLY I)	
21.	Apply photoresist	
22.	PATTERN POLYSILICON	(MASK #3)
23.	Develop photoresist	
24.	ETCH POLYSILICON	

Active Mask

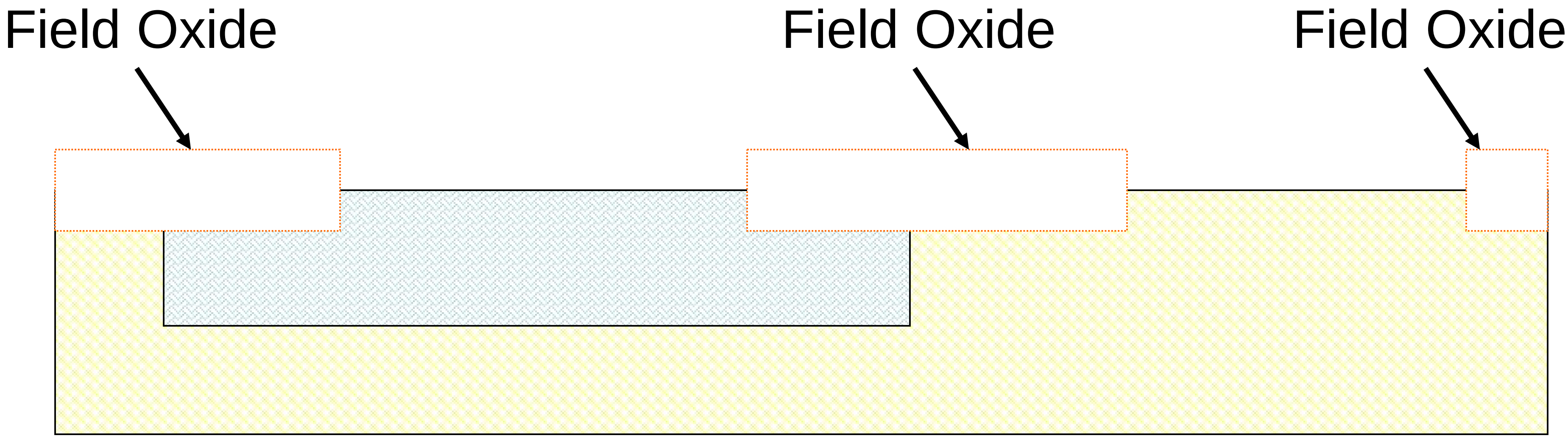



Active Mask
A
A'
B
B'

Active Mask



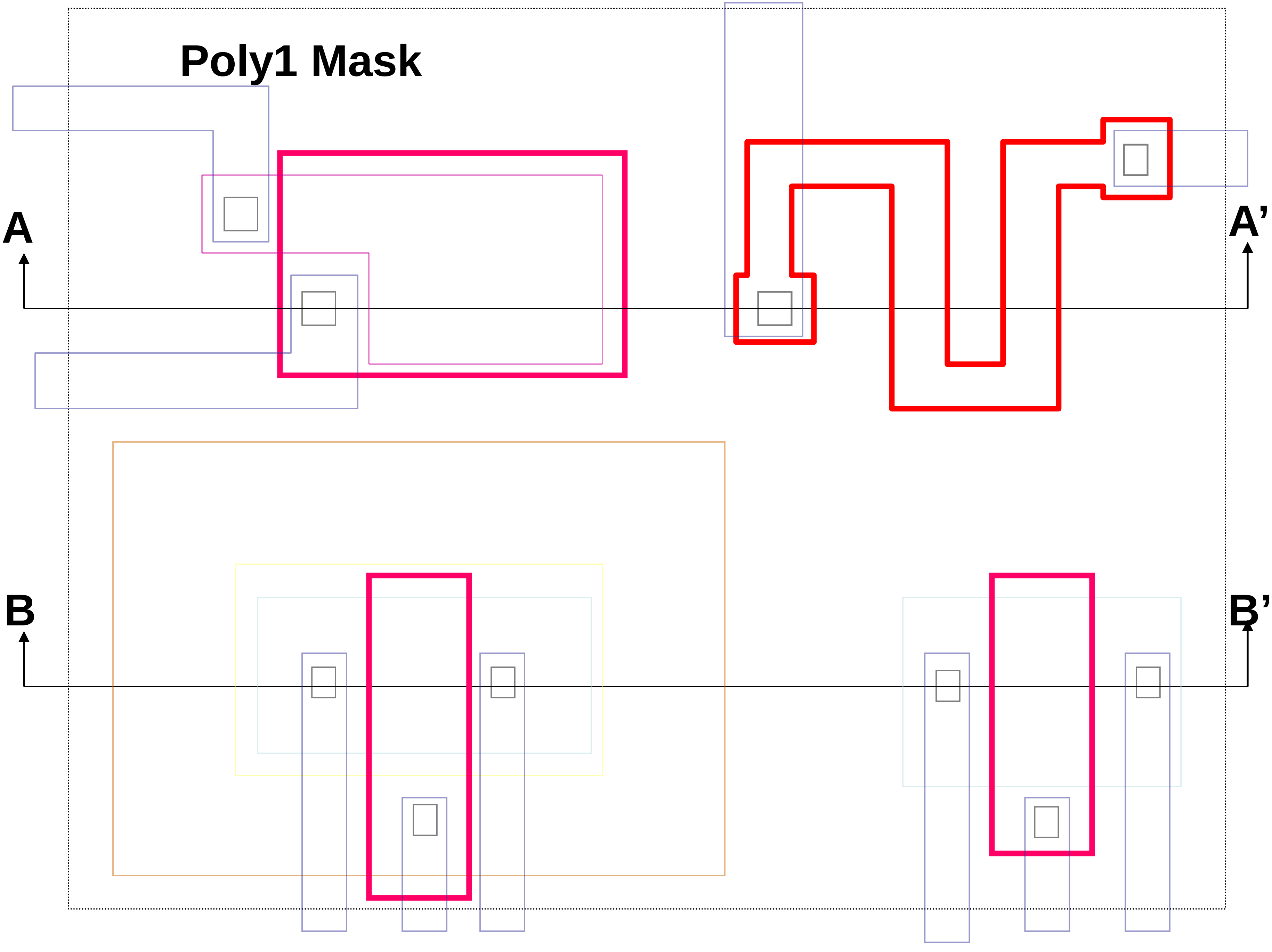
A-A' Section



B-B' Section

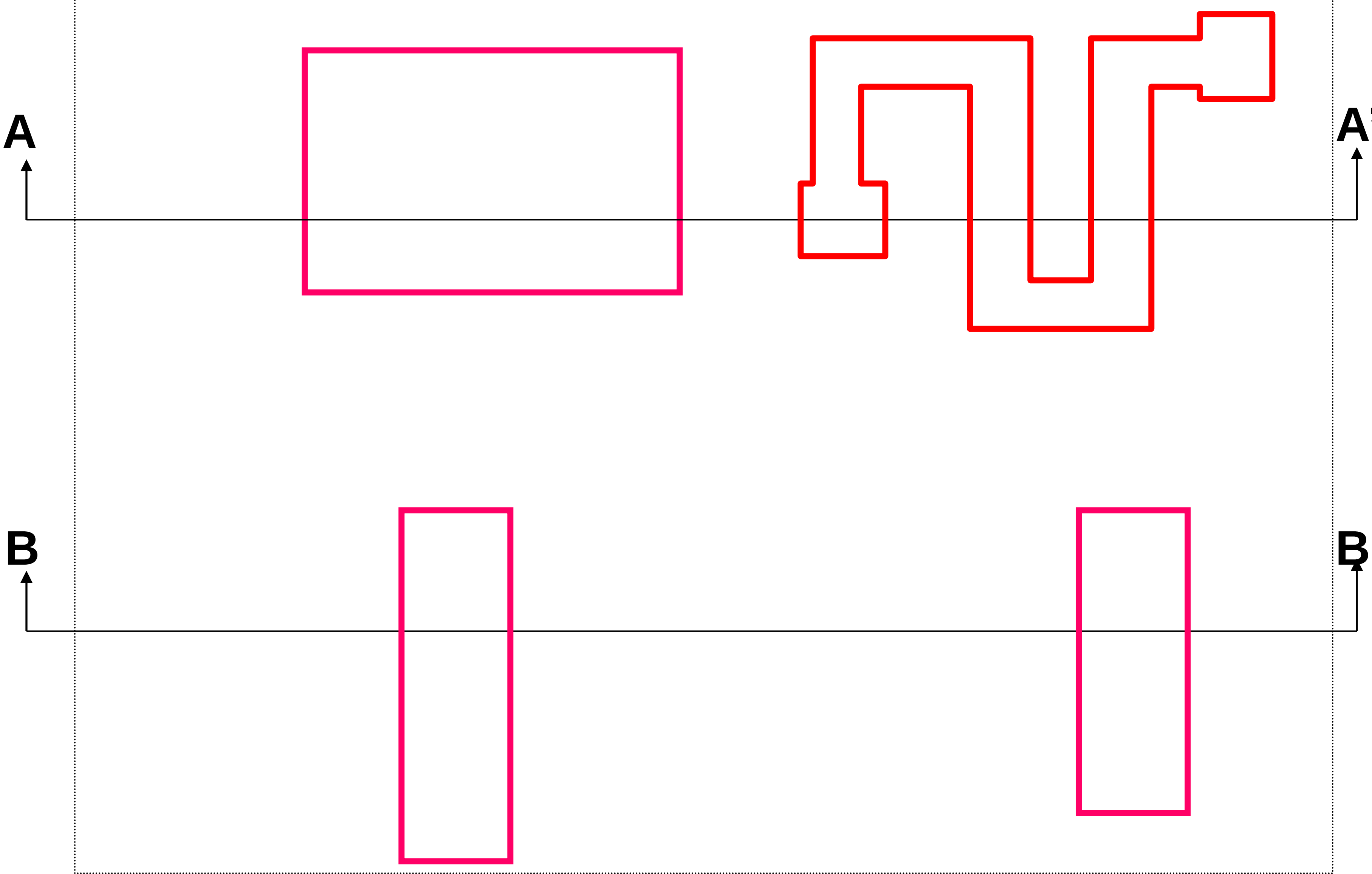
TABLE 2B.1
Process scenario of major process steps in typical n-well CMOS process[a]

1.	Clean wafer	
2.	GROW THIN OXIDE	
3.	Apply photoresist	
4.	PATTERN n-well	(MASK #1)
5.	Develop photoresist	
6.	Deposit and diffus n-type impurities	
7.	Strip photoresist	
8.	Strip thin oxide	
9.	Grow thin oxide	
10.	Apply layer of Si_3N_4	
11.	Apply photoresist	
12.	PATTERN Si_3N_4 (active area definition)	(MASK #2)
13.	Develop photoresist	
14.	Etch Si_3N_4	
15.	Strip photoresist	
	Optional field threshold voltage adjust	
	A.1 Apply photoresist	
	A.2 PATTERN ANTIMOAT IN SUBSTRATE	(MASK #A1)
	A.3 Develop photoresist	
	A.4 FIELD IMPLANT p-type)	
	A.5 Strip photoresist	
16.	GROW FIELD OXIDE	
17.	Strip Si_3N_4	
18.	Strip thin oxide	
19.	GROW GATE OXIDE	
20.	POLYSILICON DEPOSITION (POLY I)	
21.	Apply photoresist	
22.	PATTERN POLYSILICON	(MASK #3)
23.	Develop photoresist	
24.	ETCH POLYSILICON	

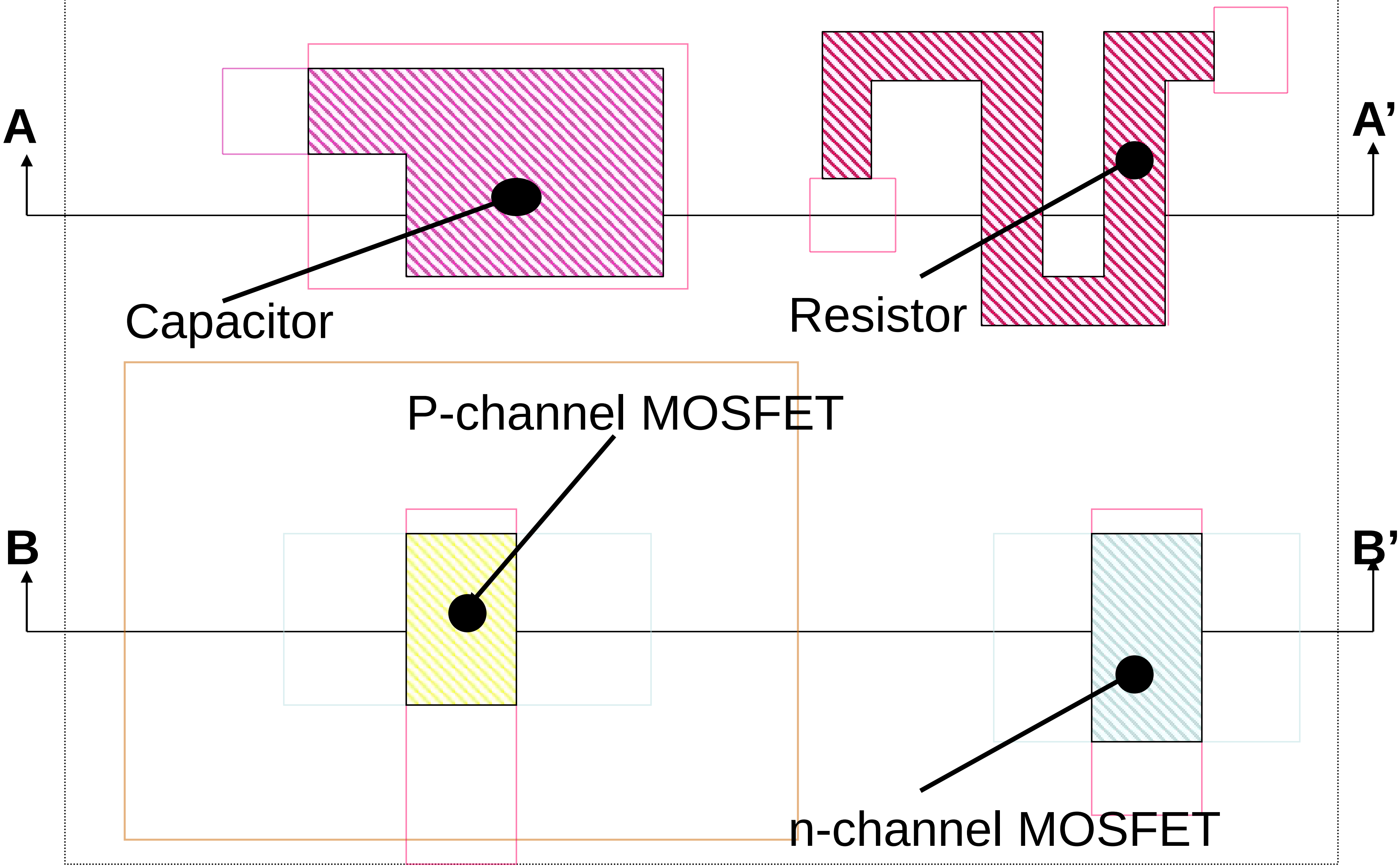


Poly1 Mask
A
A’
B
B’

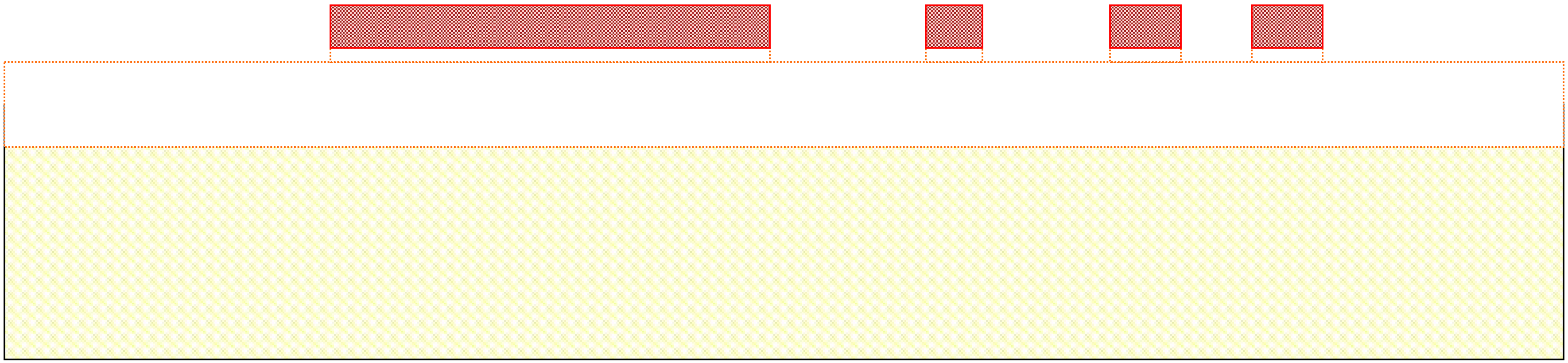
Poly1 Mask



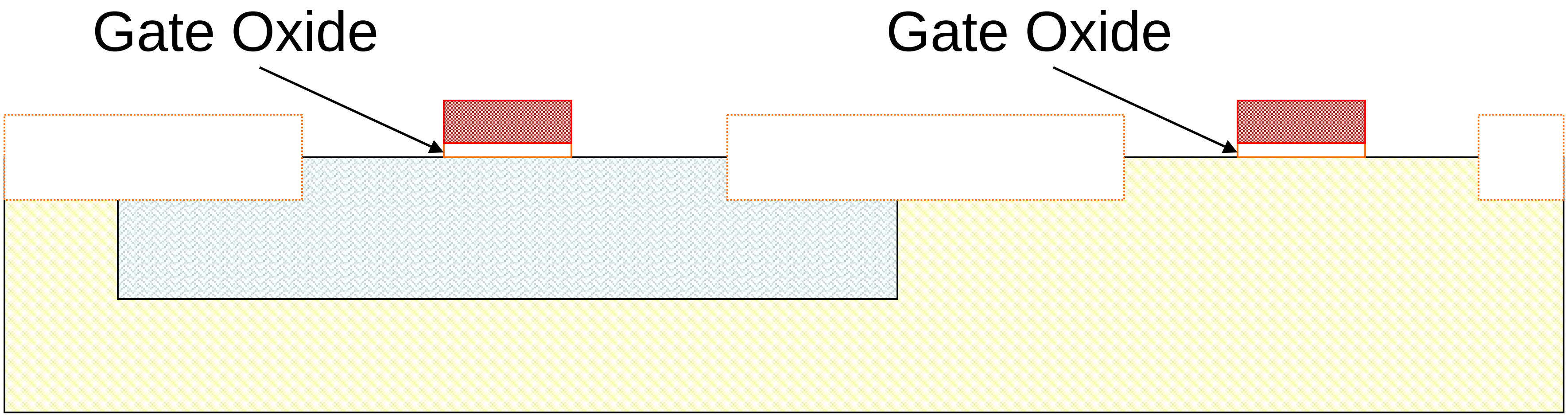
Poly plays a key role in all four types of devices !



Poly 1 Mask



A-A' Section



B-B' Section

TABLE 2B.1
Process scenario of major process steps in typical n-well CMOS process[a]

1.	Clean wafer	
2.	GROW THIN OXIDE	
3.	Apply photoresist	
4.	PATTERN n-well	(MASK #1)
5.	Develop photoresist	
6.	Deposit and diffus n-type impurities	
7.	Strip photoresist	
8.	Strip thin oxide	
9.	Grow thin oxide	
10.	Apply layer of Si_3N_4	
11.	Apply photoresist	
12.	PATTERN Si_3N_4 (active area definition)	(MASK #2)
13.	Develop photoresist	
14.	Etch Si_3N_4	
15.	Strip photoresist	
	Optional field threshold voltage adjust	
	A.1 Apply photoresist	
	A.2 PATTERN ANTIMOAT IN SUBSTRATE	(MASK #A1)
	A.3 Develop photoresist	
	A.4 FIELD IMPLANT p-type)	
	A.5 Strip photoresist	
16.	GROW FIELD OXIDE	
17.	Strip Si_3N_4	
18.	Strip thin oxide	
19.	GROW GATE OXIDE	
20.	POLYSILICON DEPOSITION (POLY I)	
21.	Apply photoresist	
22.	PATTERN POLYSILICON	(MASK #3)
23.	Develop photoresist	
24.	ETCH POLYSILICON	

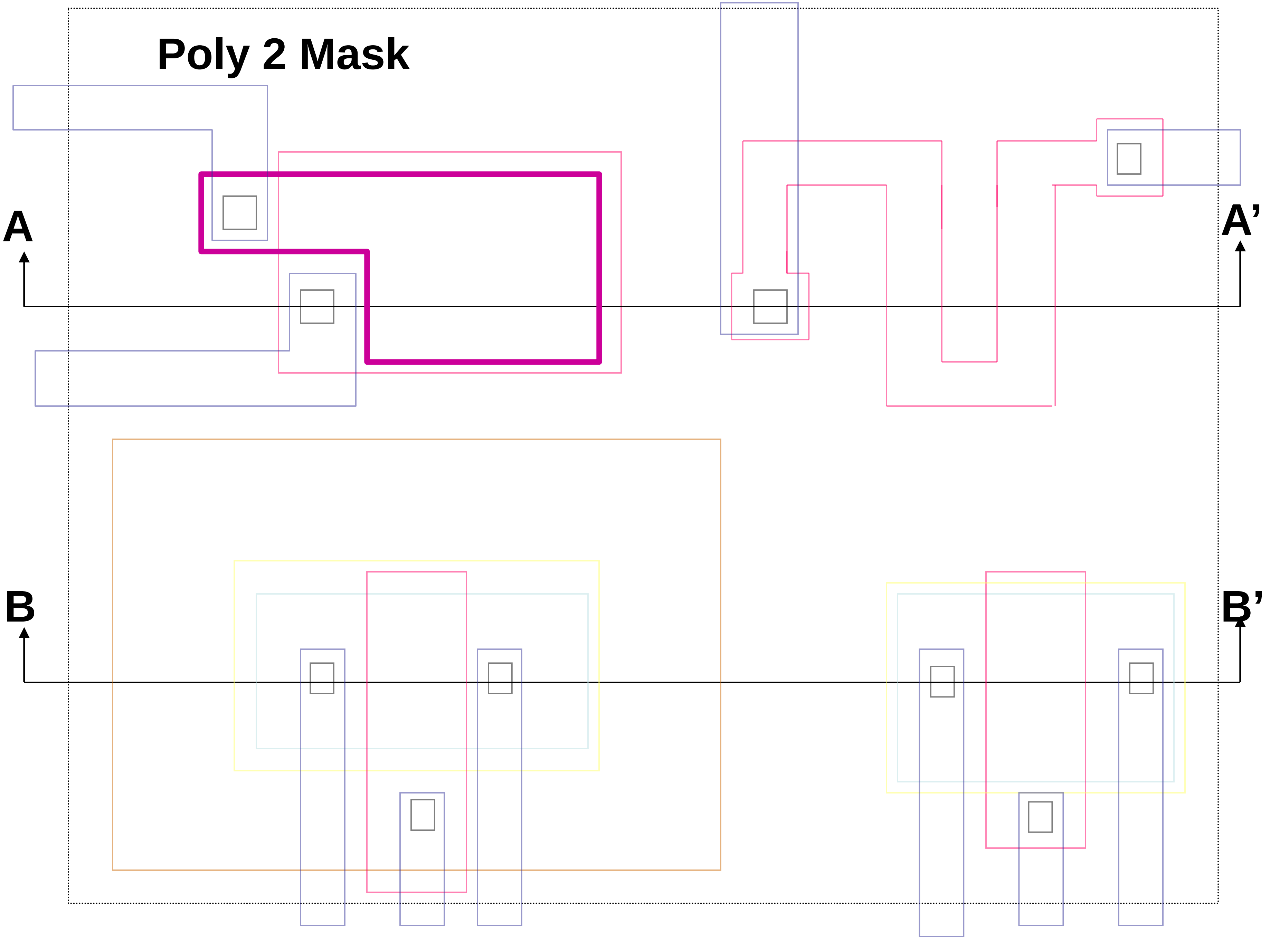
25. Strip photoresist

Optional steps for double polysilicon process

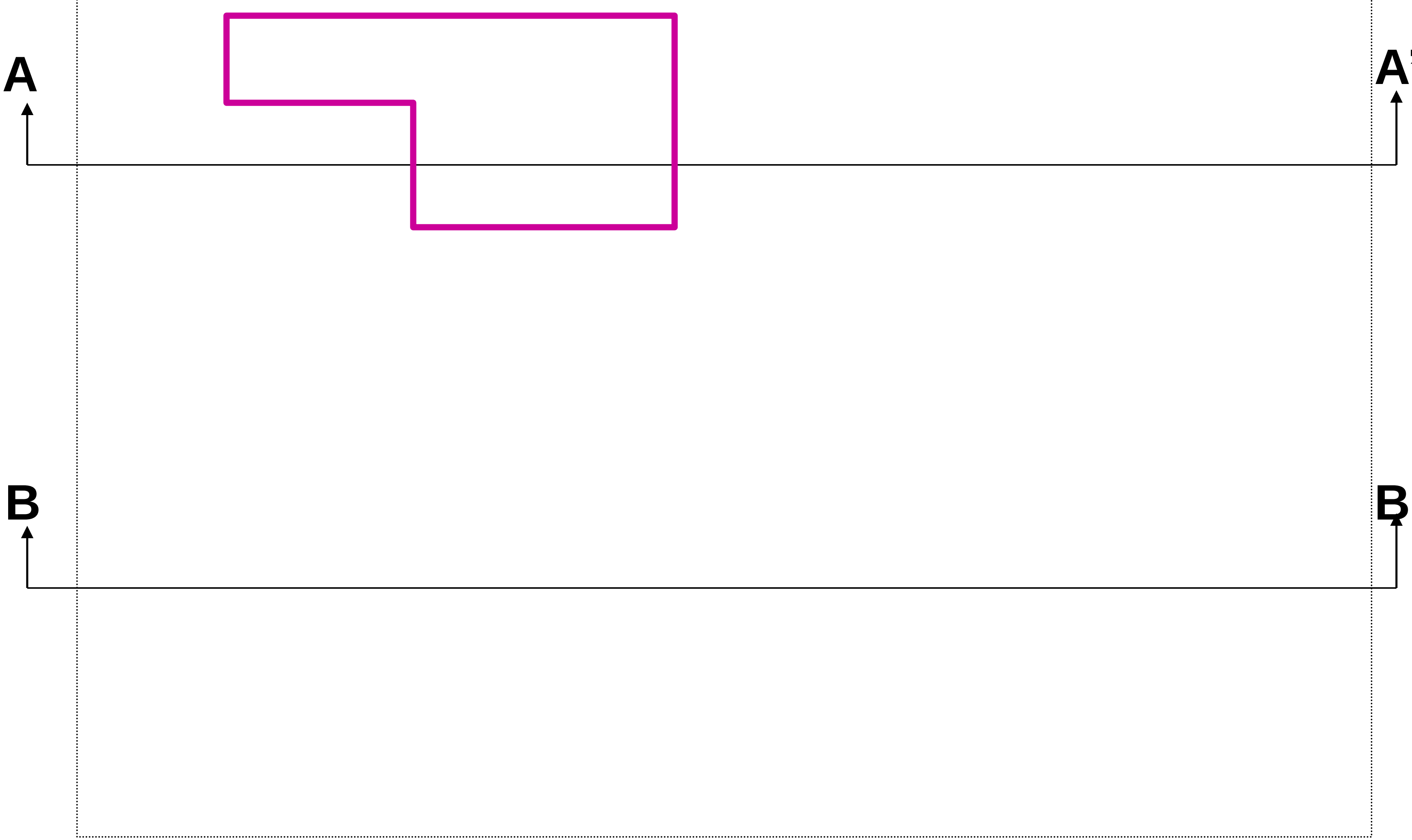
B.1 Strip thin oxide
B.2 GROW THIN OXIDE
B.3 POLYSILICON DEPOSITION (POLY II)
B.4 Apply photoresist
B.5 PATTERN POLYSILICON (MASK #B1)
B.6 Develop photoresist
B.7 ETCH POLYSILICON
B.8 Strip photoresist
B.9 Strip thin oxide

26. Apply photoresist
27. PATTERN P-CHANNEL DRAINS AND SOURCES AND P^+ GUARD RINGS (p-well ohmic contacts) (MASK #4)
28. Develop photoresist
29. p^+ IMPLANT
30. Strip photoresist
31. Apply photoresist
32. PATTERN N-CHANNEL DRAINS AND SOURCES AND N^+ GUARD RINGS (top ohmic contact to substrate) (MASK #5)
33. Develop photoresist
34. n^+ IMPLANT
35. Strip photoresist
36. Strip thin oxide
37. Grow oxide
38. Apply photoresist
39. PATTERN CONTACT OPENINGS (MASK #6)
40. Develop photoresist
41. Etch oxide
42. Strip photoresist

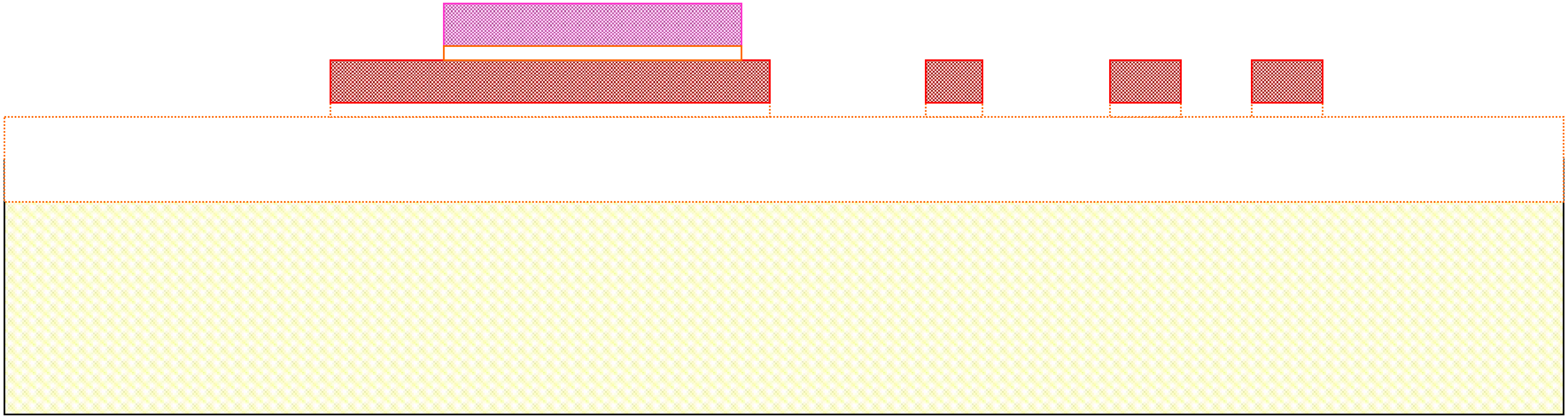
Poly 2 Mask



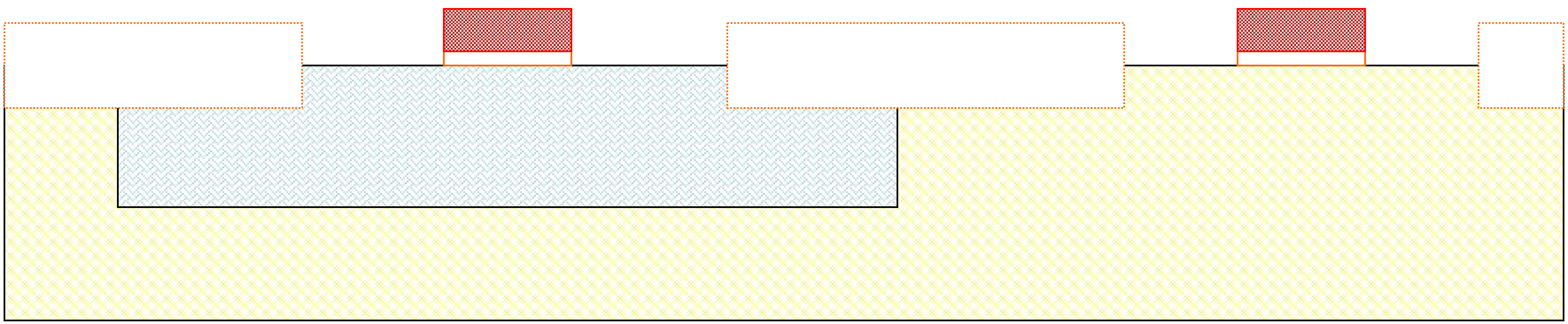
Poly 2 Mask



Poly 2 Mask



A-A’ Section



B-B’ Section

TABLE 2B.1
Process scenario of major process steps in typical n-well CMOS process[a]

1.	Clean wafer	
2.	GROW THIN OXIDE	
3.	Apply photoresist	
4.	PATTERN n-well	(MASK #1)
5.	Develop photoresist	
6.	Deposit and diffus n-type impurities	
7.	Strip photoresist	
8.	Strip thin oxide	
9.	Grow thin oxide	
10.	Apply layer of Si_3N_4	
11.	Apply photoresist	
12.	PATTERN Si_3N_4 (active area definition)	(MASK #2)
13.	Develop photoresist	
14.	Etch Si_3N_4	
15.	Strip photoresist	
	Optional field threshold voltage adjust	
	A.1 Apply photoresist	
	A.2 PATTERN ANTIMOAT IN SUBSTRATE	(MASK #A1)
	A.3 Develop photoresist	
	A.4 FIELD IMPLANT p-type)	
	A.5 Strip photoresist	
16.	GROW FIELD OXIDE	
17.	Strip Si_3N_4	
18.	Strip thin oxide	
19.	GROW GATE OXIDE	
20.	POLYSILICON DEPOSITION (POLY I)	
21.	Apply photoresist	
22.	PATTERN POLYSILICON	(MASK #3)
23.	Develop photoresist	
24.	ETCH POLYSILICON	

25. Strip photoresist

Optional steps for double polysilicon process

B.1 Strip thin oxide

B.2 GROW THIN OXIDE

B.3 POLYSILICON DEPOSITION (POLY II)

B.4 Apply photoresist

B.5 PATTERN POLYSILICON (MASK #B1)

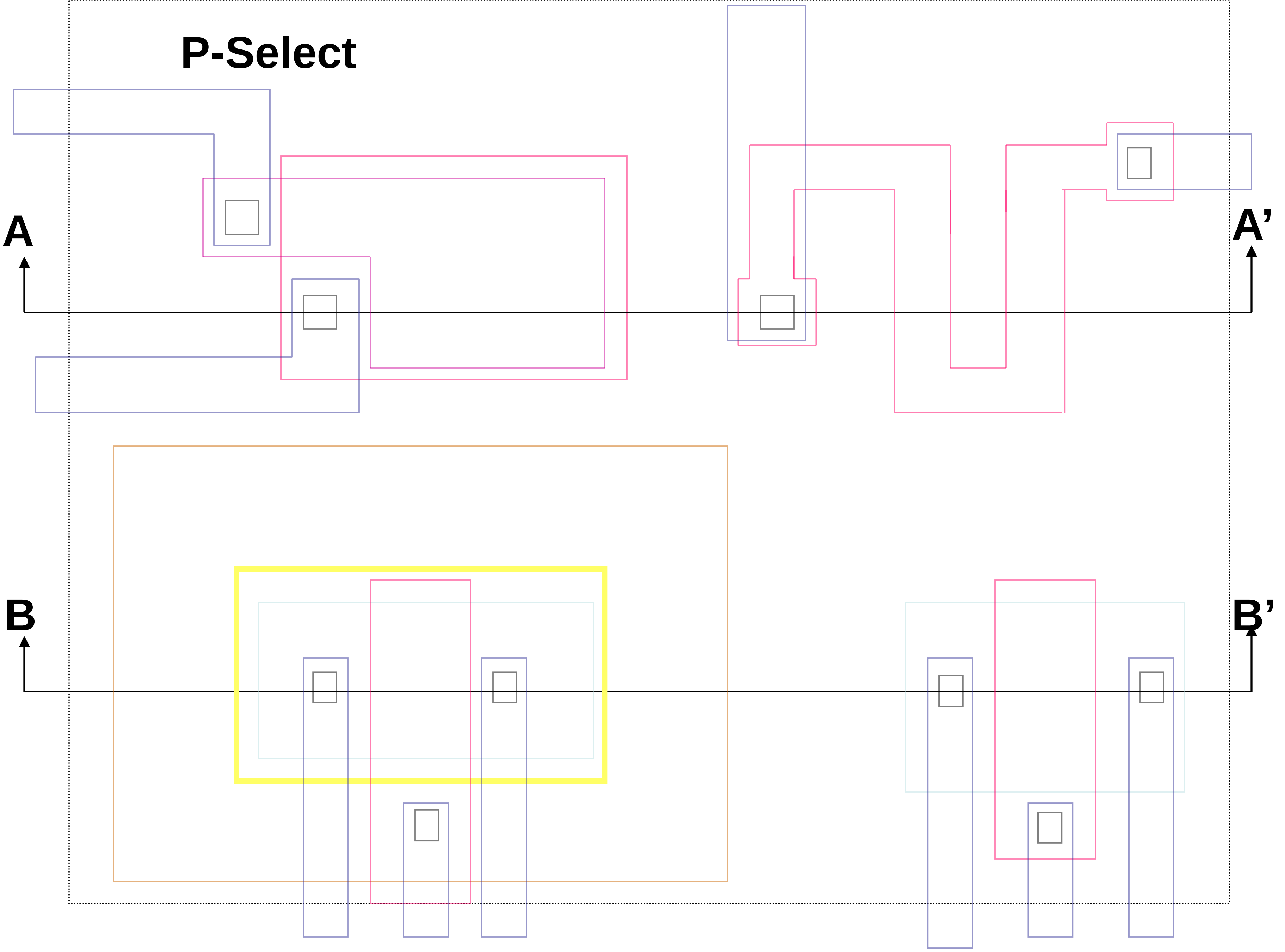
B.6 Develop photoresist

B.7 ETCH POLYSILICON

B.8 Strip photoresist

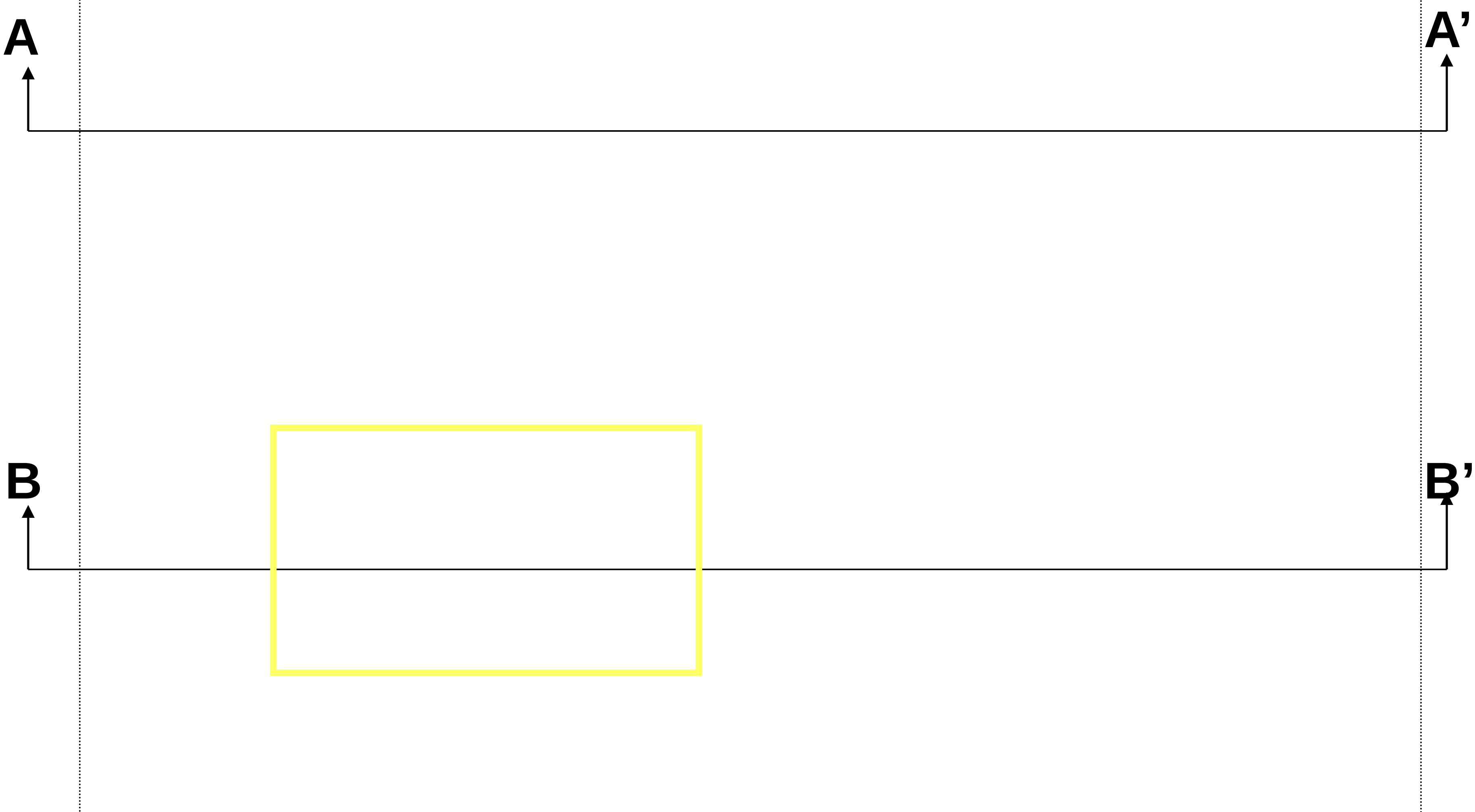
B.9 Strip thin oxide

26. Apply photoresist
27. PATTERN P-CHANNEL DRAINS AND SOURCES AND P^+ GUARD RINGS (p-well ohmic contacts) (MASK #4)
28. Develop photoresist
29. p^+ IMPLANT
30. Strip photoresist
31. Apply photoresist
32. PATTERN N-CHANNEL DRAINS AND SOURCES AND N^+ GUARD RINGS (top ohmic contact to substrate) (MASK #5)
33. Develop photoresist
34. n^+ IMPLANT
35. Strip photoresist
36. Strip thin oxide
37. Grow oxide
38. Apply photoresist
39. PATTERN CONTACT OPENINGS (MASK #6)
40. Develop photoresist
41. Etch oxide
42. Strip photoresist

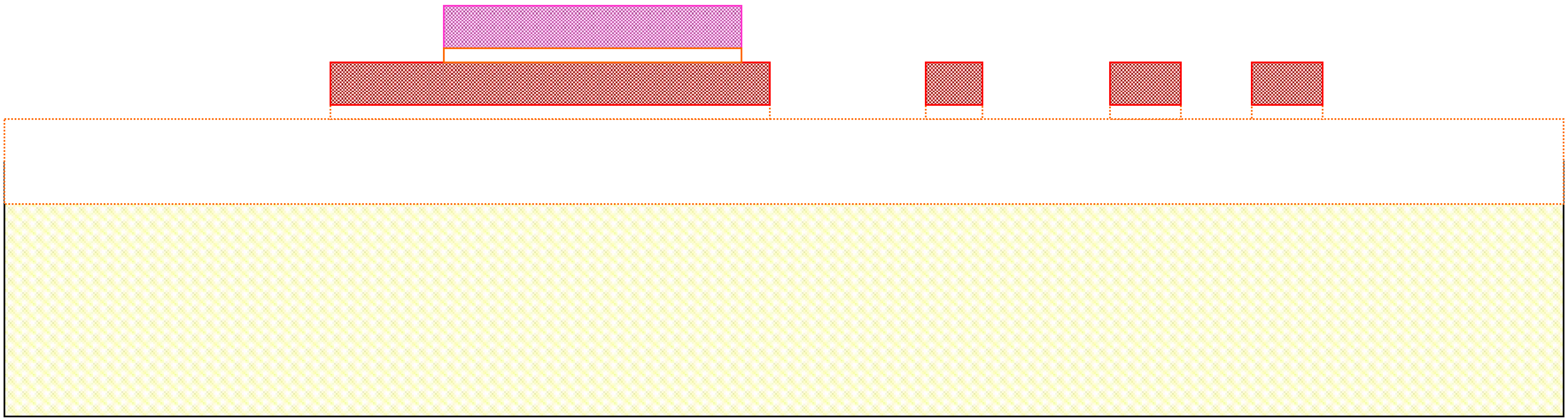


P-Select
A
A'
B
B'

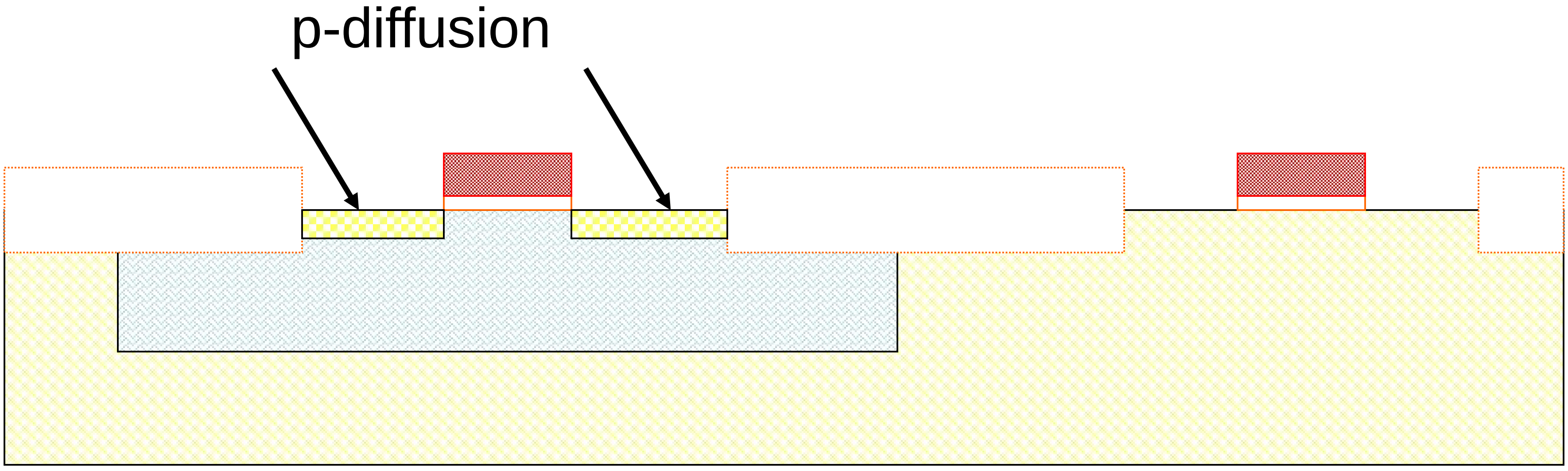
P-Select



P-Select Mask – p-diffusion



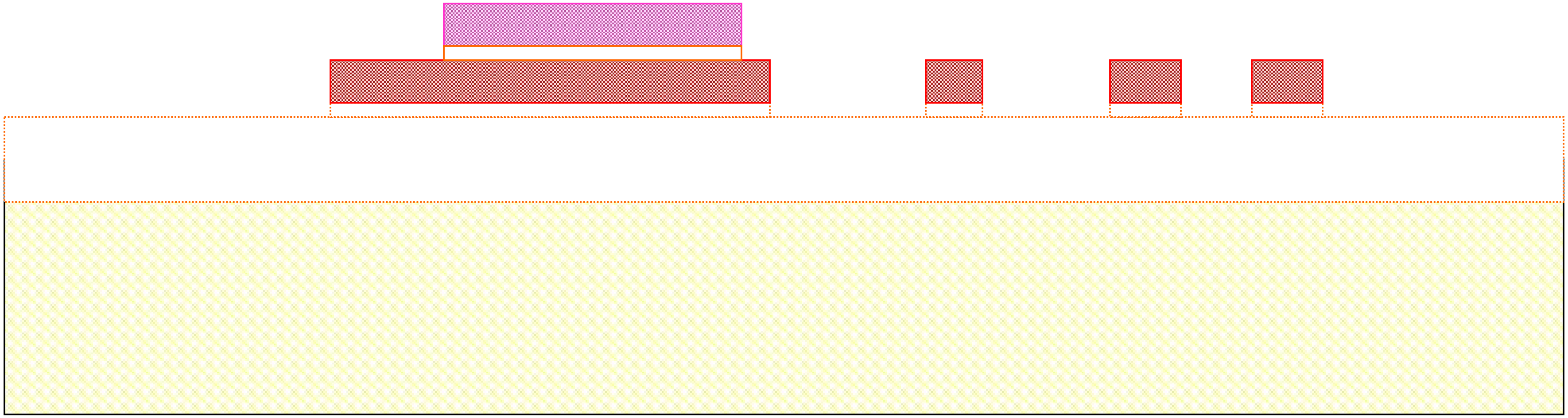
A-A’ Section



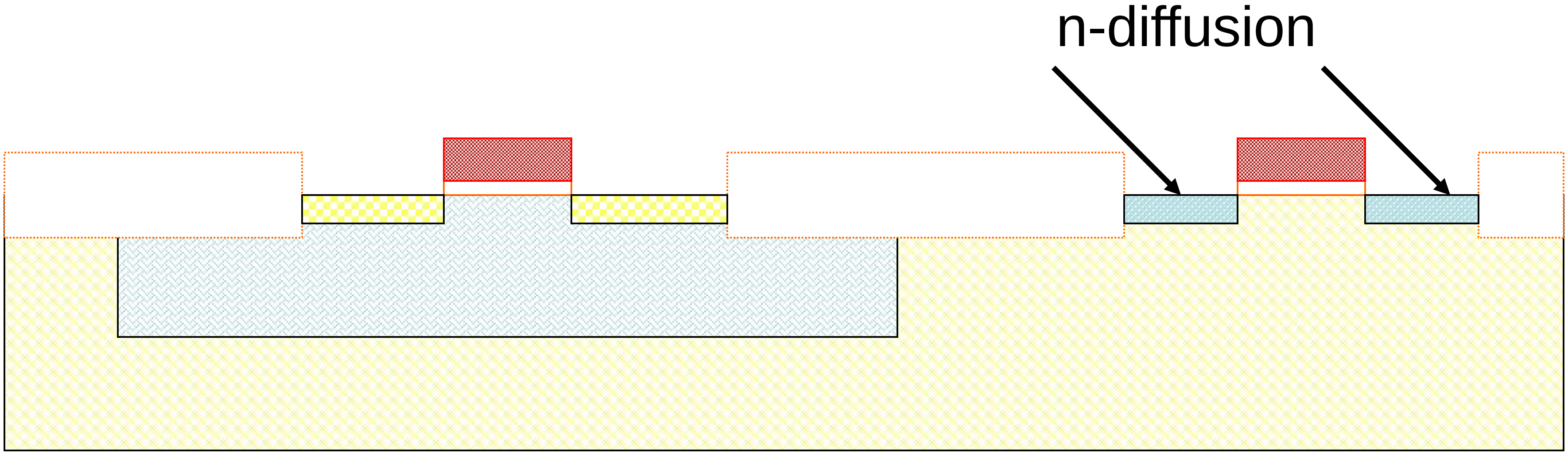
B-B’ Section

Note the gate is self aligned !!

n-Select Mask – n-diffusion



A-A' Section



B-B' Section

TABLE 2B.1

Process scenario of major process steps in typical n-well CMOS process[a]

1.	Clean wafer	
2.	GROW THIN OXIDE	
3.	Apply photoresist	
4.	PATTERN **n-well**	(MASK #1)
5.	Develop photoresist	
6.	Deposit and diffus n-type impurities	
7.	Strip photoresist	
8.	Strip thin oxide	
9.	Grow thin oxide	
10.	Apply layer of Si_3N_4	
11.	Apply photoresist	
12.	PATTERN Si_3N_4 (active area definition)	(MASK #2)
13.	Develop photoresist	
14.	Etch Si_3N_4	
15.	Strip photoresist	
	Optional field threshold voltage adjust	
	A.1 Apply photoresist	
	A.2 PATTERN ANTIMOAT IN SUBSTRATE	(MASK #A1)
	A.3 Develop photoresist	
	A.4 FIELD IMPLANT p-type)	
	A.5 Strip photoresist	
16.	GROW FIELD OXIDE	
17.	Strip Si_3N_4	
18.	Strip thin oxide	
19.	GROW GATE OXIDE	
20.	POLYSILICON DEPOSITION (POLY I)	
21.	Apply photoresist	
22.	PATTERN POLYSILICON	(MASK #3)
23.	Develop photoresist	
24.	ETCH POLYSILICON	

25.	Strip photoresist	
	Optional steps for double polysilicon process	
	B.1 Strip thin oxide	
	B.2 GROW THIN OXIDE	
	B.3 POLYSILICON DEPOSITION (POLY II)	
	B.4 Apply photoresist	
	B.5 PATTERN POLYSILICON	(MASK #B1)
	B.6 Develop photoresist	
	B.7 ETCH POLYSILICON	
	B.8 Strip photoresist	
	B.9 Strip thin oxide	
26.	Apply photoresist	
27.	PATTERN P-CHANNEL DRAINS AND SOURCES AND P^+ GUARD RINGS (p-well ohmic contacts)	(MASK #4)
28.	Develop photoresist	
29.	p^+ IMPLANT	
30.	Strip photoresist	
31.	Apply photoresist	
32.	PATTERN N-CHANNEL DRAINS AND SOURCES AND N^+ GUARD RINGS (top ohmic contact to substrate)	(MASK #5)
33.	Develop photoresist	
34.	n^+ IMPLANT	
35.	Strip photoresist	
36.	Strip thin oxide	
37.	Grow oxide	
38.	Apply photoresist	
39.	PATTERN CONTACT OPENINGS	(MASK #6)
40.	Develop photoresist	
41.	Etch oxide	
42.	Strip photoresist	

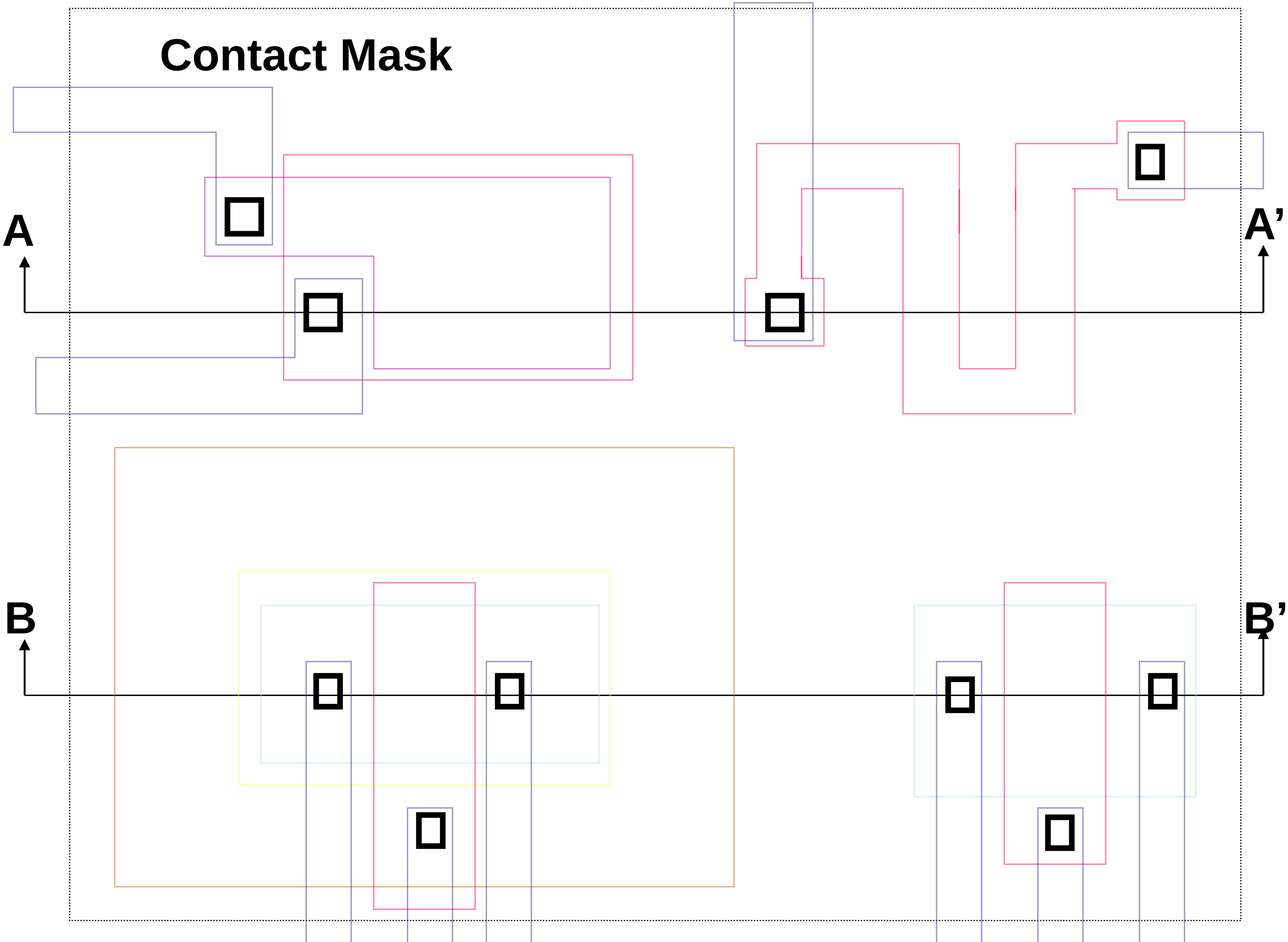
43. APPLY METAL
44. Apply photoresist
45. PATTERN METAL (MASK #7)
46. Develop photoresist
47. Etch metal
48. Strip photoresist

Optional steps for double metal process

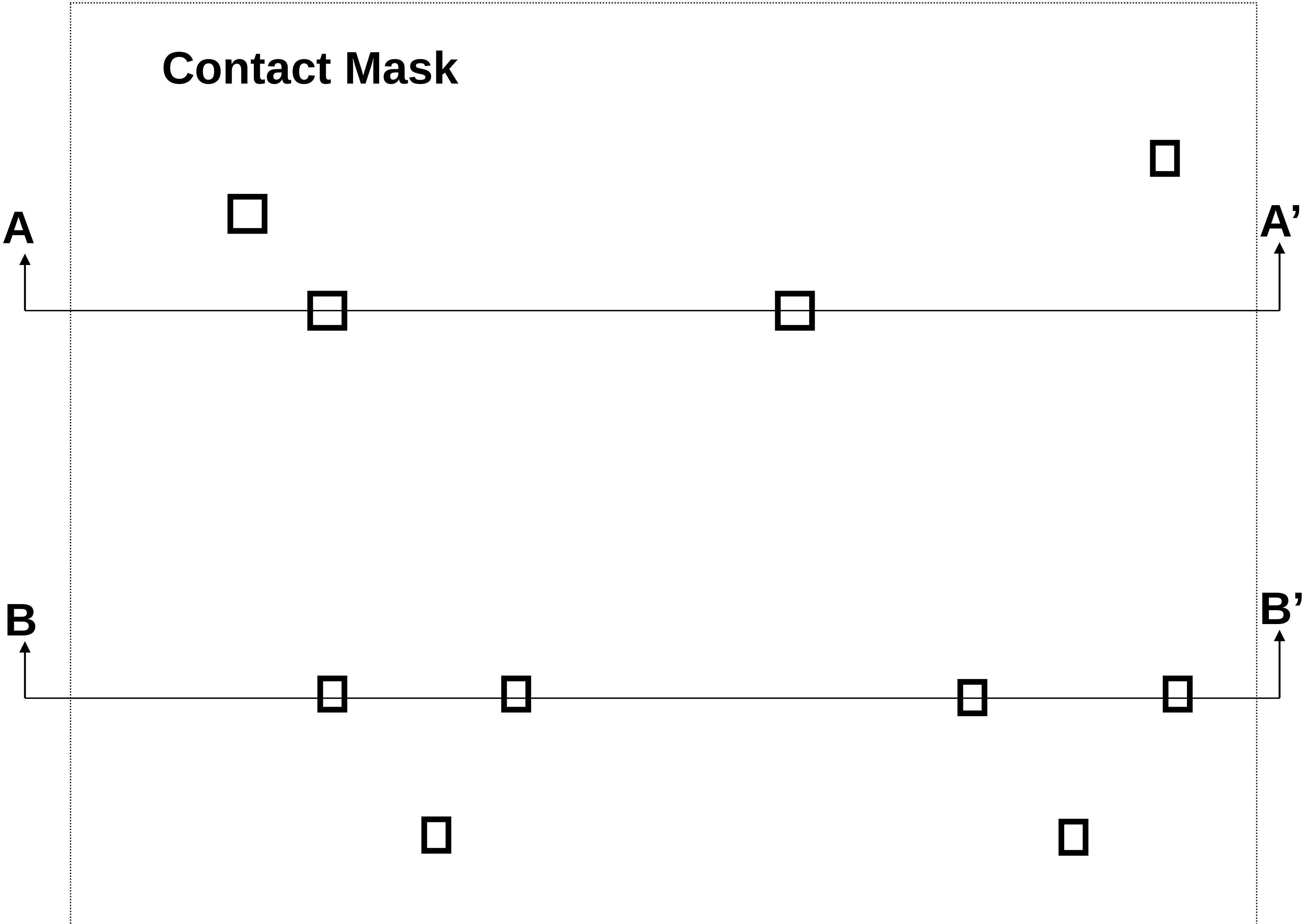
C.1 Strip thin oxide
C.2 DEPOSIT INTERMETAL OXIDE
C.3 Apply photoresist
C.4 PATTERN VIAS (MASK #C1)
C.5 Develop photoresist
C.6 Etch oxide
C.7 Strip photoresist
C.8 APPLY METAL (Metal 2)
C.9 Apply photoresist
C.10 PATTERN METAL (MASK #C2)
C.11 Develop photoresist
C.12 Etch metal
C.13 Strip photoresist

49. APPLY PASSIVATION
50. Apply photoresist
51. PATTERN PAD OPENINGS (MASK #8)
52. Develop photoresist
53. Etch passivation
54. Strip photoresist
55. ASSEMBLE, PACKAGE AND TEST

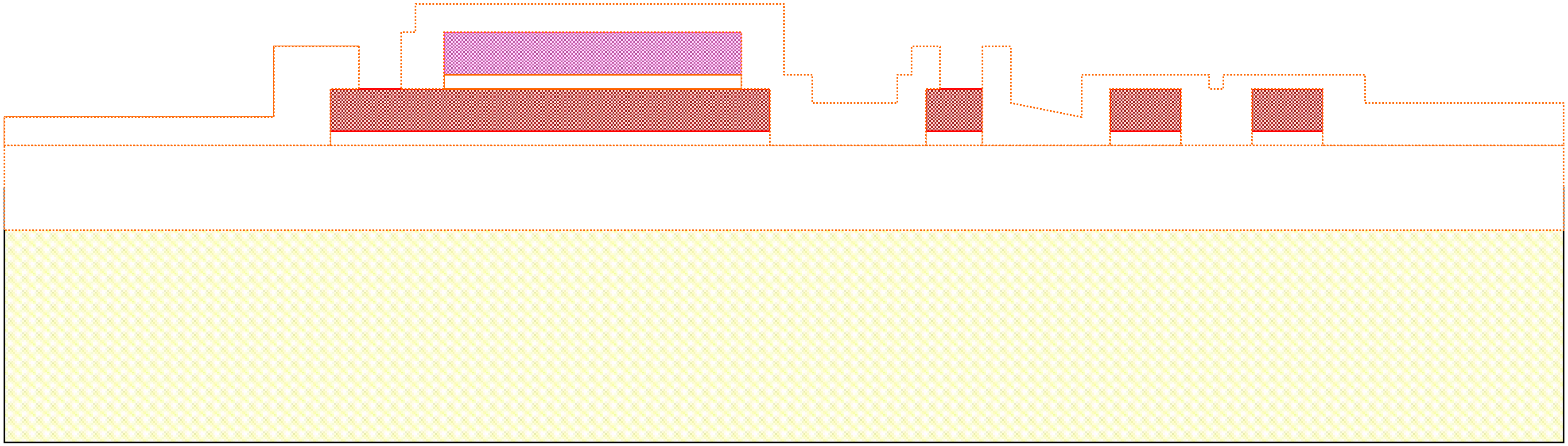
Contact Mask



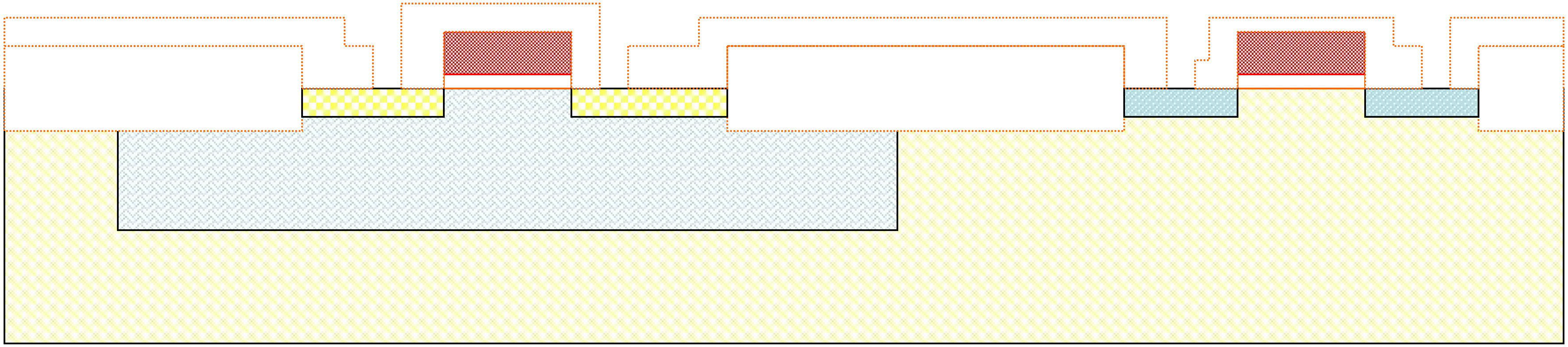
Contact Mask



Contact Mask



A-A' Section



B-B' Section

TABLE 2B.1

Process scenario of major process steps in typical n-well CMOS process[a]

1.	Clean wafer	
2.	GROW THIN OXIDE	
3.	Apply photoresist	
4.	PATTERN n-well	(MASK #1)
5.	Develop photoresist	
6.	Deposit and diffus n-type impurities	
7.	Strip photoresist	
8.	Strip thin oxide	
9.	Grow thin oxide	
10.	Apply layer of Si_3N_4	
11.	Apply photoresist	
12.	PATTERN Si_3N_4 (active area definition)	(MASK #2)
13.	Develop photoresist	
14.	Etch Si_3N_4	
15.	Strip photoresist	
	Optional field threshold voltage adjust	
	A.1 Apply photoresist	
	A.2 PATTERN ANTIMOAT IN SUBSTRATE	(MASK #A1)
	A.3 Develop photoresist	
	A.4 FIELD IMPLANT p-type)	
	A.5 Strip photoresist	
16.	GROW FIELD OXIDE	
17.	Strip Si_3N_4	
18.	Strip thin oxide	
19.	GROW GATE OXIDE	
20.	POLYSILICON DEPOSITION (POLY I)	
21.	Apply photoresist	
22.	PATTERN POLYSILICON	(MASK #3)
23.	Develop photoresist	
24.	ETCH POLYSILICON	

25. Strip photoresist

Optional steps for double polysilicon process

B.1 Strip thin oxide
B.2 GROW THIN OXIDE
B.3 POLYSILICON DEPOSITION (POLY II)
B.4 Apply photoresist
B.5 PATTERN POLYSILICON (MASK #B1)
B.6 Develop photoresist
B.7 ETCH POLYSILICON
B.8 Strip photoresist
B.9 Strip thin oxide

26. Apply photoresist
27. PATTERN P-CHANNEL DRAINS AND SOURCES AND P^+ GUARD RINGS (p-well ohmic contacts) (MASK #4)
28. Develop photoresist
29. p^+ IMPLANT
30. Strip photoresist
31. Apply photoresist
32. PATTERN N-CHANNEL DRAINS AND SOURCES AND N^+ GUARD RINGS (top ohmic contact to substrate) (MASK #5)
33. Develop photoresist
34. n^+ IMPLANT
35. Strip photoresist
36. Strip thin oxide
37. Grow oxide
38. Apply photoresist
39. PATTERN CONTACT OPENINGS (MASK #6)
40. Develop photoresist
41. Etch oxide
42. Strip photoresist

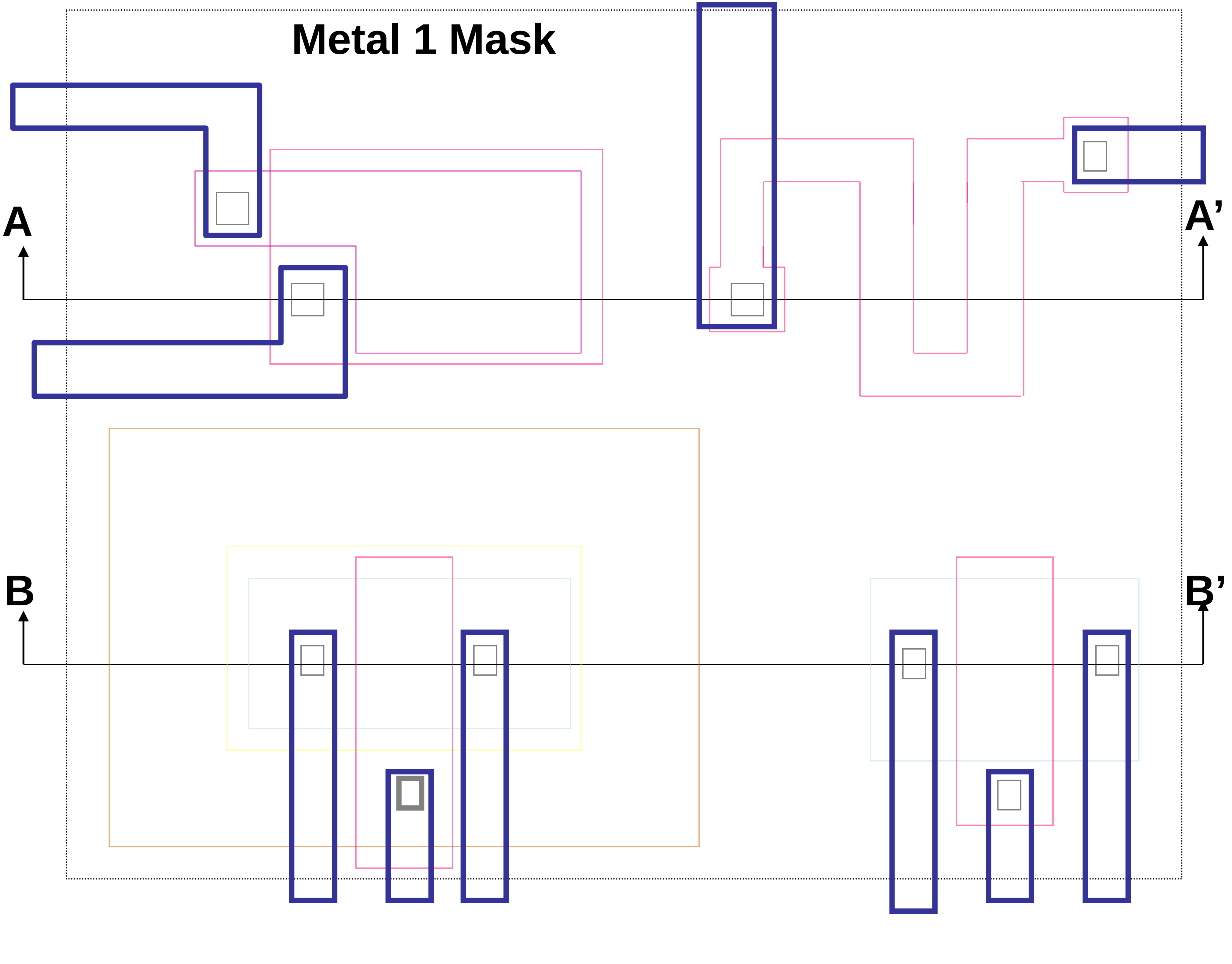
43. APPLY METAL
44. Apply photoresist
45. PATTERN METAL (MASK #7)
46. Develop photoresist
47. Etch metal
48. Strip photoresist

Optional steps for double metal process

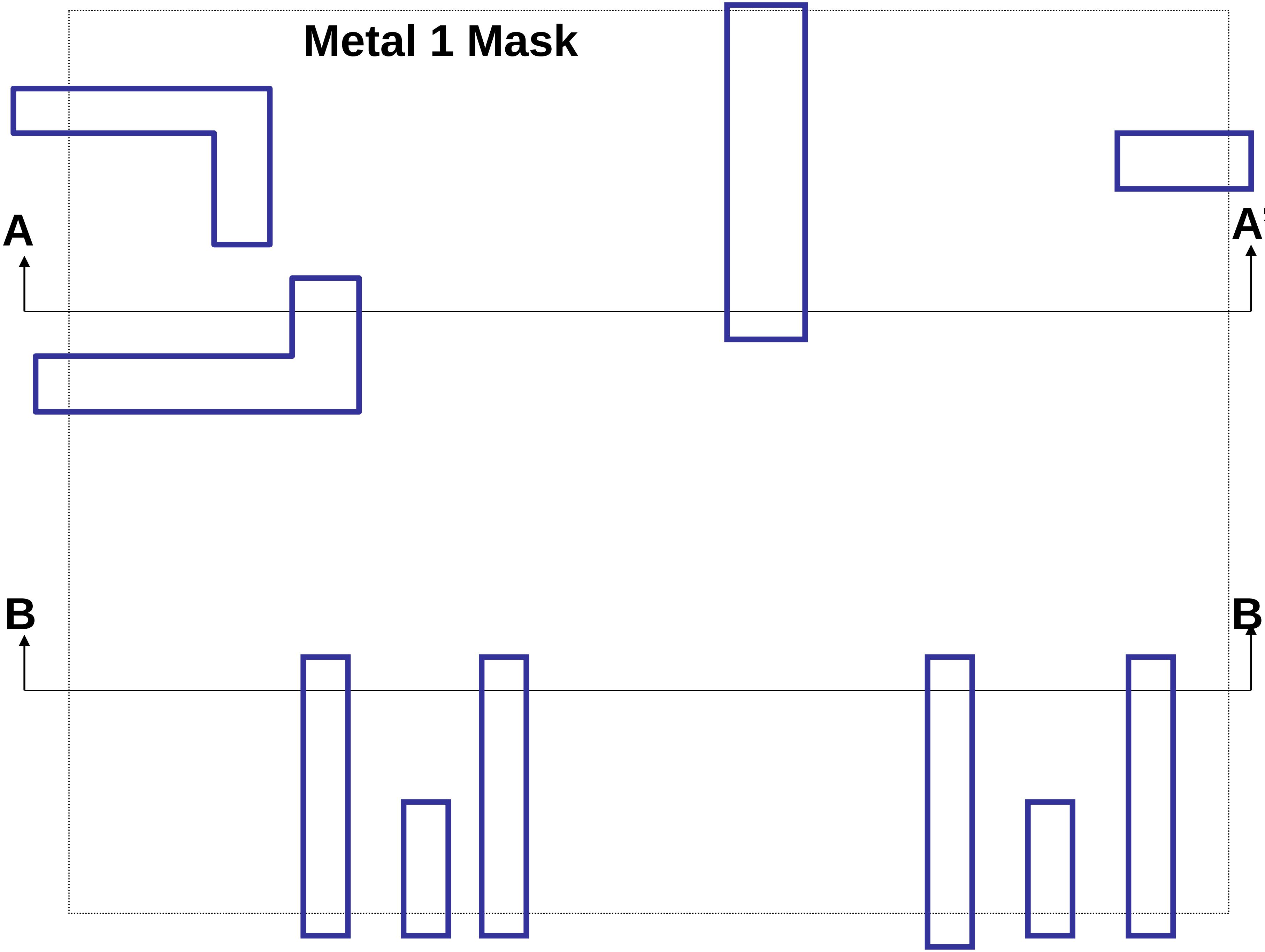
C.1 Strip thin oxide
C.2 DEPOSIT INTERMETAL OXIDE
C.3 Apply photoresist
C.4 PATTERN VIAS (MASK #C1)
C.5 Develop photoresist
C.6 Etch oxide
C.7 Strip photoresist
C.8 APPLY METAL (Metal 2)
C.9 Apply photoresist
C.10 PATTERN METAL (MASK #C2)
C.11 Develop photoresist
C.12 Etch metal
C.13 Strip photoresist

49. APPLY PASSIVATION
50. Apply photoresist
51. PATTERN PAD OPENINGS (MASK #8)
52. Develop photoresist
53. Etch passivation
54. Strip photoresist
55. ASSEMBLE, PACKAGE AND TEST

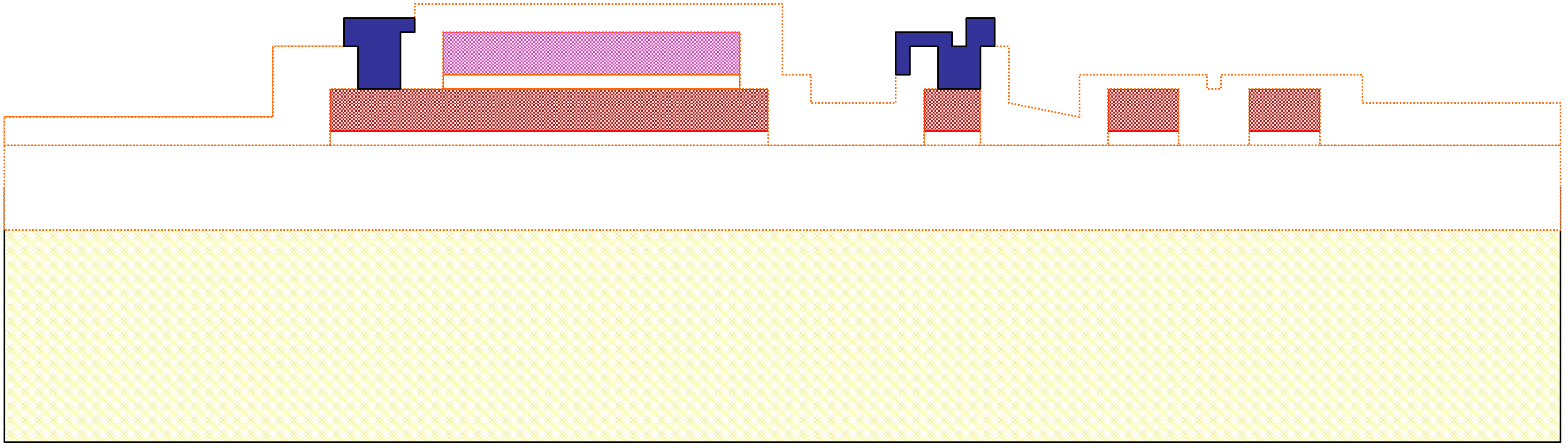
Metal 1 Mask



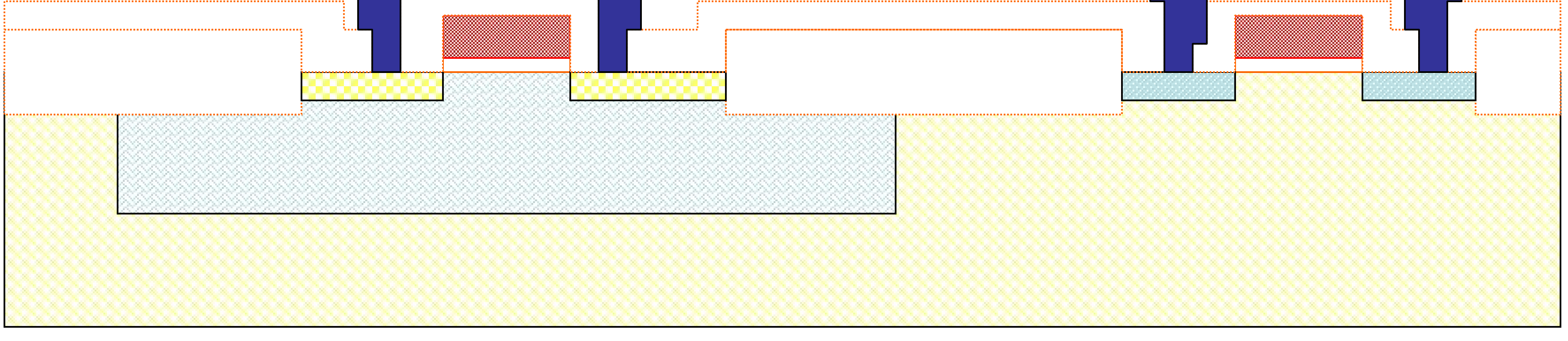
Metal 1 Mask



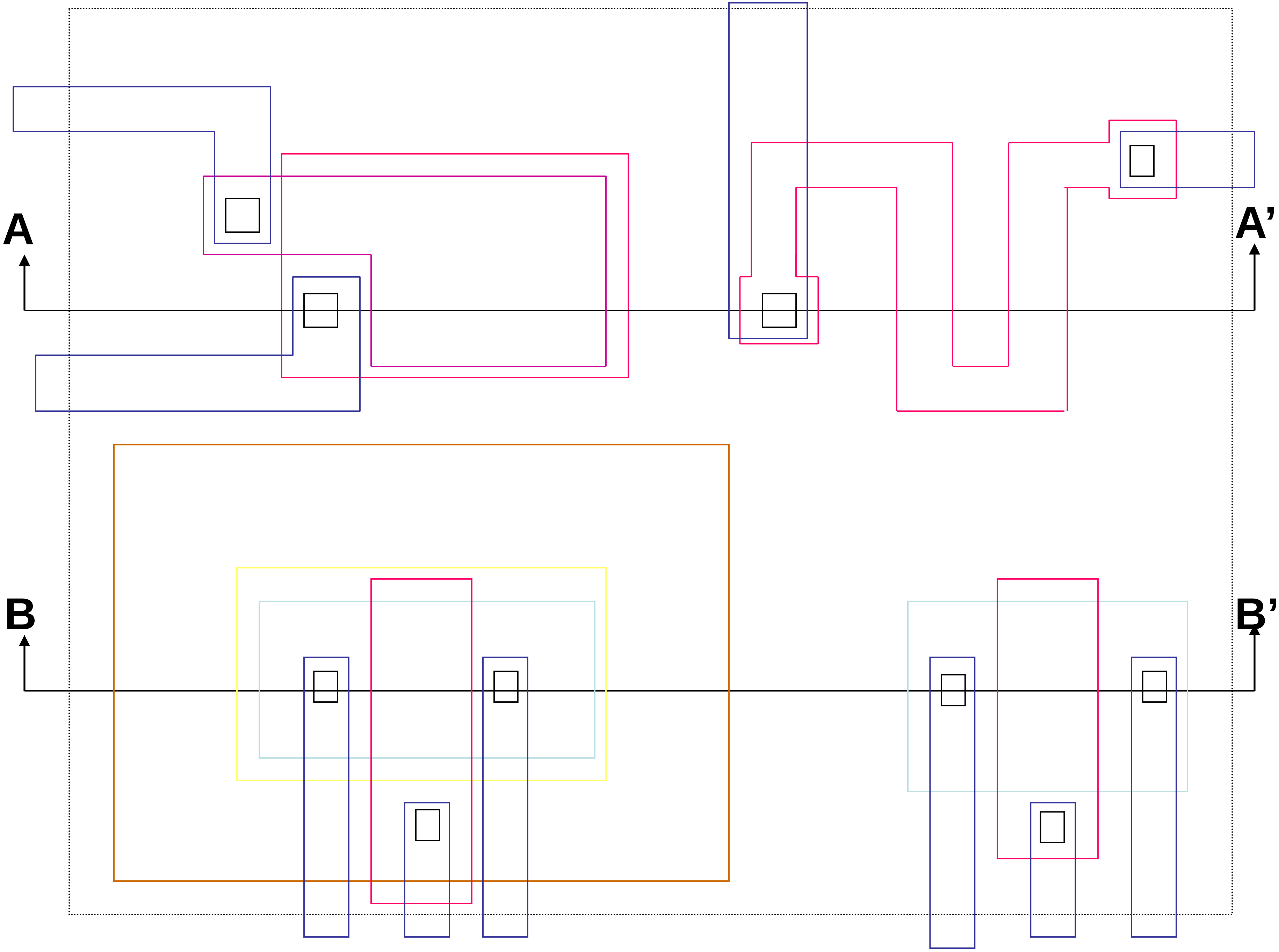
Metal Mask

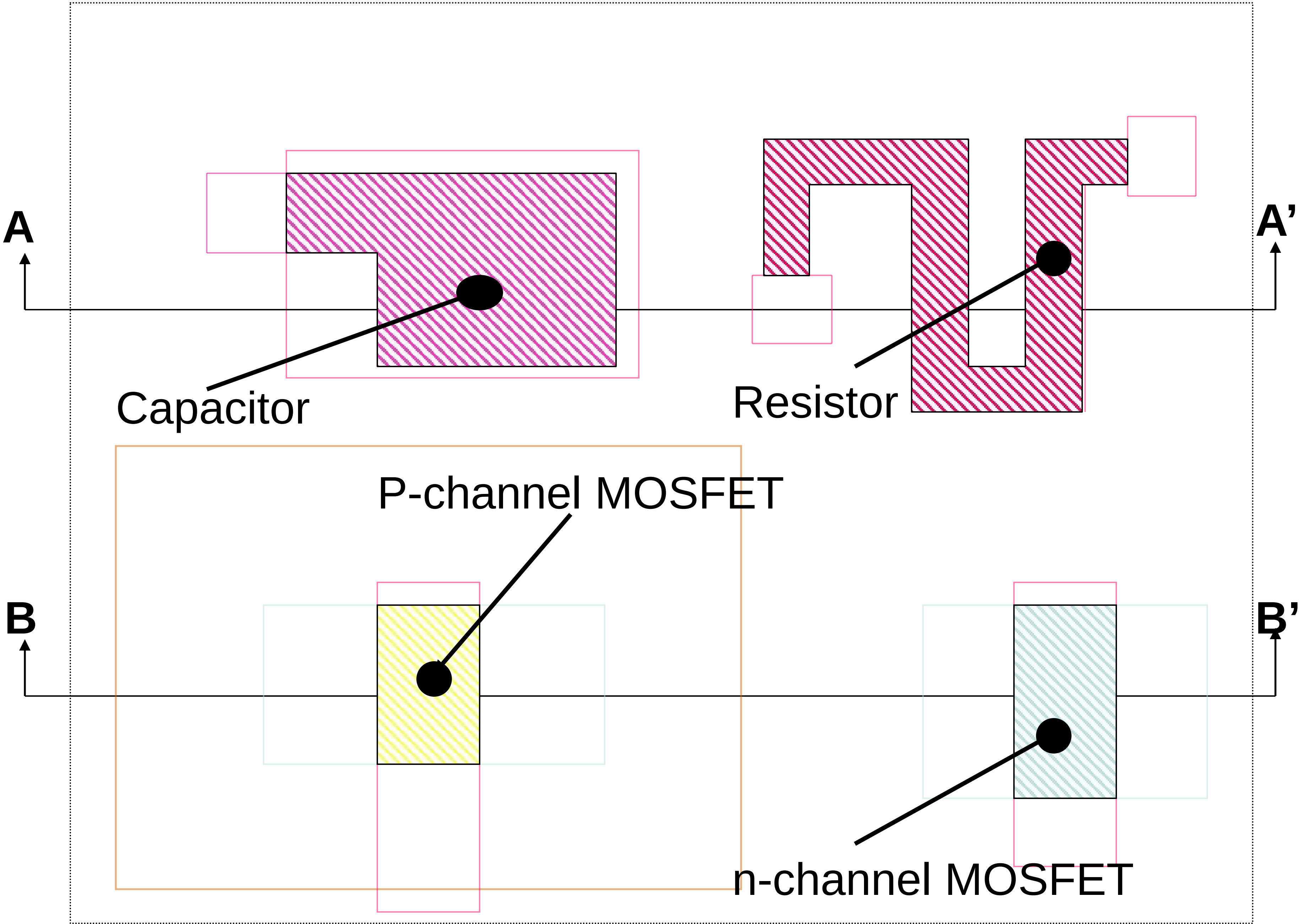


A-A' Section



B-B' Section


A
A'
B
B'


A
A’
Capacitor
Resistor
P-channel MOSFET
B
B’
n-channel MOSFET

Should now know what you can do in this process !!

Can metal connect to active?

Can metal connect to substrate when on top of field oxide?

How can metal be connected to substrate?

Can poly be connected to active under gate?

Can poly be connected to active any place?

Can metal be placed under poly to isolate it from bulk?

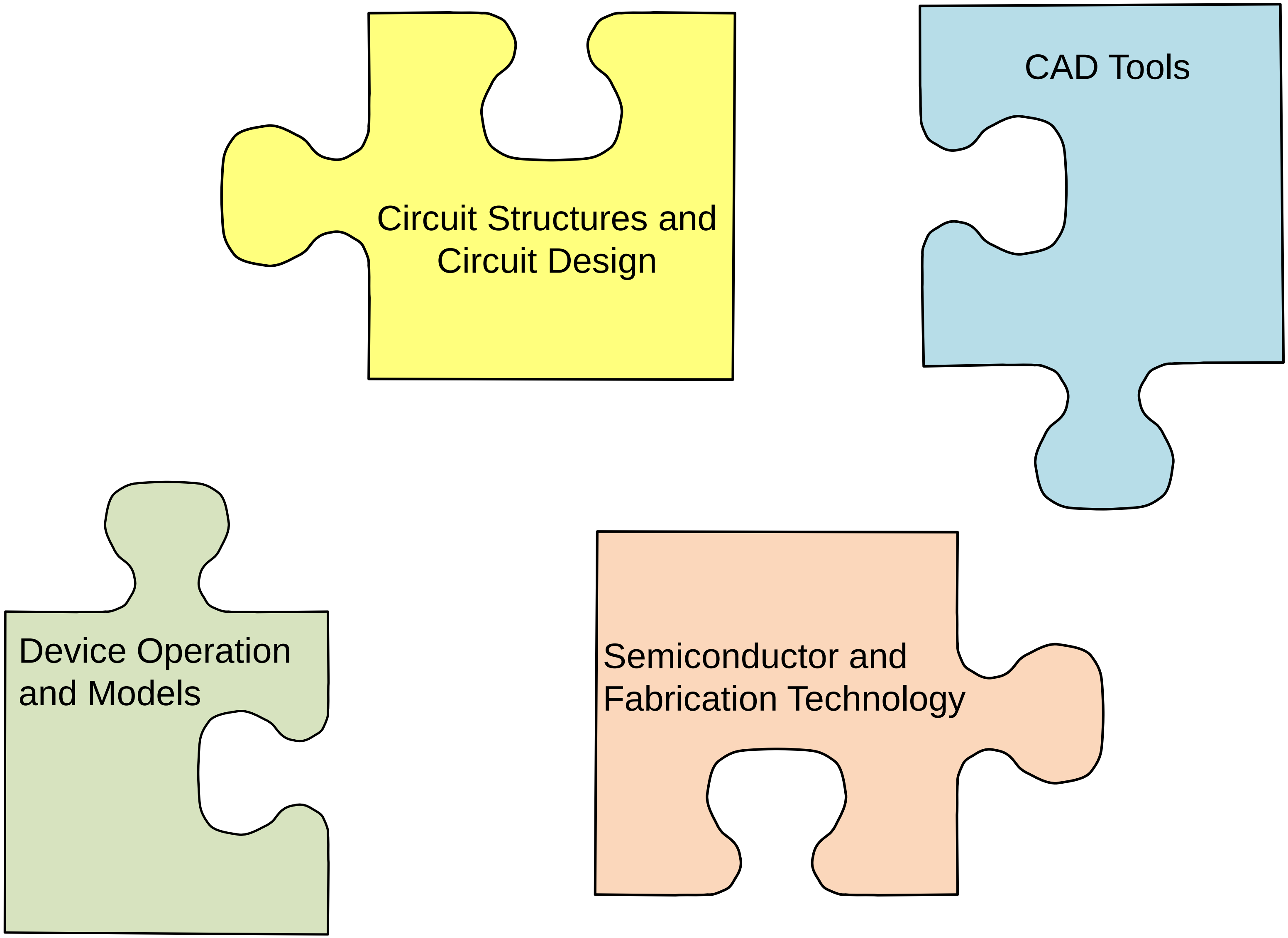
Can metal 2 be connected directly to active?

Can metal 2 be connected to metal 1?

Can metal 2 pass under metal 1?

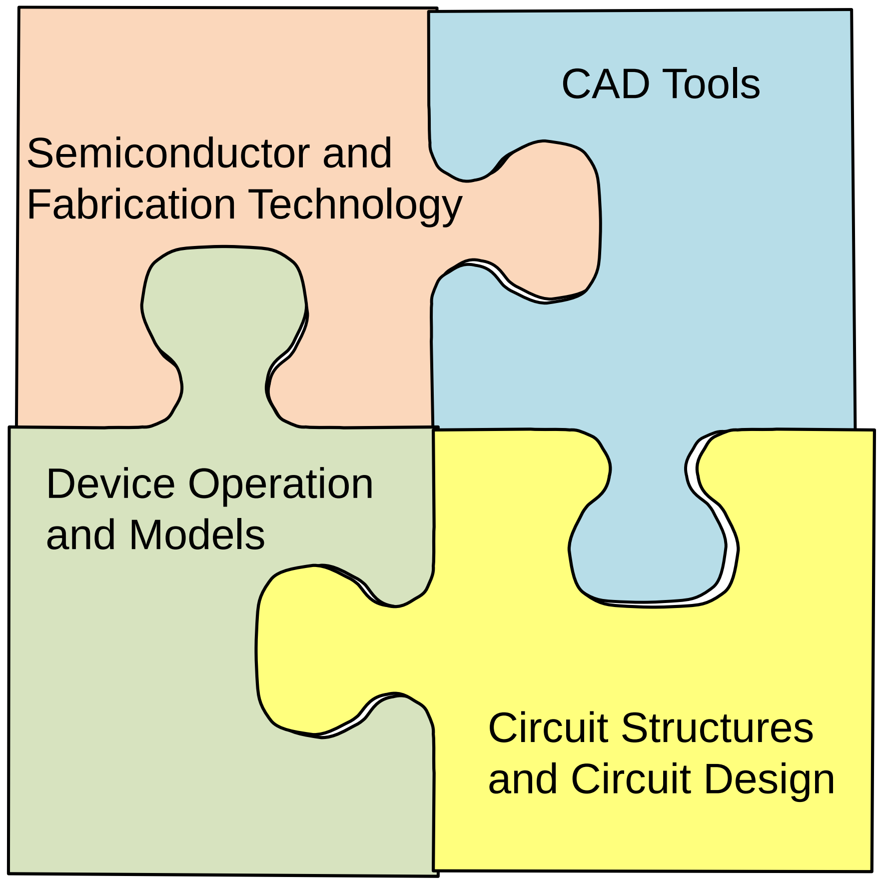
Could a process be created that will result in an answer of YES to most of above?

How we started this course

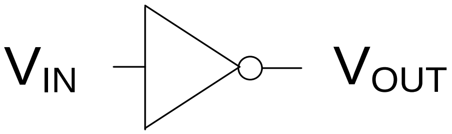


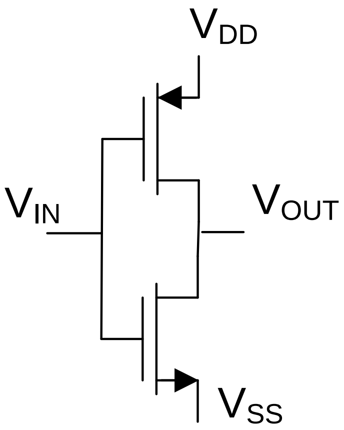
Thanks for your patience !!

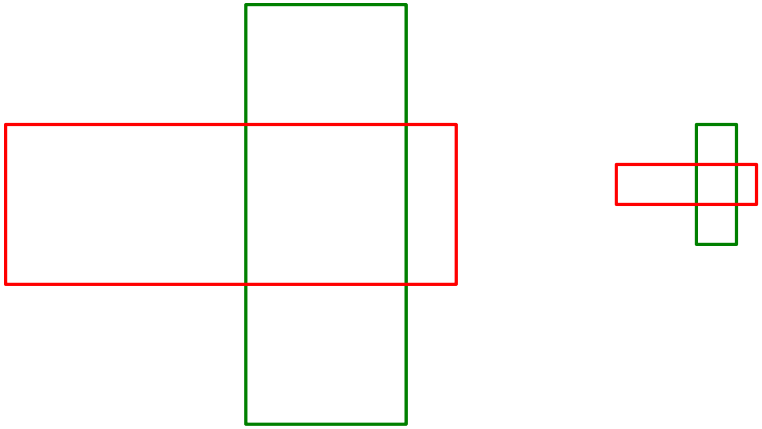
The basic concepts should have now come together



How does the inverter delay compare between a 0.5u process and a 0.18u process?







RUN: T91T VENDOR: AMIS
TECHNOLOGY: SCN05 FEATURE SIZE: 0.5 microns
Run type: SKD

INTRODUCTION: This report contains the lot average results obtained by MOSIS from measurements of MOSIS test structures on each wafer of this fabrication lot. SPICE parameters obtained from similar measurements on a selected wafer are also attached.

COMMENTS: American Microsystems, Inc. C5

TRANSISTOR PARAMETERS	W/L	N-CHANNEL	P-CHANNEL	UNITS
MINIMUM	3.0/0.6			
Vth		0.81	-0.92	volts
SHORT	20.0/0.6			
Idss		466	-250	uA/um
Vth		0.69	-0.89	volts
Vpt		12.7	-11.7	volts
WIDE	20.0/0.6			
Ids0		< 2.5	< 2.5	pA/um
LARGE	20.0/20.0			
Vth		0.71	-0.94	volts
Vjbkd		8.8	-11.7	volts
Ijlk		<50.0	<50.0	pA
Gamma		0.44	0.57	V^0.5
K' (Uo*Cox/2)		54.8	-19.7	uA/V^2
Low-field Mobility		434.84	156.32	cm^2/V*s

PROCESS PARAMETERS	N+	P+	POLY	PLY2_HR	M1	UNITS
Sheet Resistance	85.3	111.2	22.4	1033	0.09	ohms/sq
Contact Resistance	59.6	145.4	17.9			ohms
Gate Oxide Thickness	137					angstroms

CAPACITANCE PARAMETERS	N+	P+	POLY	POLY2	M1	UNITS
Area (substrate)	443	745	102			aF/um^2
Area (N+active)			2518			aF/um^2
Area (P+active)			2441			aF/um^2
Area (poly)				896	61	aF/um^2

CIRCUIT PARAMETERS		UNITS
Ring Oscillator Freq.		
DIV256 (31-stg,5.0V)	94.47	MHz
Ring Oscillator Power		
DIV256 (31-stg,5.0V)	0.48	uW/MHz/gate

MOSIS WAFER ACCEPTANCE TESTS

RUN: T4BK (MM_NON-EPI_THK-MTL)
TECHNOLOGY: SCN018

VENDOR: TSMC
FEATURE SIZE: 0.18 microns

INTRODUCTION: This report contains the lot average results obtained by MOSIS from measurements of MOSIS test structures on each wafer of this fabrication lot. SPICE parameters obtained from similar measurements on a selected wafer are also attached.

COMMENTS: DSCN6M018_TSMC

TRANSISTOR PARAMETERS	W/L	N-CHANNEL	P-CHANNEL	UNITS
MINIMUM	0.27/0.18			
Vth		0.50	-0.53	volts
SHORT	20.0/0.18			
Idss		571	-266	uA/um
Vth		0.51	-0.53	volts
Vpt		4.7	-5.5	volts
WIDE	20.0/0.18			
Ids0		22.0	-5.6	pA/um
LARGE	50/50			
Vth		0.42	-0.41	volts
Vjbkd		3.1	-4.1	volts
Ijlk		<50.0	<50.0	pA
K' (Uo*Cox/2)		171.8	-36.3	uA/V^2
Low-field Mobility		398.02	84.10	cm^2/V*s

CAPACITANCE PARAMETERS	N+	P+	POLY	M1	M2	M3	M4	M5	M6	R_W	D_N_W	M5P	N_W	UNITS
Area (substrate)	998	1152	103	39	19	13	9	8	3		129		127	aF/um^2
Area (N+active)			8566	54	21	14	11	10	9					aF/um^2
Area (P+active)			8324											aF/um^2
Area (poly)				64	18	10	7	6	5					aF/um^2
Area (metal1)					44	16	10	7	5					aF/um^2
Area (metal2)						38	15	9	7					aF/um^2
Area (metal3)							40	15	9					aF/um^2
Area (metal4)								37	14					aF/um^2
Area (metal5)									36			1003		aF/um^2
Area (r well)	987													aF/um^2
Area (d well)										574				aF/um^2
Area (no well)	139													aF/um^2
Fringe (substrate)	244	201		18	61	55	43	25						aF/um
Fringe (poly)				69	39	29	24	21	19					aF/um
Fringe (metal1)					61	35		23	21					aF/um
Fringe (metal2)						54	37	27	24					aF/um
Fringe (metal3)							56	34	31					aF/um
Fringe (metal4)								58	40					aF/um
Fringe (metal5)									61					aF/um
Overlap (P+active)			652											aF/um

CIRCUIT PARAMETERS			UNITS
Inverters	K		
Vinv	1.0	0.74	volts
Vinv	1.5	0.78	volts
Vol (100 uA)	2.0	0.08	volts
Voh (100 uA)	2.0	1.63	volts
Vinv	2.0	0.82	volts
Gain	2.0	-23.33	
Ring Oscillator Freq.			
D1024_THK (31-stg,3.3V)		338.22	MHz
DIV1024 (31-stg,1.8V)		402.84	MHz
Ring Oscillator Power			
D1024_THK (31-stg,3.3V)		0.07	uW/MHz/gate
DIV1024 (31-stg,1.8V)		0.02	uW/MHz/gate

End of Lecture 17