

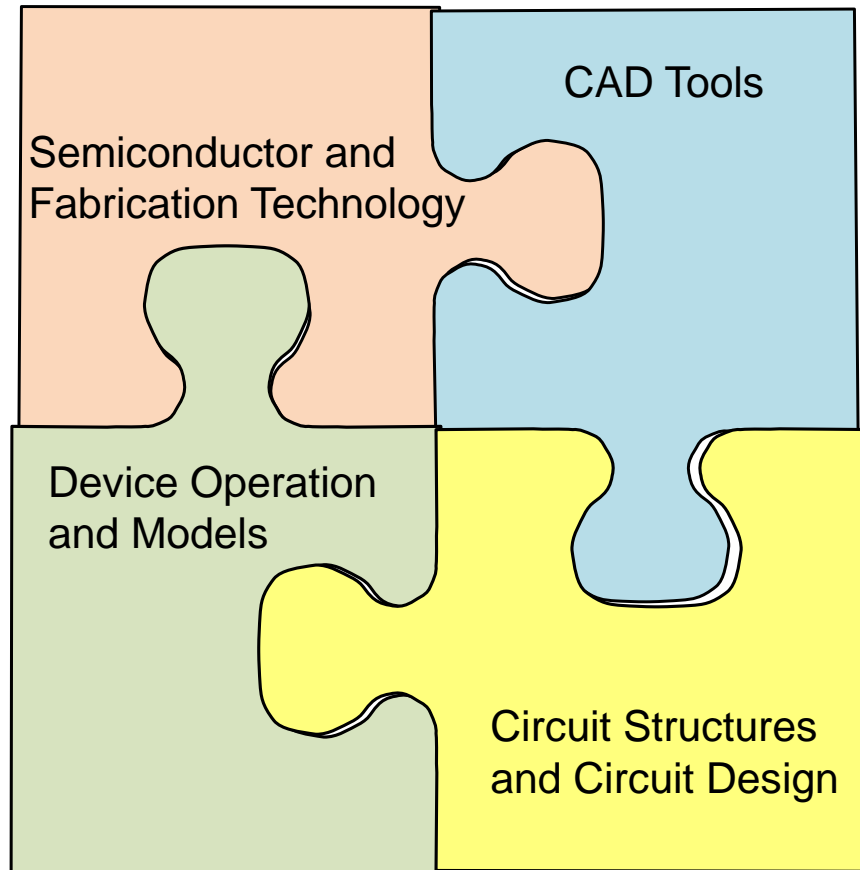
EE 330

Lecture 2

Basic Concepts

How Integrated Electronics will be Approached

After about four weeks, through laboratory experiments and lectures, the concepts should come together



Selected Semiconductor Trends

- Microprocessors
 - State of the art technology is now 10nm with over 20 Billion transistors on a chip
- DRAMS
 - State of the art is now 16G bits on a chip in a 10nm process which requires somewhere around 18 Billion transistors
- FPGA
 - FPGAs currently have over 50 Billion transistors with 7nm technology and are growing larger

Device count on a chip has been increasing rapidly with time, device size has been decreasing rapidly with time and speed/performance has been rapidly increasing

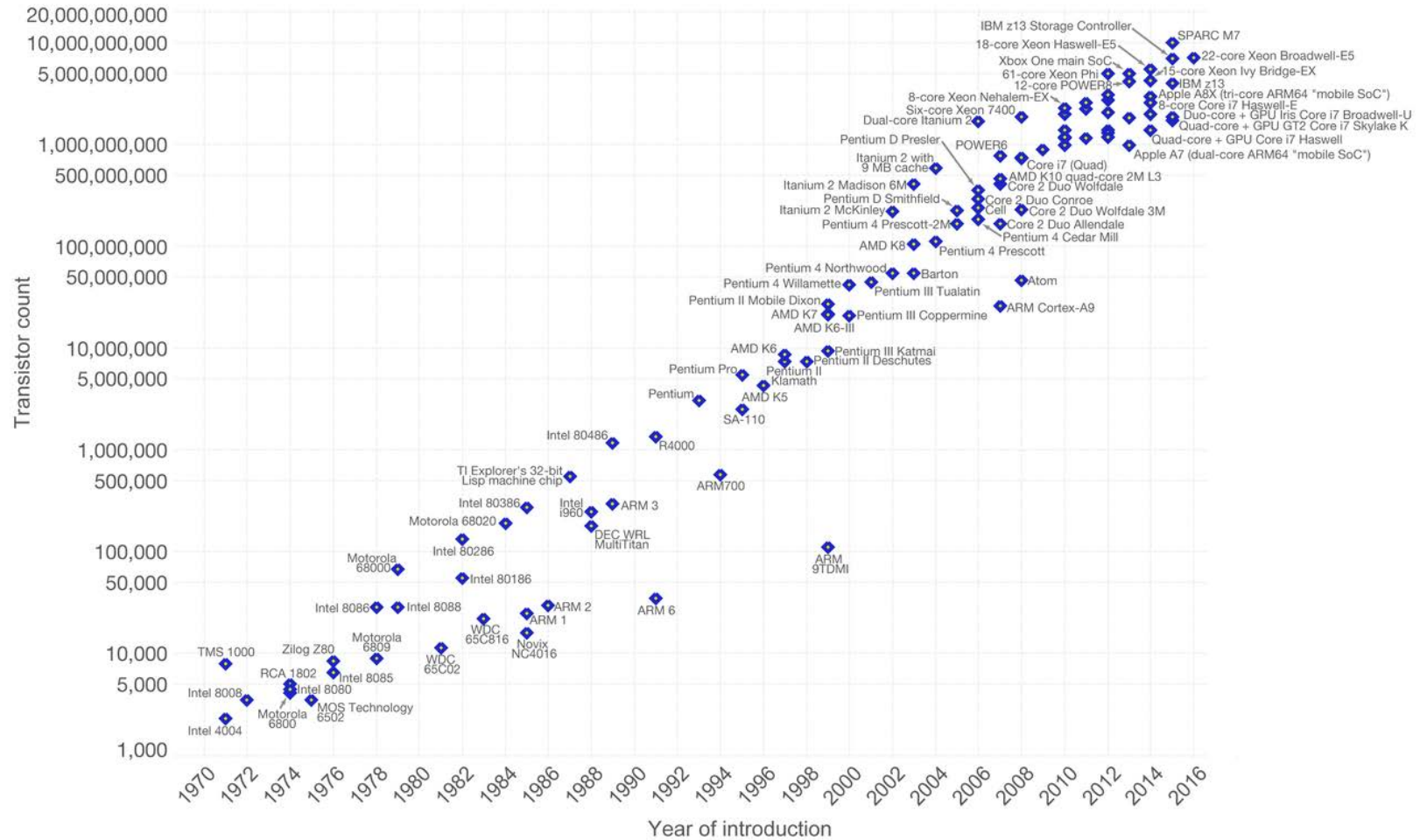
Moore's Law

From Webopedia (Aug 2016)

The observation made in 1965 by Gordon Moore, co-founder of [Intel](#), that the number of [transistors](#) per square inch on [integrated circuits](#) had doubled every year since the integrated circuit was invented. Moore predicted that this trend would continue for the foreseeable future. In subsequent years, the pace slowed down a bit, but [data](#) density has doubled approximately every 18 months, and this is the current definition of Moore's Law, which Moore himself has blessed. Most experts, including Moore himself, expect Moore's Law to hold for at least another two decades.

Moore's Law – The number of transistors on integrated circuit chips (1971-2016)

Moore's law describes the empirical regularity that the number of transistors on integrated circuits doubles approximately every two years. This advancement is important as other aspects of technological progress – such as processing speed or the price of electronic products – are strongly linked to Moore's law.



Data source: Wikipedia (https://en.wikipedia.org/wiki/Transistor_count)

The data visualization is available at [OurWorldinData.org](https://www.ourworldindata.org). There you find more visualizations and research on this topic.

Licensed under CC-BY-SA by the author Max Roser.

More on Moore's Law

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SEE HOW WITH open technologies.

START EXPLORING

Intelligent Machines

Moore's Law Is Dead. Now What?

Shrinking transistors have powered 50 years of advances in computing—but now other ways must be found to make computers more capable.

by Tom Simonite May 13, 2016

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TECH

End of Moore's Law: It's not just about physics

Moore's Law's End Reboots Industry | EE Times

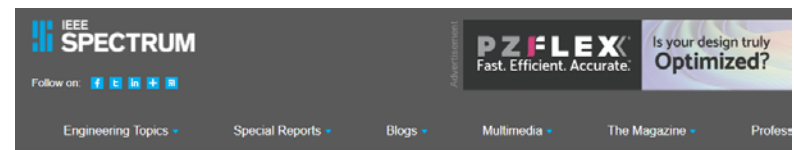
www.eetimes.com/document.asp?doc_id=1331941 ▼

Jun 26, 2017 - The expected death of **Moore's Law** will transform the ... four years, so were reaching the **end** of semiconductor technology as we know it," said ...

Moore's Law Running Out of Room, Tech Looks for a Successor - The ...

<https://www.nytimes.com/.../moores-law-running-out-of-room-tech-looks-for-a-successor...>

May 4, 2016 - "The **end** of **Moore's Law** is what led to this," said Thomas M. Conte, a Georgia Institute of Technology computer scientist and co-chairman of ...



News | Semiconductors | Devices

Transistors Could Stop Shrinking in 2021

A key industry report forecasts an end to traditional scaling of transistors

Posted 22 Jul 2016 | 13:04 GMT
By RACHEL COURTLAND

Moore's Law

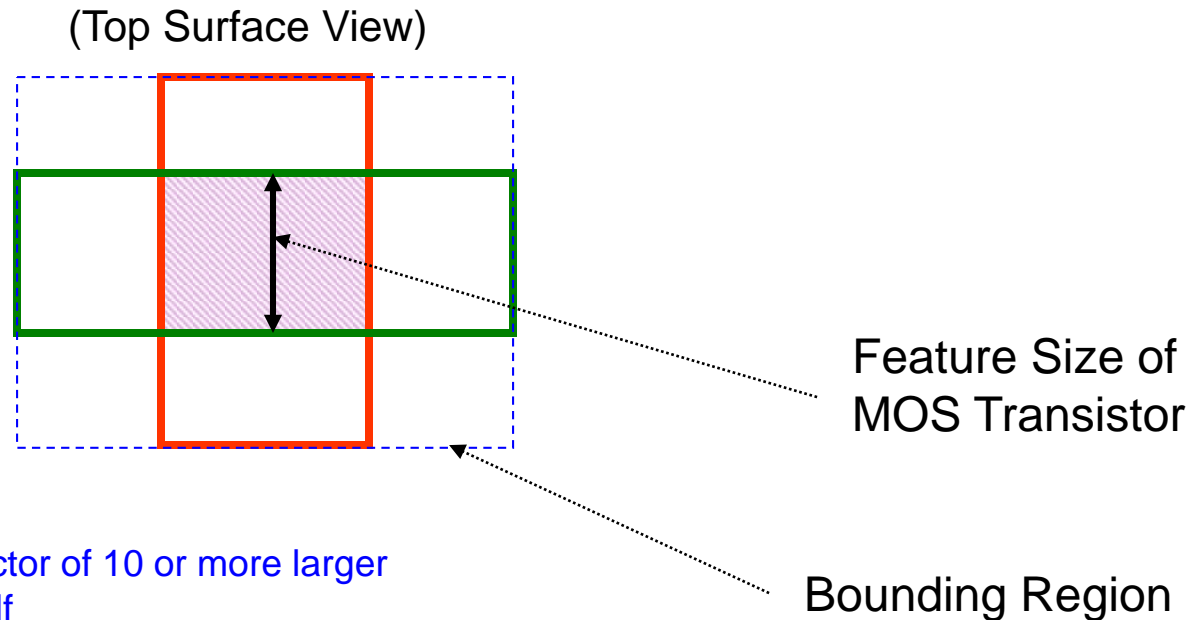
From Wikipedia (Aug 2017)

....However, in April 2016, Intel CEO Brian Krzanich stated that "In my 34 years in the semiconductor industry, I have witnessed the advertised death of Moore's Law no less than four times. As we progress from 14 nanometer technology to 10 nanometer and plan for 7 nanometer and 5 nanometer and even beyond, our plans are proof that Moore's Law is alive and well".^[25] In January 2017, he declared that "I've heard the death of Moore's law more times than anything else in my career ... And I'm here today to really show you and tell you that Moore's Law is alive and well and flourishing."^[26]

Today hardware has to be designed in a [multi-core](#) manner to keep up with Moore's law. In turn, this also means that software has to be written in a [multi-threaded](#) manner to take full advantage of the hardware.

Feature Size

The feature size of a process generally corresponds to the minimum lateral dimensions of the transistors that can be fabricated in the process



- Bounding region often a factor of 10 or more larger than area of transistor itself
- This along with interconnect requirements and sizing requirements throughout the circuit create an area overhead factor of 10x to 100x

Moore's Law

(from Wikipedia)

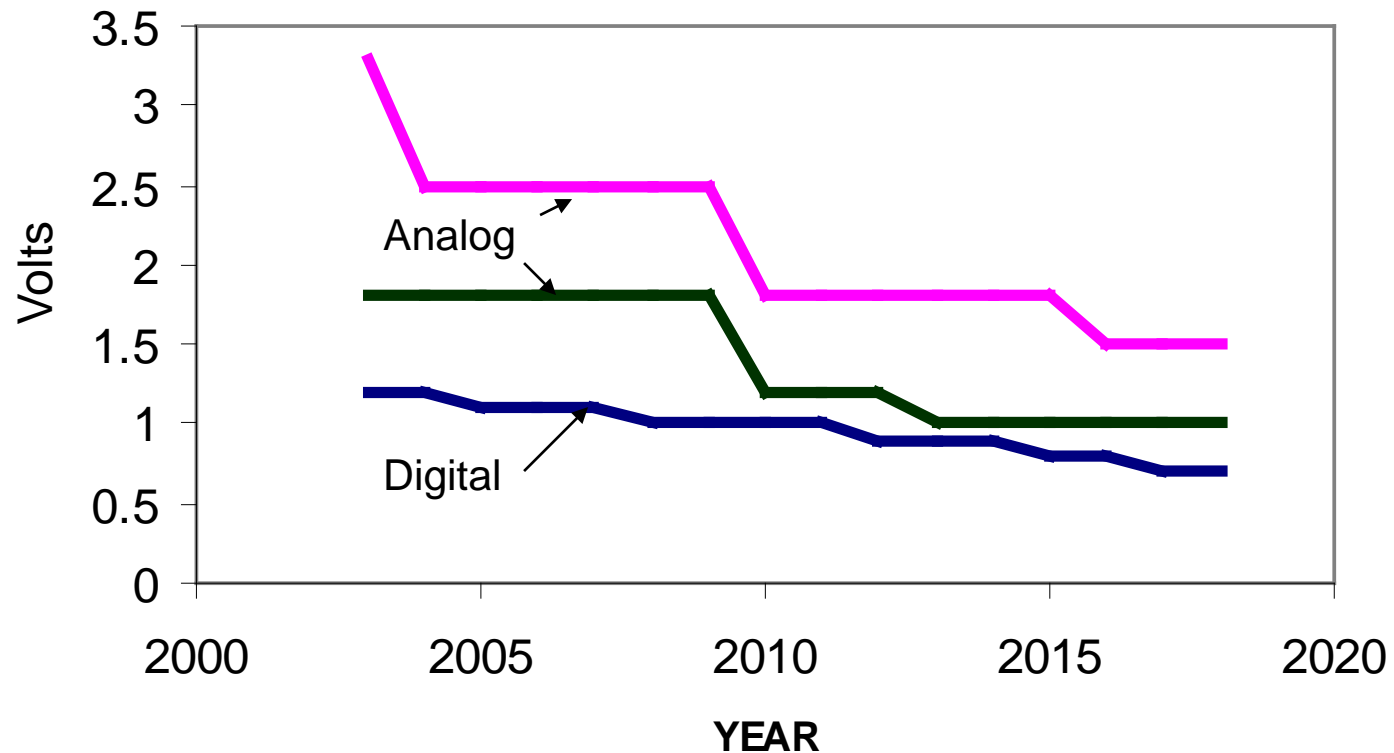
Moore's law is the [empirical](#) observation that the [complexity](#) of [integrated circuits](#), with respect to minimum component cost, doubles every 24 months[\[1\]](#). It is attributed to [Gordon E. Moore\[2\]](#), a co-founder of [Intel](#).

- Observation, not a physical law
- Often misinterpreted or generalized
- Many say it has been dead for several years
- Many say it will continue for a long while
- Not intended to be a long-term prophecy about trends in the semiconductor field
- Something a reporter can always comment about when they have nothing to say!

Device scaling, device count, circuit complexity, device cost, ... in leading-edge processes will continue to dramatically improve (probably nearly geometrically with a time constant of around 2 years) for the foreseeable future !!

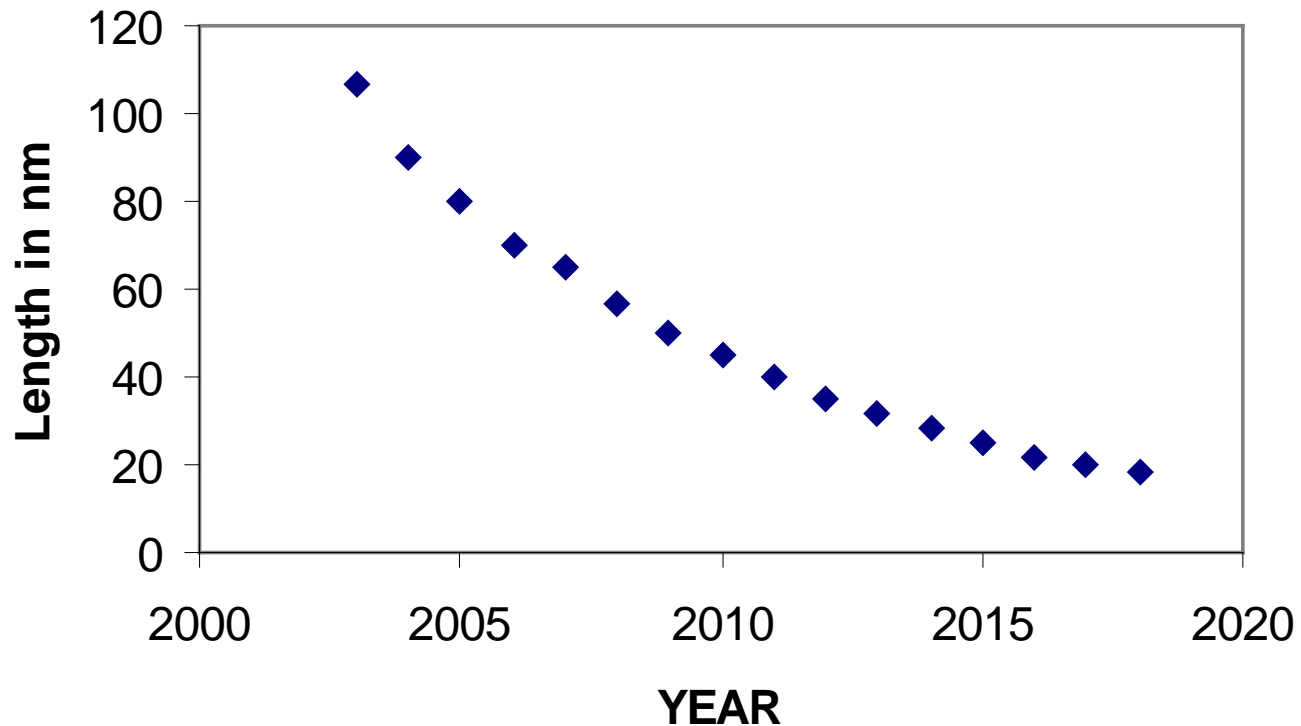
ITRS Technology Predictions

ITRS Supply Voltage Predictions



ITRS Technology Predictions

Minimum ASIC Gate Length



Challenges

- Managing increasing device count
- Short lead time from conception to marketplace
- Process technology advances
- Device performance degradation
- Increasing variability
- Increasing pressure for cost reduction
- Power dissipation

Future Trends and Opportunities

- Is there an end in sight?

No ! But the direction the industry will follow is not yet known and the role semiconductor technology plays on society will increase dramatically!

- Will engineers trained in this field become obsolete at mid-career ?

No ! Engineers trained in this field will naturally evolve to support the microelectronics technology of the future. Integrated Circuit designers are now being trained to efficiently manage enormous levels of complexity and any evolutionary technology will result in even larger and more complexity systems with similar and expanded skills being required by the engineering community with the major changes occurring only in the details.

Future Trends and Opportunities

- Will engineers trained in this field be doing things the same way as they are now at mid-career?

No ! There have been substantive changes in approaches every few years since 1965 and those changes will continue. Continuing education to track evolutionary and revolutionary changes in the field will be essential to remain productive in the field.

- What changes can we expect to see beyond the continued geometric growth in complexity (capability) ?

That will be determined by the creativity and marketing skills of those who become immersed in the technology. New “Gordon Moores”, “Bill Gates” and “Jim Dells” will evolve.

Creation of Integrated Circuits

Most integrated circuits are comprised of transistors along with a small number of passive components and maybe a few diodes

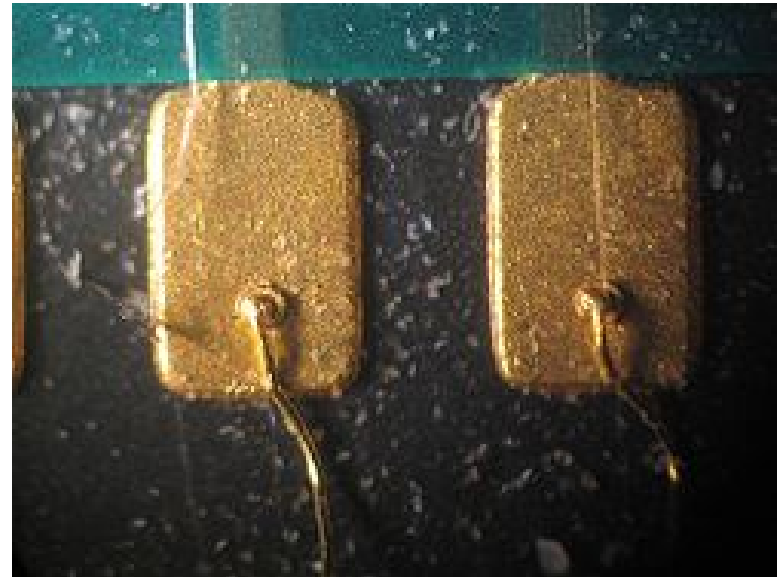
This course will focus on understanding how transistors operate and on how they can be interconnected and possibly combined with a small number of passive components to form useful integrated circuits

Wire Sizes for Electrical Interconnects



50 A Range Cord

6 ga Wiring 0.162 in diameter



25um Gold Bonding Wire

Leading Analog IC Suppliers (\$M)

2014 Rank	Company	2013	2014	% Change	% Marketshare
1	Texas Instruments	7,194	8,104	13%	18%
2	ST	2,775	2,836	2%	6%
3	Infineon	2,550	2,770	9%	6%
4	Analog Devices	2,409	2,615	9%	6%
5	Skyworks Solutions	1,807	2,570	42%	6%
6	Maxim	2,055	2,035	-1%	4%
7	NXP	1,430	1,730	21%	4%
8	Linear Technology	1,317	1,437	9%	3%
9	ON Semi	1,239	1,291	4%	3%
10	Renesas	975	910	-7%	2%

Source: IC Insights, company reports

Selected Observations about Semiconductor Companies

ANALOG IC SUPPLIER RANKING				
Rank	Gartner 1995	IC Insights 2015	Revenues (US\$ billions)	SC-IQ forecast 2016
1	ST	TI	8.34	TI
2	Philips	Infineon	2.89	ADI
3	National	Skyworks	2.70	Infineon
4	Motorola	ADI	2.67	Skyworks
5	TI	ST	2.47	ST
6	Toshiba	Maxim	1.96	Maxim
7	Sanyo	NXP	1.91	NXP
8	ADI	LTC	1.44	ON
9	Siemens	ON	1.16	Renesas
10	NEC	Renesas	0.81	MediTek

Sam Davis 2 | Oct 05, 2016

From following WEB site, Aug 23, 2017

<http://www.powerelectronics.com/blog/shakeup-analog-ic-rankings>

Selected Semiconductor Company Profiles

(with Iowa ties)

Texas Instruments:

- World's largest producer of analog semiconductors at \$8.2B, over 100% larger than closest competitor
- Ranks 1st in DSP
- Ranks 7th in World in semiconductor sales

Number of employees: 30,000

2015 sales: \$13.0B

2015 income: \$3.0B

(after taxes)

Average annual sales/employee: \$433K

Average annual earnings/employee: \$100K



Jerry Junkins

Past CEO of TI
ISU EE Class of '59

Selected Semiconductor Company Profiles

(with Iowa ties)

Intel:

World's largest producer of semiconductors

Cofounders: Robert Noyce and Gordon Moore

Number of employees (Dec '13) : 108,000

2013 sales: \$53B

2013 income: \$12.6B

Average annual sales/employee: \$490K

Average annual earnings/employee: \$117K



Robert Noyce
BA Grinnell 1949

Noyce is also the co-inventor of the integrated circuit !

Selected Semiconductor Company Profiles

(with Iowa ties)

Marvell:

Cofounders: Sehat Sutardja (CEO), Welli Dai and Pantas Sutardja

Number of employees: 7200

2015 sales: \$3.7B

2015 income: \$435M

Average annual sales/employee: \$513K

Average annual earnings/employee: \$60K

Fabless Semiconductor Company



Sehat Sutardja

BSEE ISU
(approx 1985)

Selected Semiconductor Company Profiles

(with Iowa ties)

Maxim: Founded in April 1983, profitable every year since 1987

Tunc Doluca joined Maxim in October 1984,
appointed President and CEO in 2007

Number of employees: 9200

2013 sales: \$2.5B

2013 income: \$409M

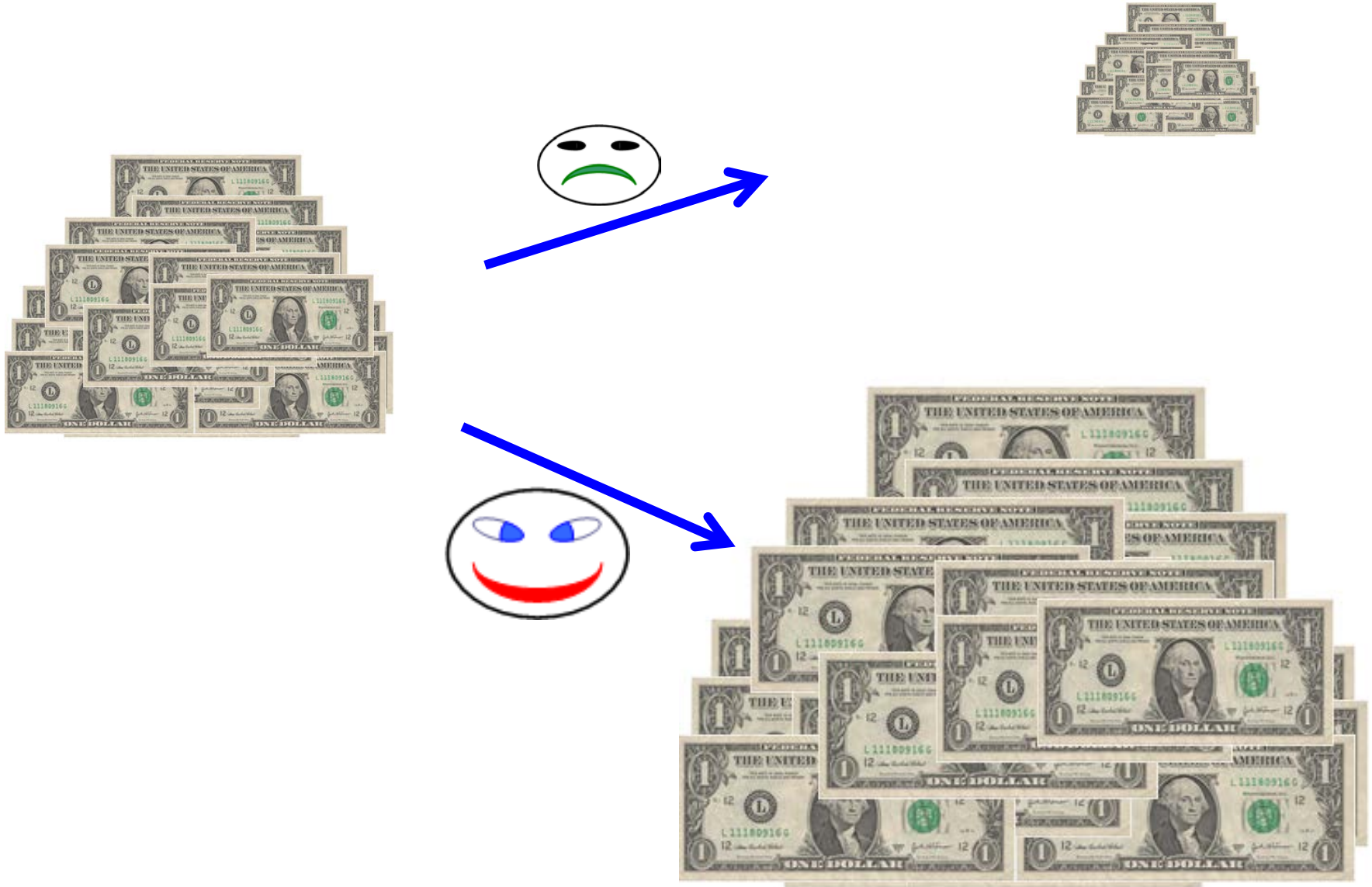
Average annual sales/employee: \$272K

Average annual earnings/employee: \$45K



Tunc Doluca
BSEE IASTATE
(1979)

Considerable Cash Flow Inherent in the Semiconductor Industry



Essentially All Activities Driven by Economic Considerations



- Many Designs Cost Tens of Millions of Dollars
- Mask Set and Production of New Circuit Approaching \$2 Million
- New Foundries Costs Approaching \$10 Billion (few players in World can compete)
- Many Companies Now Contract Fabrication (Fabless Semiconductor Companies)
- Time to Market is Usually Critical
- Single Design Error Often Causes Months of Delay and Requires New Mask Set
- Potential Rewards in Semiconductor Industry are Very High

Will emphasize economic considerations throughout this course

Understanding of the Big Picture is Critical



Solving Design Problems can be Challenging

Be sure to solve the right problem !



How can complex circuits with a very large number of transistors be efficiently designed with low probability of error?

 Many designers often work on a single design

 Single error in reasoning, in circuit design, or in implementing circuit on silicon generally results in failure

- Design costs and fabrication costs for test circuits are very high
 - Design costs for even rather routine circuits often a few million dollars and some much more
 - Masks and processing for state of the art processes often between \$1M and \$2M
- Although much re-use is common on many designs, considerable new circuits that have never been designed or tested are often required
- Time to market critical – missing a deadline by even a week or two may kill the market potential

Single Errors Usually Cause Circuit Failure

- How many components were typical of lab experiments in EE 201 and EE 230?
- Has anyone ever made an error in the laboratory of these courses ? (wrong circuit, incomplete understanding, wrong wiring, wrong component values, imprecise communication, frustration)
- How many errors are made in a typical laboratory experiment in these courses?
- How many errors per hour might have occurred?

Single Errors Usually Cause Circuit Failure

Consider an extremely complicated circuit

- with requirements to do things that have never been done before
- with devices that are not completely understood
- that requires several billion transistors
- that requires 200 or more engineers working on a project full-time for 3 years
- with a company investment of many million dollars
- with an expectation that nobody makes a single error

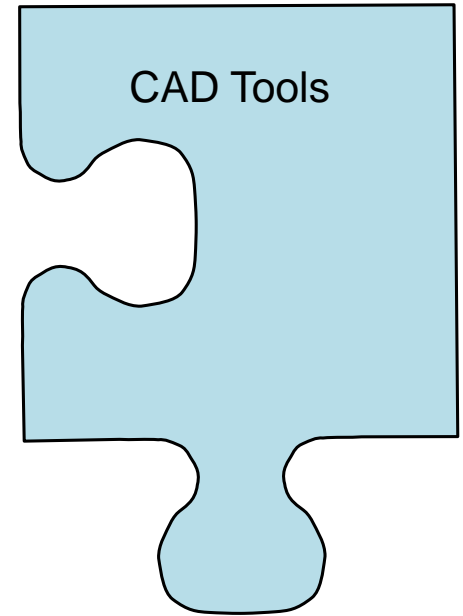
Is this a challenging problem for all involved?

How can complex circuits with a very large number of transistors be efficiently designed with low probability of error?

- CAD tools and CAD-tool environment critical for success today
- Small number of VLSI CAD toolset vendors
- CAD toolset helps the engineer and it is highly unlikely the CAD tools will replace the design engineer
- An emphasis in this course is placed on using toolset to support the design process

CAD Environment for Integrated Circuit Design

- Typical Tool Flow
 - (See Chapter 14 of Text)
- Laboratory Experiments in Course



System Description

A diagram illustrating the process flow. A black box labeled "SPICE" has a red arrow pointing to a dashed red box labeled "Simulation Results". A red line also connects the "Simulation Results" box back to the "SPICE" box, forming a loop.

SPICE Simulation

Layout/DRC...

LVS

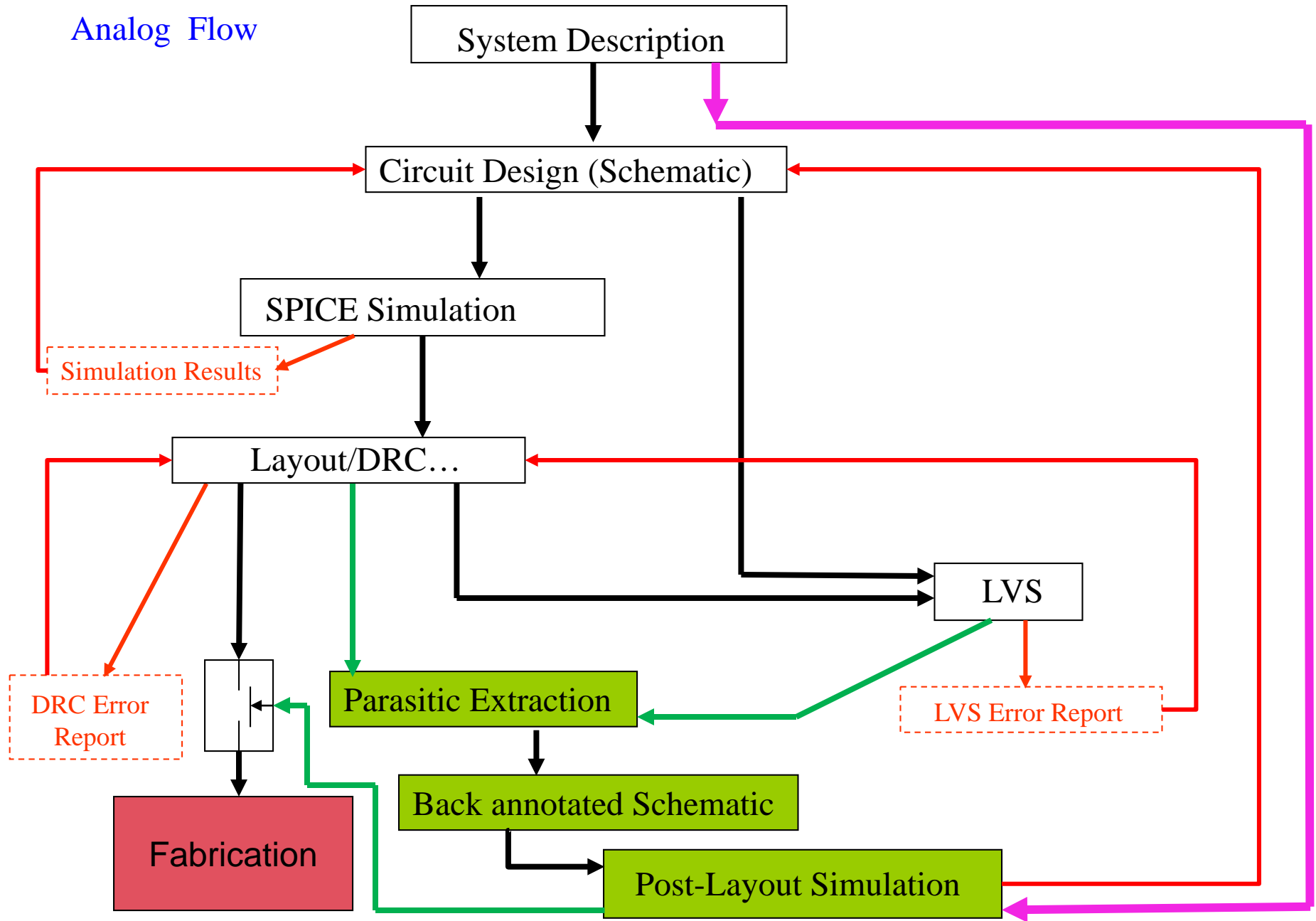
LVS Error Report

Parasitic Extraction

Back annotated Schematic

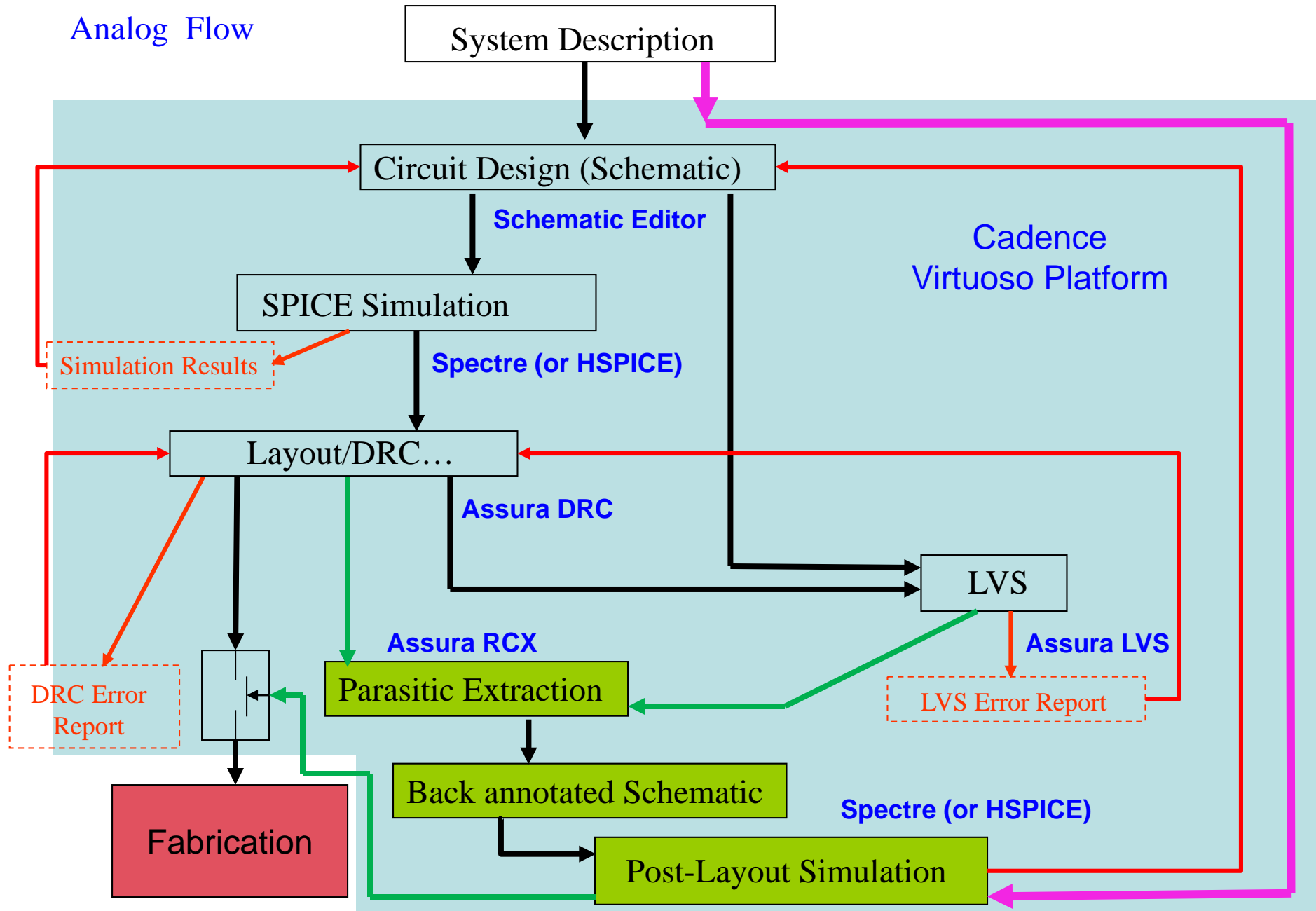
Post-Layout Simulation

Fabrication

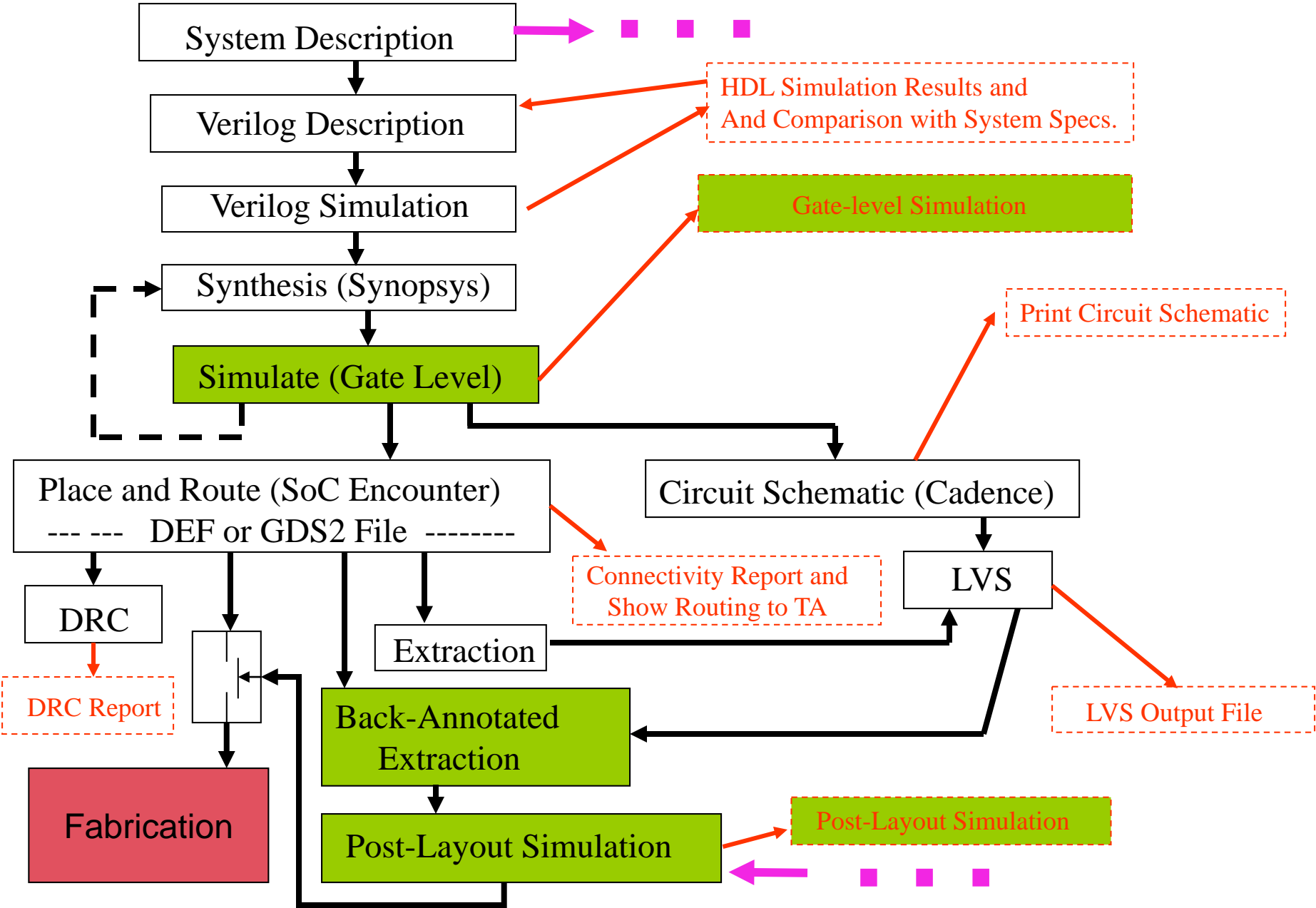


VLSI Design Flow Summary

Analog Flow

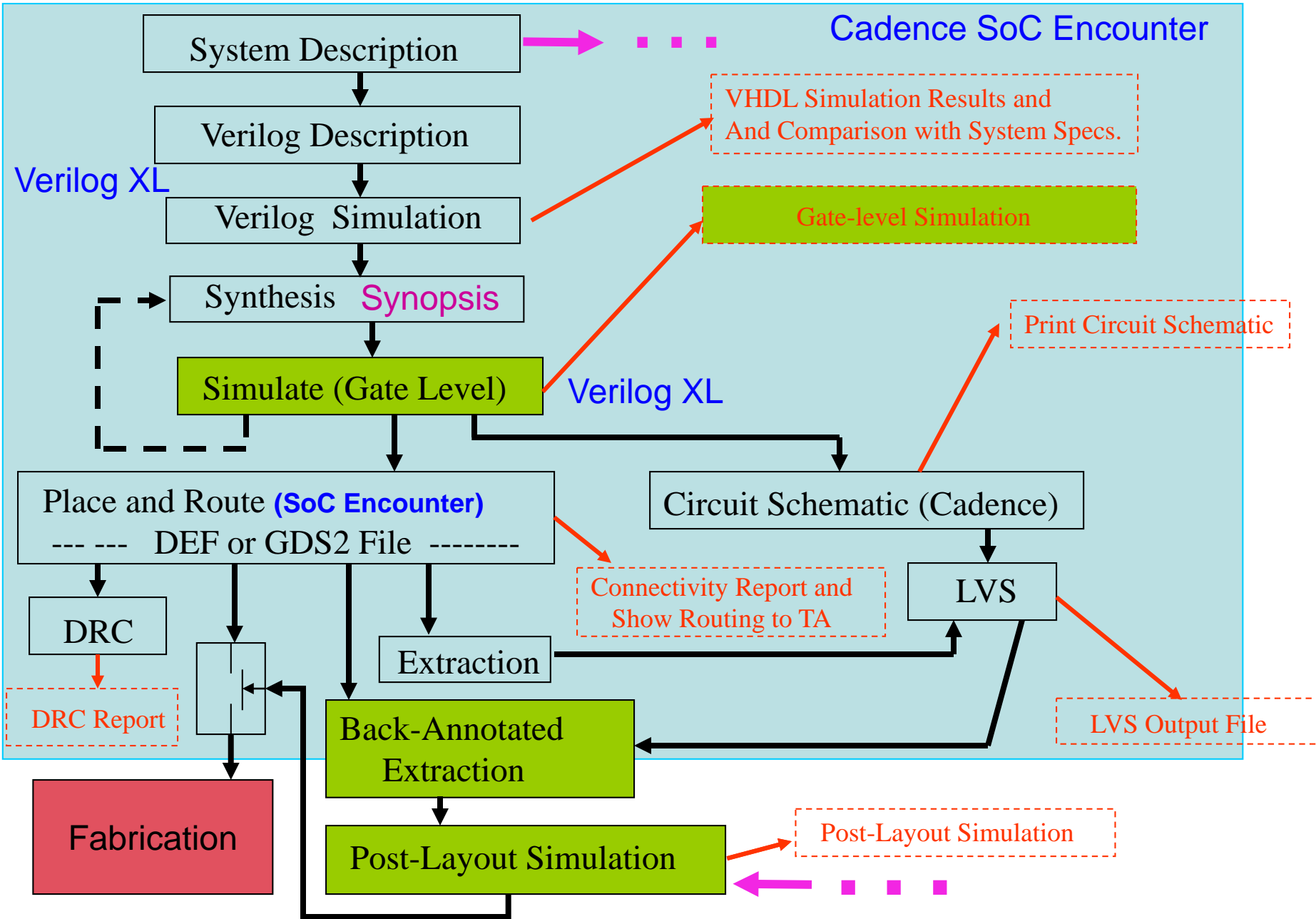


VLSI Design Flow Summary



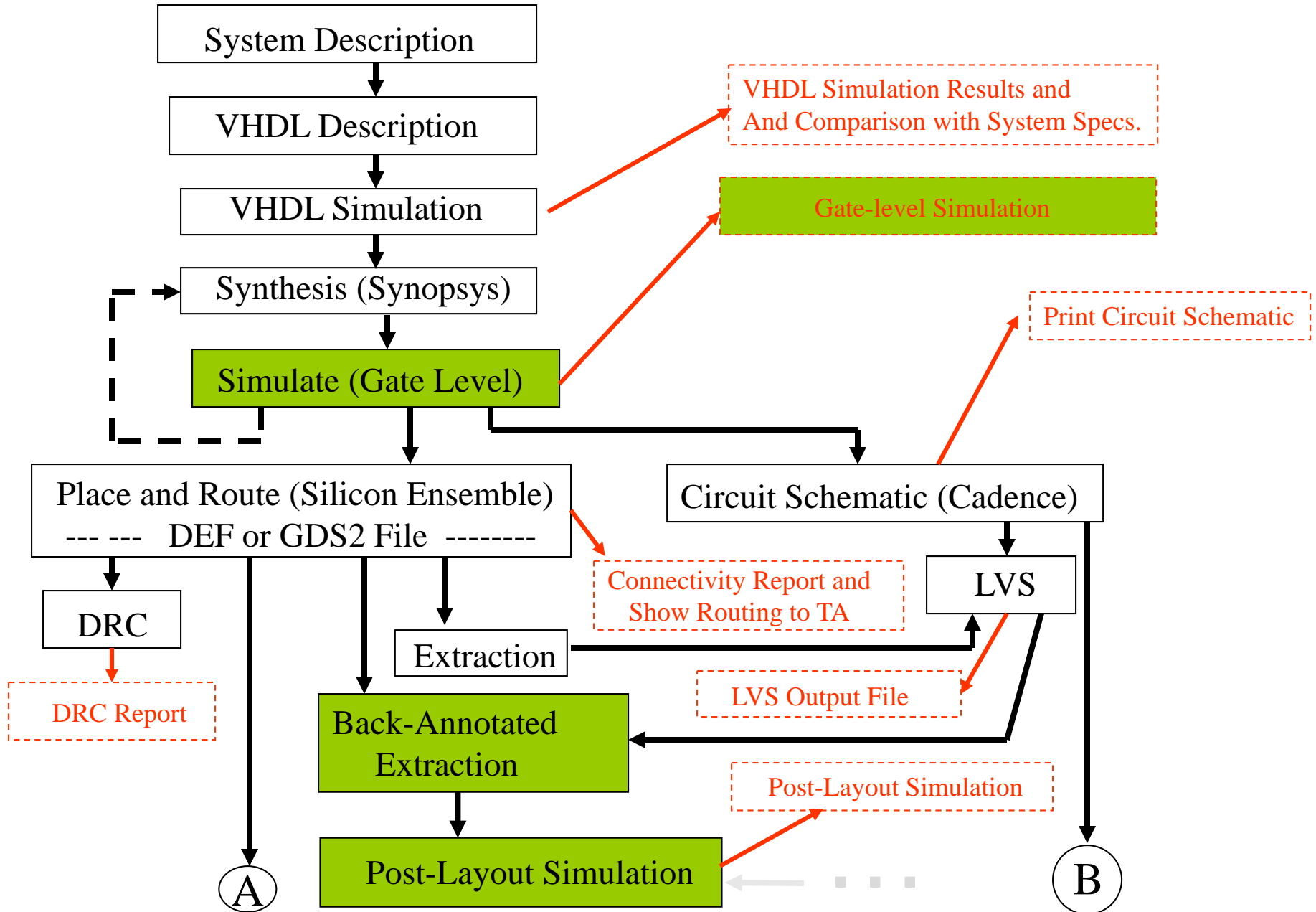
VLSI Design Flow Summary

Digital Flow



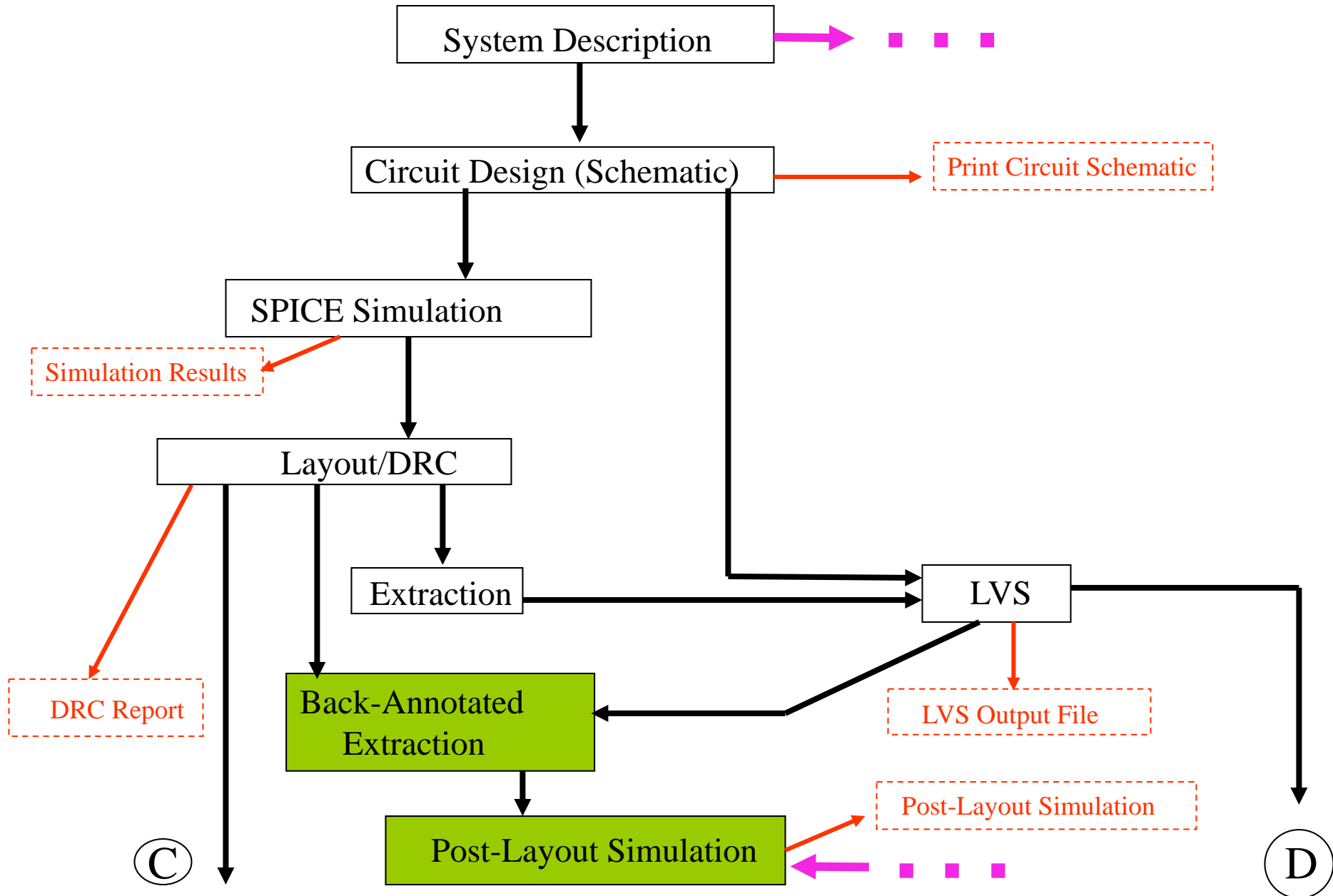
VLSI Design Flow Summary

Mixed Signal Flow (Digital Part)



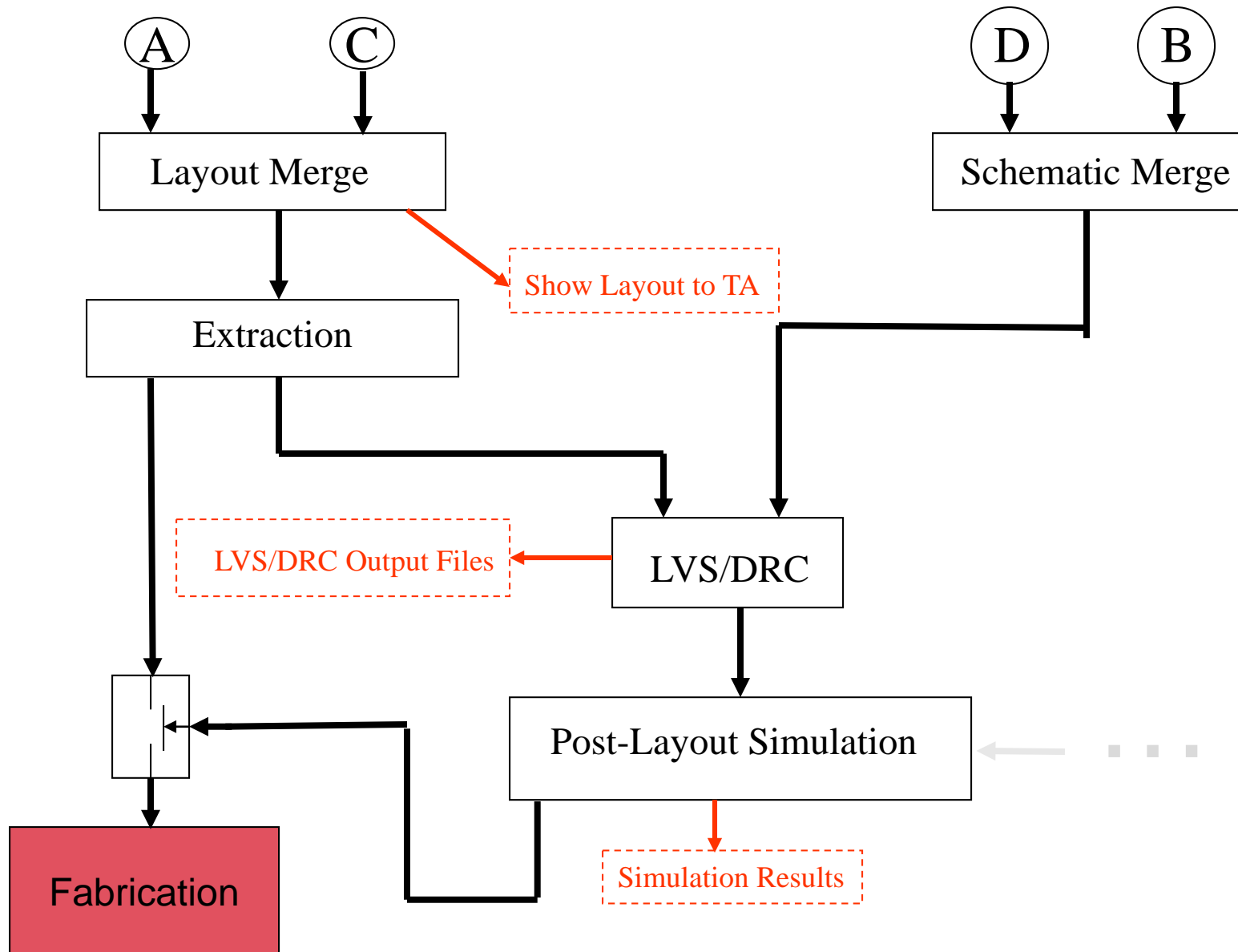
VLSI Design Flow Summary

Mixed-Signal Flow (Analog Part)



VLSI Design Flow Summary

Mixed-Signal Flow (Analog-Digital Merger)



Comments

- The Analog Design Flow is often used for small digital blocks or when particular structure or logic styles are used in digital systems
- Variants of these flows are widely used and often personalized by a given company or for specific classes of circuits

End of Lecture 2