EE 330
Lecture 3

- Basic Concepts
  - Feature Sizes
  - Manufacturing Costs
  - Yield
- Key Historical Developments

IEEE-USA

SALARY & BENEFITS SURVEY

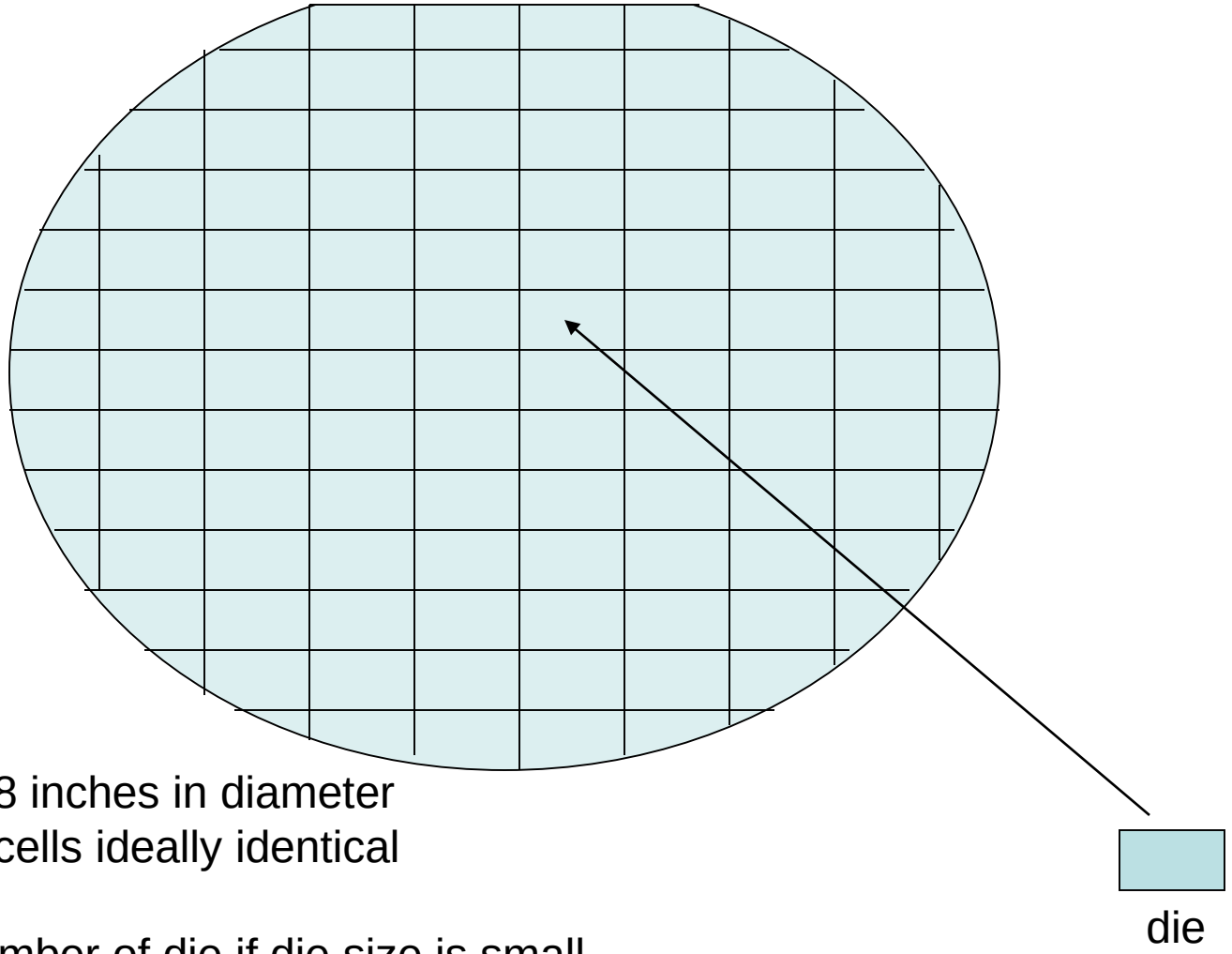
2016 EDITION

2015 Primary Income by Primary Area of Technical Competence

	Number of Cases	Lowest Decile	Lower Quartile	Median	Upper Quartile	Highest Decile
TOTAL	7,391	$79,200	$103,000	$135,000	$173,000	$223,000
CIRCUITS AND DEVICES	1,127	$85,000	$110,000	$144,700	$182,878	$240,000
Circuits and Systems	416	$79,750	$100,991	$130,000	$165,000	$210,000
Components, Packaging and Manufacturing Technology	94	$103,200	$120,188	$153,850	$190,700	$258,800
Electronic Devices	239	$80,000	$105,034	$141,458	$186,372	$235,240
Lasers and Electro-Optics	79	$83,800	$112,915	$150,000	$184,000	$222,800
Solid-State Circuits	277	$105,030	$134,000	$165,000	$204,700	$265,168
Other	25	$72,380	$107,000	$136,000	$208,000	$332,175
COMMUNICATIONS TECHNOLOGY	581	$87,000	$114,000	$152,500	$196,000	$250,000
Broadcast Technology	46	$64,500	$97,500	$141,500	$198,000	$326,250
Communications	419	$87,400	$114,945	$153,000	$193,289	$246,370
Consumer Electronics	42	$94,150	$105,750	$156,500	$188,750	$256,500
Vehicular Technology	21	-	-	-	-	-
Other	61	$93,441	$122,400	$163,000	$208,099	$270,000
COMPUTERS	1,545	$80,000	$103,500	$138,941	$180,000	$233,614
Hardware	246	$90,000	$110,000	$143,702	$182,625	$254,261
Non-Internet Software Development	591	$80,000	$101,000	$136,000	$176,928	$226,000
Non-Internet Systems Analysis/Integration	179	$83,800	$102,583	$130,000	$173,726	$221,850
Non-Internet Software Applications including Database Admin.	90	$65,260	$100,415	$132,500	$165,825	$222,500
Internet/Web Development/Applications	220	$73,538	$106,875	$139,800	$181,438	$256,757
Other	224	$80,300	$108,172	$147,500	$181,875	$234,290
ELECTROMAGNETICS AND RADIATION	420	$84,900	$110,000	$137,912	$169,606	$204,655
Antennas and Propagation	103	$78,720	$116,100	$140,000	$172,000	$197,367
Electromagnetic Compatibility	65	$76,800	$96,000	$123,079	$155,000	$180,600
Magnetics	26	$90,500	$109,472	$145,000	$180,902	$241,000
Microwave Theory and Techniques	114	$79,200	$105,314	$133,526	$168,344	$200,650
Nuclear and Plasma Sciences	70	$87,660	$113,725	$139,000	$159,825	$192,660
Other	50	$102,000	$121,500	$150,000	$184,600	$220,000
ENERGY AND POWER ENGINEERING	1,597	$75,000	$94,450	$121,000	$152,000	$192,000

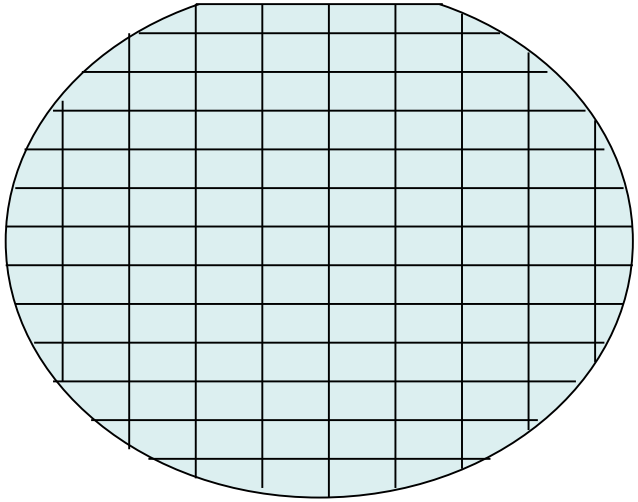
ENGINEERING AND HUMAN ENVIRONMENT	144	$73,868	$99,900	$132,667	$167,625	$220,728
Education	24	-	-	-	-	-
Engineering Management	87	$97,200	$116,000	$145,000	$180,000	$230,480
Professional Communication	0	-	-	-	-	-
Reliability	15	-	-	-	-	-
Social Implications of Technology	8	-	-	-	-	-
Other	14	-	-	-	-	-
INDUSTRIAL APPLICATIONS	340	$79,900	$100,000	$126,600	$160,000	$210,000
Dielectrics and Electrical Insulation	16	-	-	-	-	-
Industry Applications	149	$87,660	$108,400	$130,000	$166,220	$211,460
Instrumentation and Measurement	91	$68,000	$92,124	$118,000	$144,985	$180,000
Power Electronics	59	$81,835	$102,500	$130,000	$160,500	$208,400
Other	25	$99,780	$120,000	$143,000	$210,000	$235,145
SIGNALS AND APPLICATIONS	532	$94,100	$114,263	$142,792	$180,000	$223,000
Aerospace and Electronic Systems	162	$90,300	$113,010	$147,500	$179,250	$216,895
Geoscience and Remote Sensing	47	$96,600	$113,379	$153,200	$198,000	$220,531
Oceanic Engineering	13	-	-	-	-	-
Signal Processing	243	$95,046	$116,237	$141,200	$179,000	$230,649
Ultrasonics, Ferroelectrics and Frequency Control	36	$96,750	$117,197	$136,000	$167,657	$239,500
Other	30	$75,020	$106,250	$130,926	$178,277	$205,100
SYSTEMS AND CONTROL	689	$74,800	$98,000	$130,000	$165,000	$209,582
Control Systems	270	$72,000	$94,625	$122,183	$155,110	$197,000
Engineering in Medicine and Biology	124	$88,002	$113,847	$143,500	$182,000	$229,600
Industrial Electronics	62	$71,550	$89,250	$118,517	$154,113	$194,188
Information Theory	10	-	-	-	-	-
Robotics and Automation	129	$73,106	$92,842	$123,000	$154,609	$188,520
Systems, Man and Cybernetics	64	$75,000	$120,000	$146,946	$184,250	$222,800
Other	47	$97,600	$117,250	$154,000	$182,000	$224,960
OTHER	346	$79,000	$103,000	$131,424	$178,000	$235,000

Wafer



- 6 inches to 18 inches in diameter
- All complete cells ideally identical
- flat edge
- very large number of die if die size is small

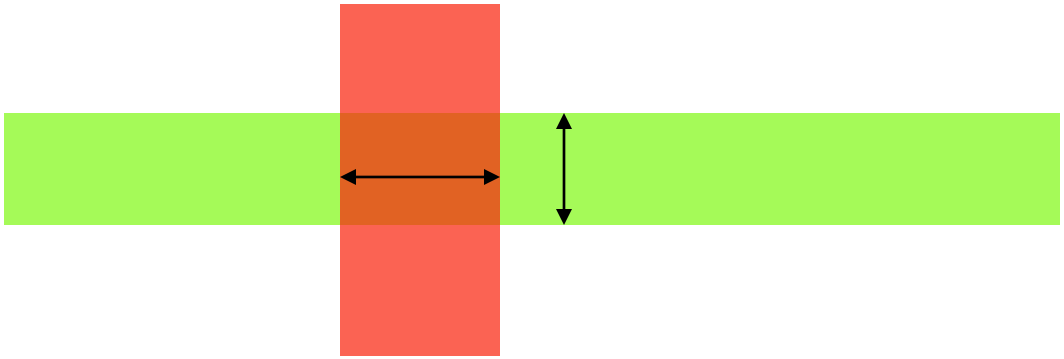
Why are wafers round?



- Ingot spins as crystal is being made (dominant reason)
- Edge loss would be larger with rectangular wafers
- Heat is more uniformly distributed during processing
- Size of furnace is smaller for round wafers
- Wafers are spun during application of photoresist and even coatings is critical
- Optics for projection are better near center of image

Feature Size

Feature size is the minimum lateral feature size that can be **reliably** manufactured

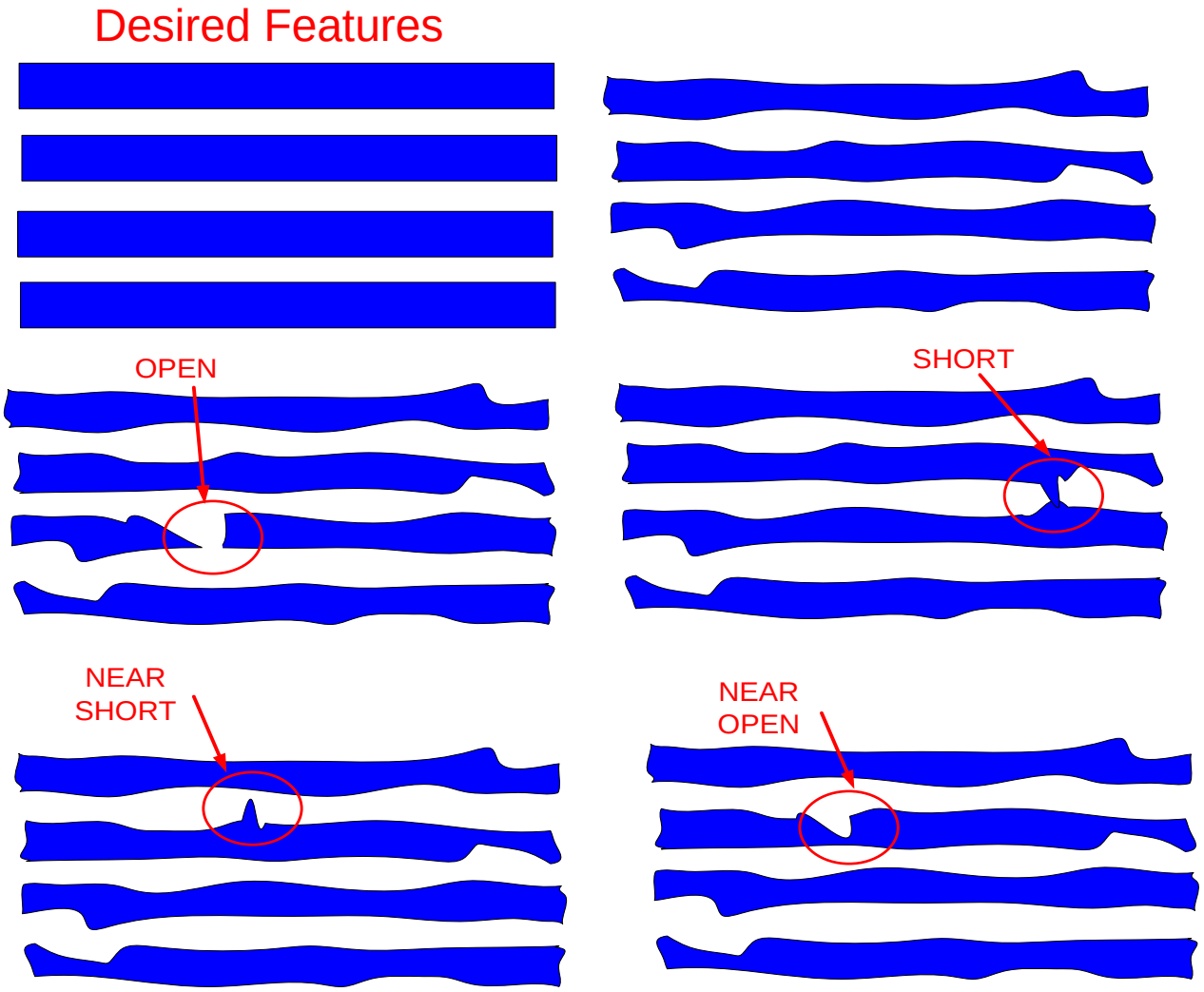


Often given as either feature size or pitch

Minimum feature size often identical for different features

Extremely challenging to decrease minimum feature size in a new process

Reliability Problems



Actual features show some variability (dramatically exaggerated here !!!!)

What is meant by “reliably”

Yield is acceptable if circuit performs as designed even when a very large number of these features are made

If P is the probability that a feature is good

n is the number of uncorrelated features on an IC

Y is the yield

$$Y = P^n$$

$$P = e^{\frac{\log_e Y}{n}}$$

Example: How reliable must a feature be?

n=5E3

Y=0.9

$$P = e^{\frac{\log_e Y}{n}} = e^{\frac{\log_e 0.9}{5E3}}$$ **=0.999979**

But is n=5000 large enough ?

More realistically n=5E9 (or even 5E10)

Consider n=5E9

$$P = e^{\frac{\log_e Y}{n}} = e^{\frac{\log_e 0.9}{5E9}}$$ **=0.999999999979**

20 parts in a trillion or size of a piece of sheetrock relative to area of Iowa

Extremely high reliability must be achieved in all processing steps to obtain acceptable yields in state of the art processes

Feature Size

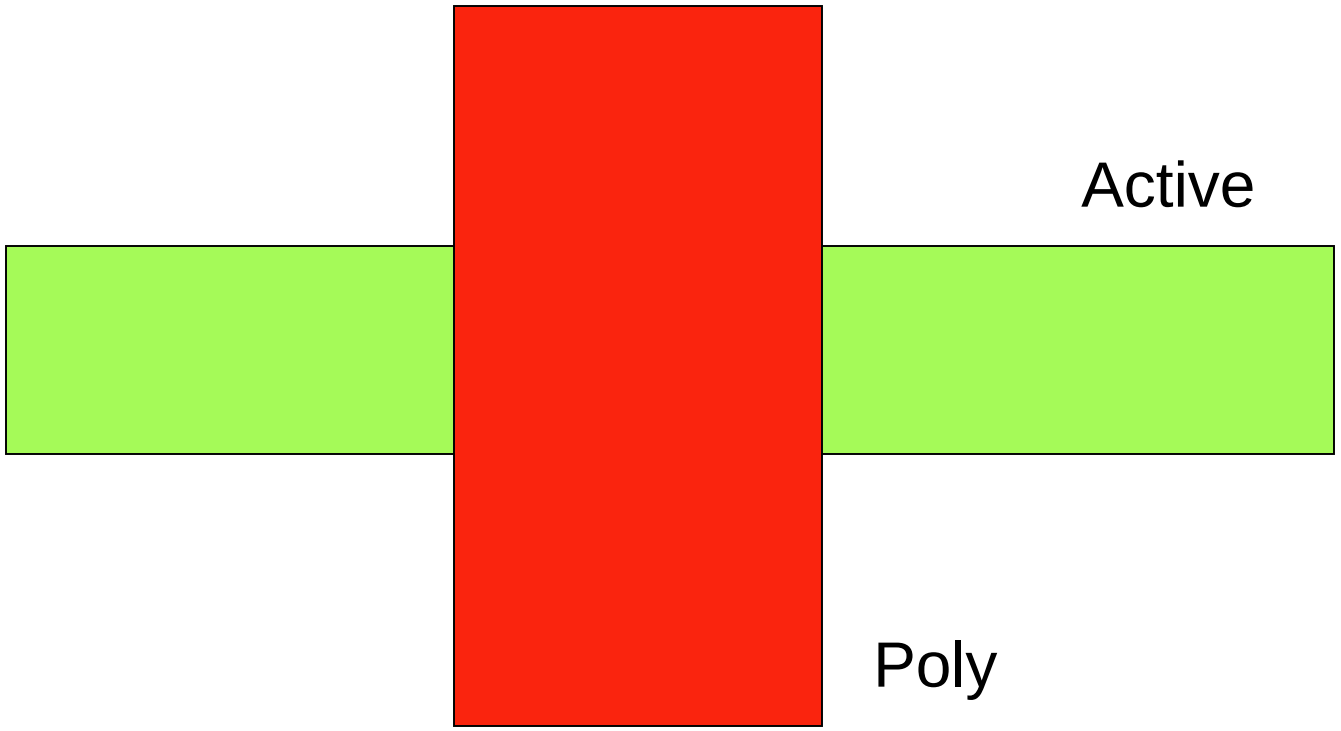
- Typically minimum length of a transistor
- Often minimum width or spacing of a metal interconnect (wire)
- Point of “bragging” by foundries
  - Drawn length and actual length differ
- Often specified in terms of pitch
  - Pitch is sum of feature size and spacing to same feature
  - Pitch approximately equal to twice minimum feature size

Feature Size Evolution

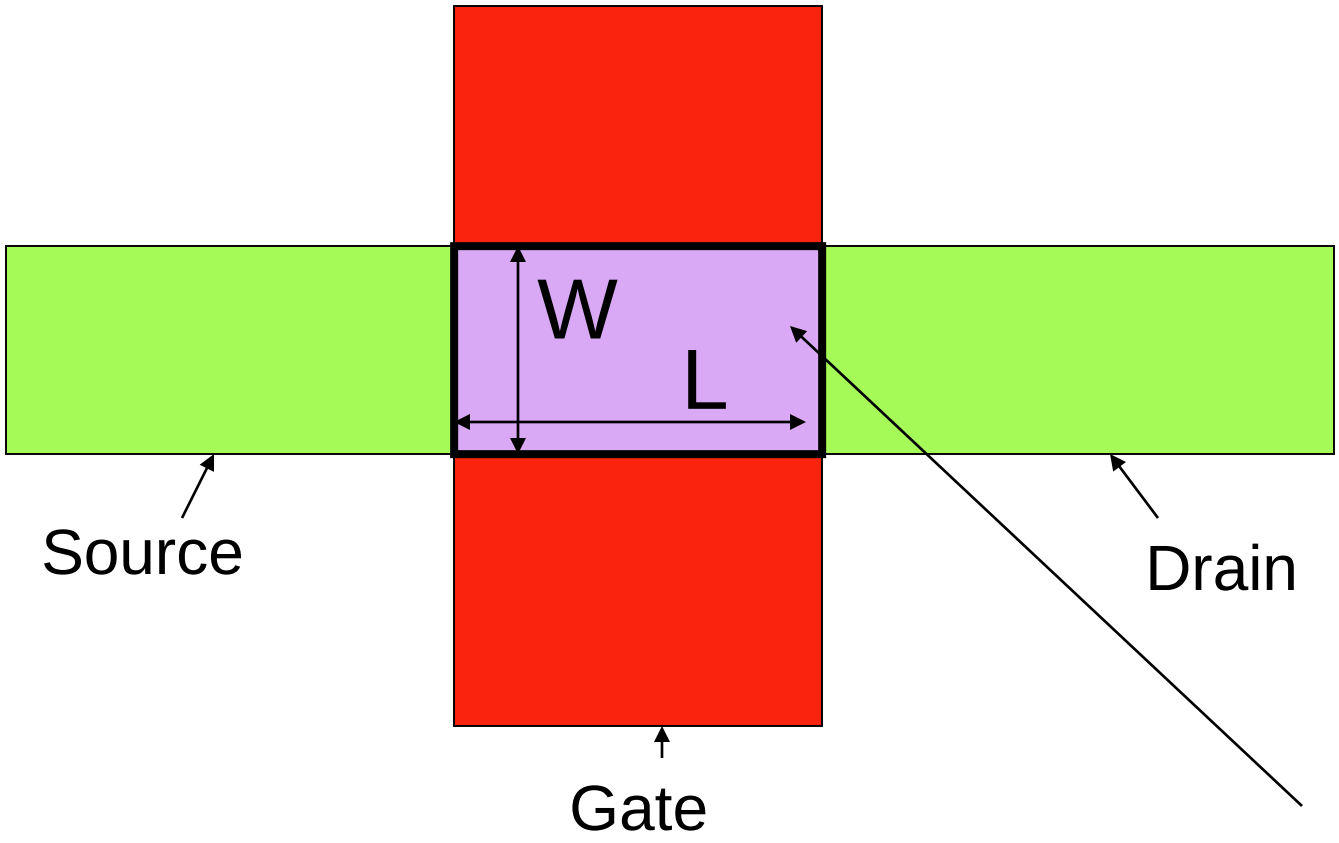
Mid 70's	25μ
2005	90nm
2010	20nm
2020	7nm

$$1\mu = 10^{3}\,nm = 10^{-6}\,m = 10^{4}\ \mathring{\mathrm{A}}$$

MOS Transistor

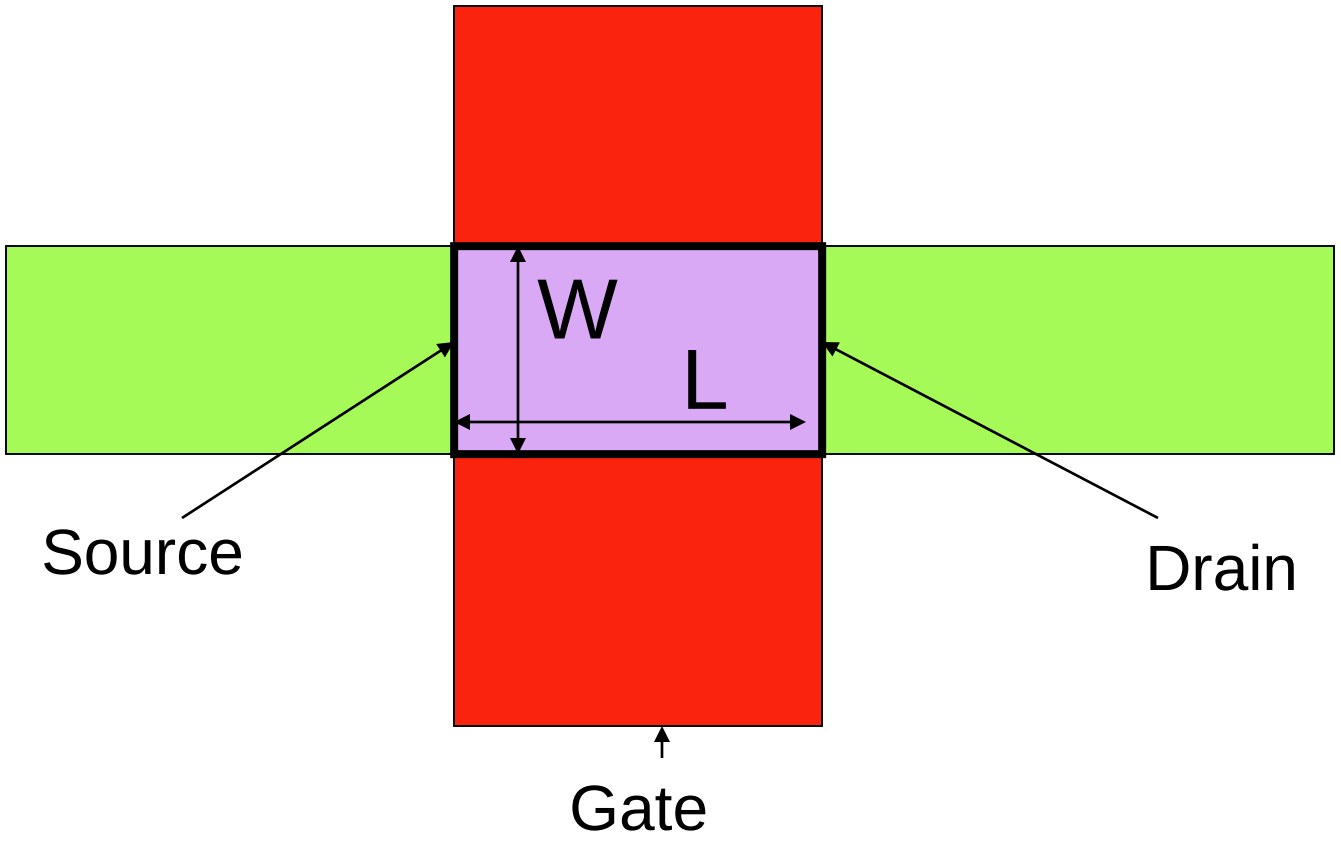


MOS Transistor



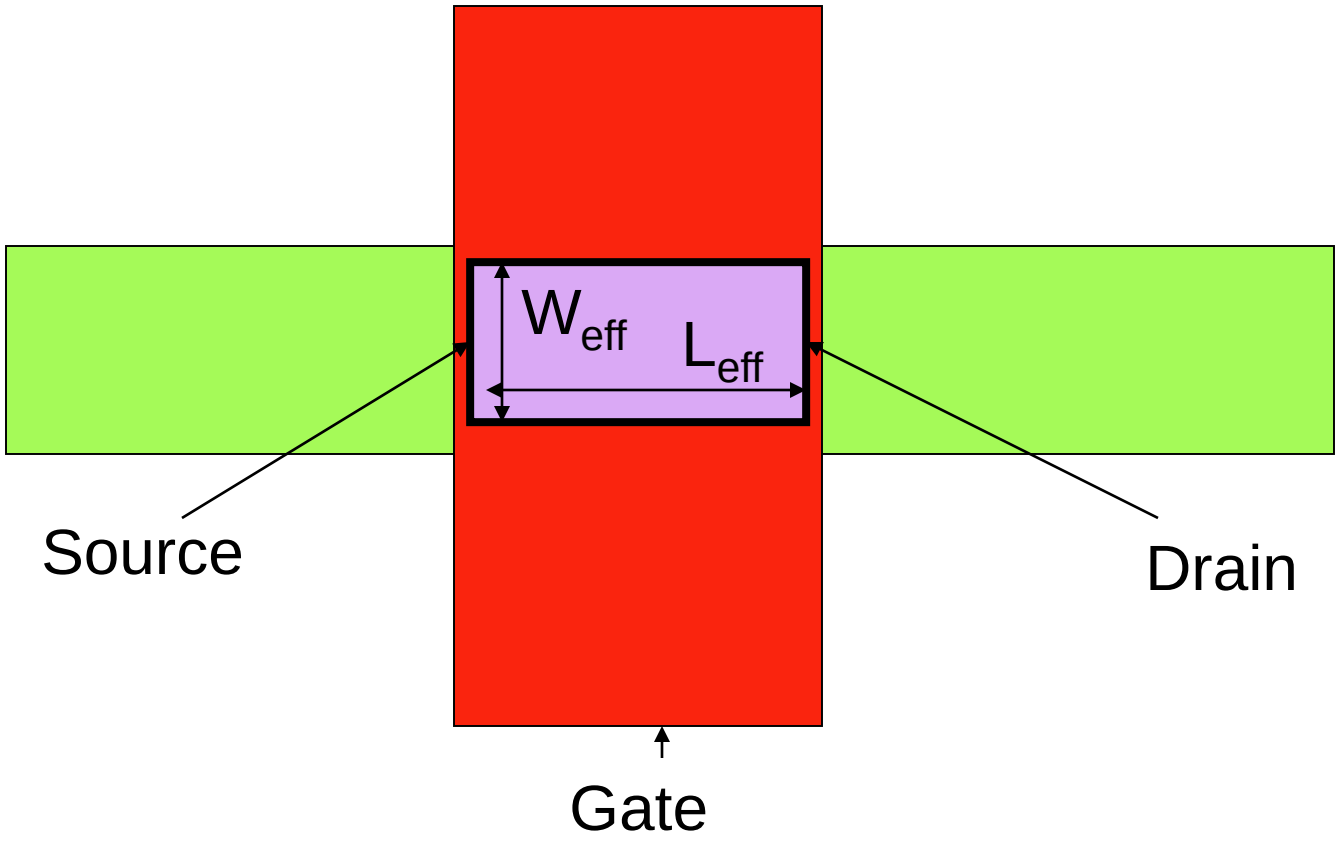
Drawn Length and Width Shown

MOS Transistor



Actual Drain and Source at Edges of Channel

MOS Transistor



Effective Width and Length Generally Smaller than Drawn Width and Length

Device and Die Costs

Characterize the high-volume incremental costs of manufacturing integrated circuits

Example: Assume manufacturing cost of an 8” wafer in a 0.25µ process is $800

Determine the number of minimum-sized transistors that can be fabricated on this wafer and the cost per transistor. Neglect spacing and interconnect.

Solution:

$$n_{trans} \cong \frac{A_{wafer}}{A_{trans}} = \frac{\pi(4in)^2}{(0.25\mu)^2} = 5.2E11$$

(520 Billion!)

(Trillion, Tera …10^{12})

$$C_{trans} = \frac{C_{wafer}}{n_{trans}} = \frac{\$800}{5.2E11} = \$15.4E-9$$

Note: the device count may be decreased by a factor of 10 or more if Interconnect and spacing is included but even with this decrease, the cost per transistor is still very low!

Device and Die Costs

$$C_{per\ unit\ area} \cong \$2.5/cm^2$$

Example: If the die area of the 741 op amp is 1.8mm^2, determine the cost of the silicon needed to fabricate this op amp

$$C_{741} = \$2.5/cm^2 \bullet \left(1.8mm^2\right) \cong \$.05$$

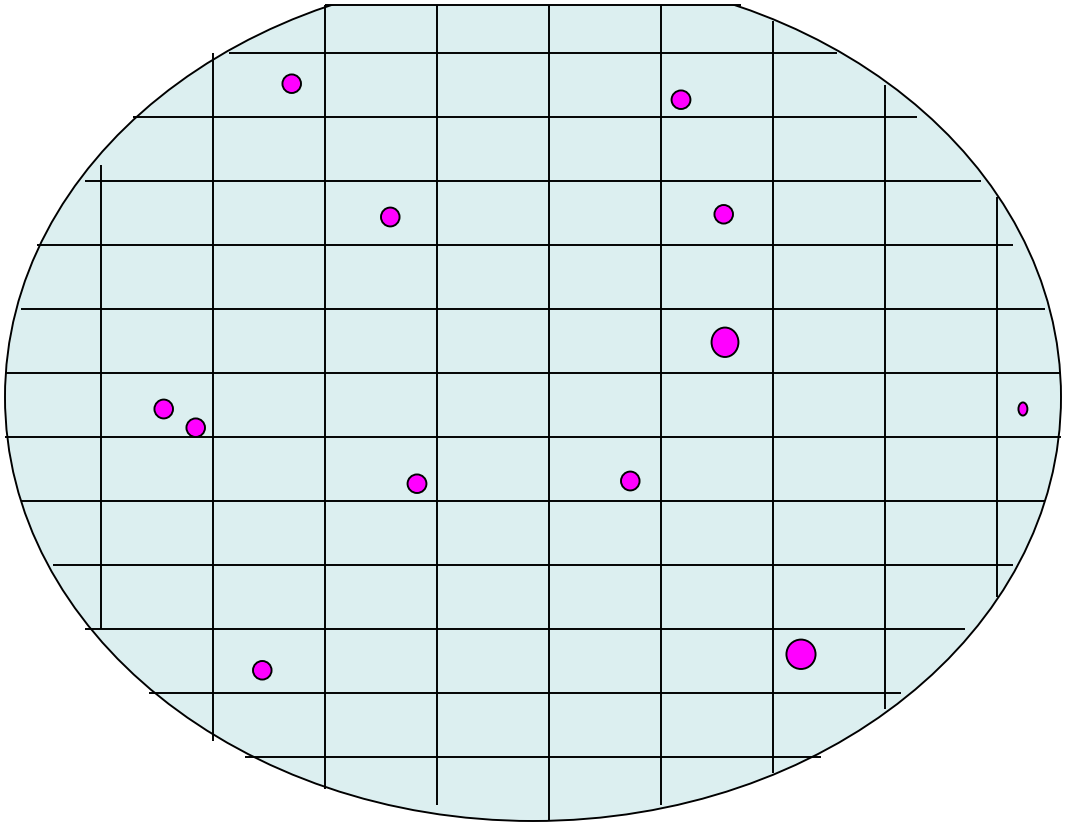
Actual integrated op amp will be dramatically less if bonding pads are not needed

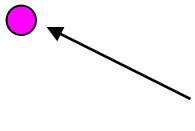
Size of Atoms and Molecules in Semiconductor Processes

Silicon:	Average Atom Spacing	$2.7\,\mathring{A}$
	Lattice Constant	$5.4\,\mathring{A}$
S_iO_2	Average Atom Spacing	$3.5\,\mathring{A}$
	Breakdown Voltage	$5 \text{ to } 10 MV/cm = 5 \text{ to } 10 mV/\mathring{A}$
Air		$20 KV/cm$

Physical size of atoms and molecules place fundamental limit on conventional scaling approaches

Defects in a Wafer





- Dust particles and other undesirable processes cause defects
- Defects in manufacturing cause yield loss

Yield Issues and Models

- Defects in processing cause yield loss
- The probability of a defect causing a circuit failure increases with die area
- The circuit failures associated with these defects are termed **Hard Faults**
- This is the major factor limiting the size of die in integrated circuits
- Wafer scale integration has been a “gleam in the eye” of designers for 3 decades but the defect problem continues to limit the viability of such approaches
- Several different models have been proposed to model the hard faults

Yield Issues and Models

- Parametric variations in a process can also cause circuit failure or cause circuits to not meet desired performance specifications (this is of particular concern in analog and mixed-signal circuits)
- The circuits failures associated with these parametric variations are termed **Soft Faults**
- Increases in area, judicious layout and routing, and clever circuit design techniques can reduce the effects of soft faults

Hard Fault Model

$$Y_H = e^{-\alpha Ad}$$

Y_H is the probability that the die does not have a hard fault
A is the die area
d is the defect density (typically $1cm^{-2} < d < 2cm^{-2}$)

Industry often closely guards the value of d for their process

Other models, which may be better, have the same general functional form

Soft Fault Model

Soft fault models often dependent upon design and application

Often the standard deviation of a parameter is dependent upon the reciprocal of the square root of the parameter sensitive area

$$\sigma = \frac{\rho}{\sqrt{A_k}}$$

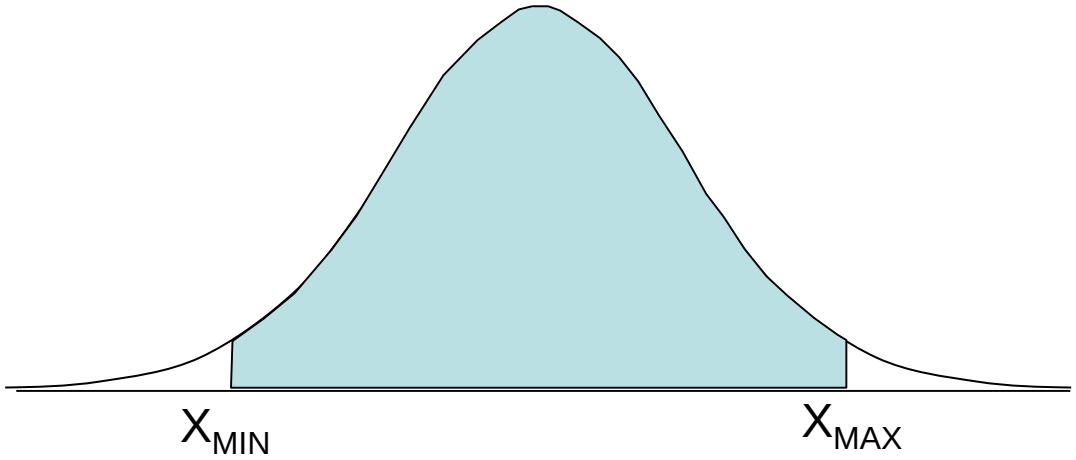
ρ is a constant dependent upon the architecture and the process

A_k is the area of the parameter sensitive area

Soft Fault Model

$$P_{SOFT} = \int_{X_{MIN}}^{X_{MAX}} f(x)dx$$

P_{SOFT} is the soft fault yield
f(x) is the probability density function of the parameter of interest
X_{MIN} and X_{MAX} define the acceptable range of the parameter of interest



Some circuits may have several parameters that must meet performance requirements

Soft Fault Model

If there are k parameters that must meet parametric performance requirements and if the random variables characterizing these parameters are uncorrelated, then the soft yield is given by

$$Y_S = \prod_{j=1}^{k} P_{SOFT_j}$$

Overall Yield

If both hard and soft faults affect the yield of a circuit, the overall yield is given by the expression

$$Y = Y_H Y_S$$

Cost Per Good Die

The manufacturing costs per good die is given by

$$C_{Good} = \frac{C_{FabDie}}{Y}$$

where C_{FabDie} is the manufacturing costs of a fab die and Y is the yield

There are other costs that must ultimately be included such as testing costs, engineering costs, etc.

Example: Assume a die has no soft fault vulnerability, a die area of $1cm^2$ and a process has a defect density of $1.5cm^{-2}$

a) Determine the hard yield
b) Determine the manufacturing cost per good die if 8” wafers are used and if the cost of the wafers is $1200

Solution

a) $$Y_H = e^{-Ad}$$

$$Y = e^{-1\text{cm}^2 \bullet 1.5\text{cm}^{-2}} = 0.22$$

b) $$C_{Good} = \frac{C_{FabDie}}{Y}$$

$$C_{FabDie} = \frac{C_{Wafer}}{A_{Wafer}} A_{Die}$$

$$C_{FabDie} = \frac{\$1200}{\pi(4\text{in})^2} 1\text{cm}^2 = \$3.82$$

$$C_{Good} = \frac{\$3.82}{0.22} = \$17.37$$

Do you like statistics ?

Statistics are Real!

Statistics govern what really happens throughout much of the engineering field!

Statistics are your Friend !!!!

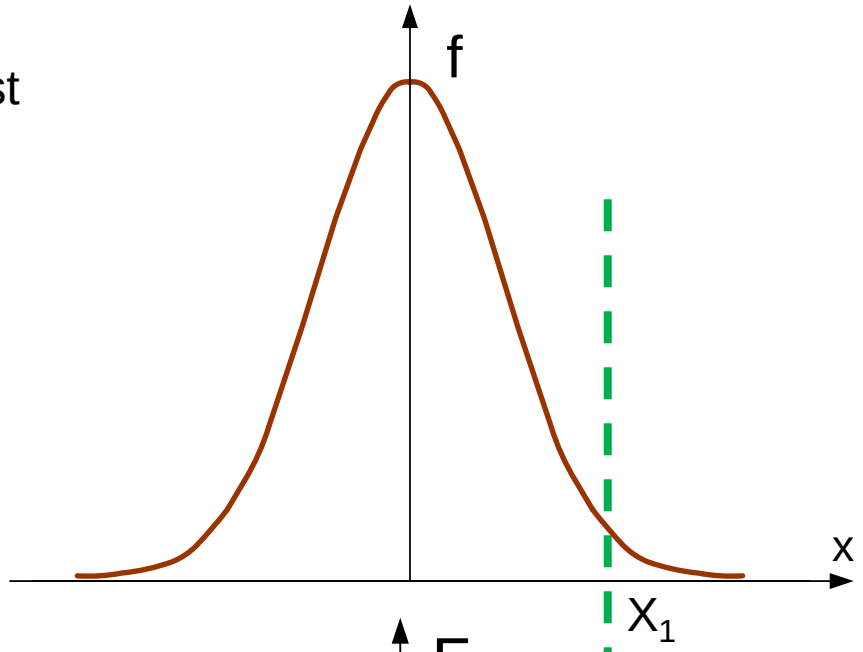
You might as well know what will happen since statistics characterize what WILL happen in the presence of variability in many processes !

Statistics Review

Assume x is a random variable of interest

f(x) = Probability Density Function for x

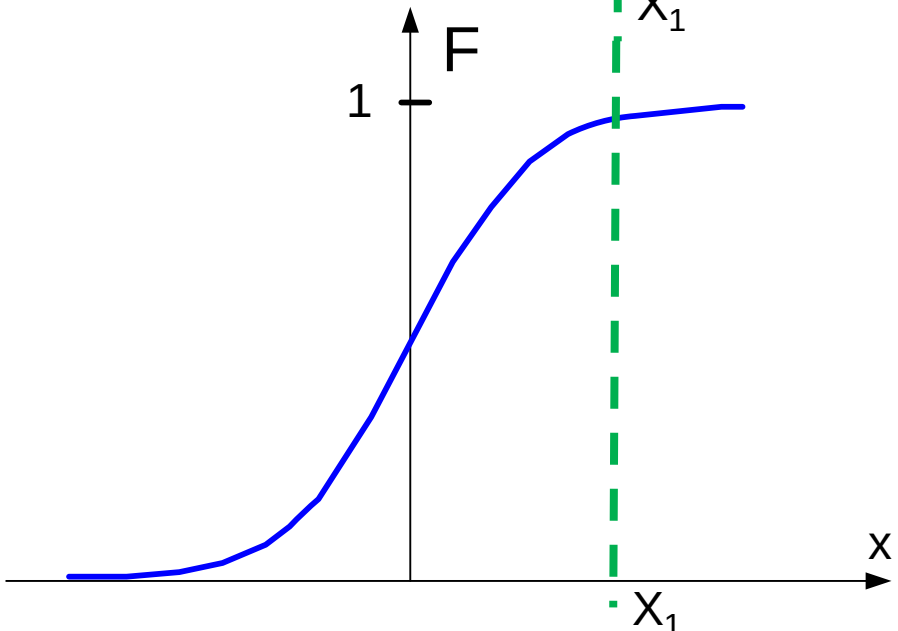
$$\int_{x=-\infty}^{\infty} f(x)\,dx = 1$$



F(x) = Cumulative Density Function for x

$$F(X_1) = \int_{x=-\infty}^{X_1} f(x)\,dx$$

$$0 \le F(x) \le 1 \qquad \frac{\partial F(x)}{\partial x} \ge 0$$



Statistics Review

f(x) = Probability Density Function for x

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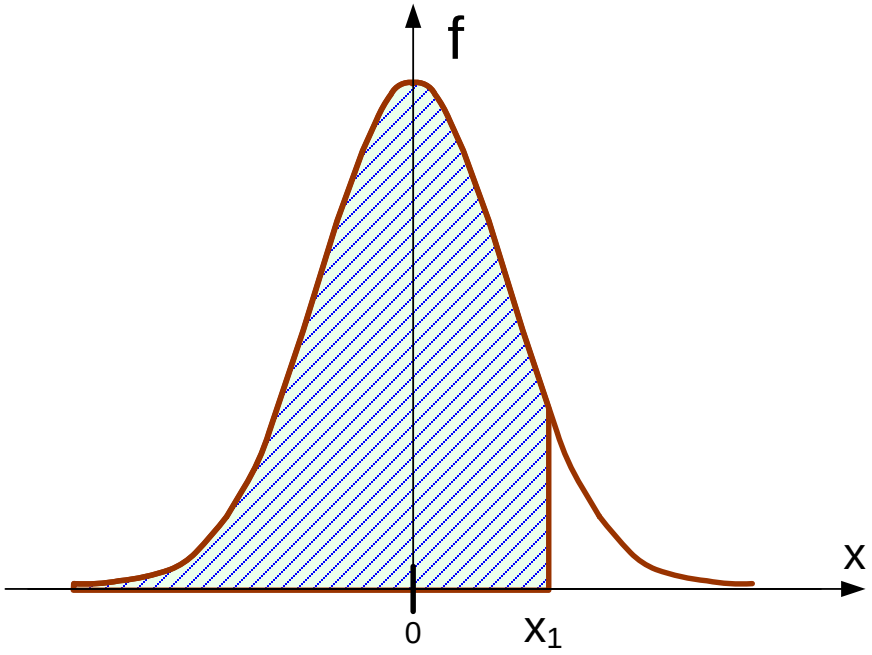
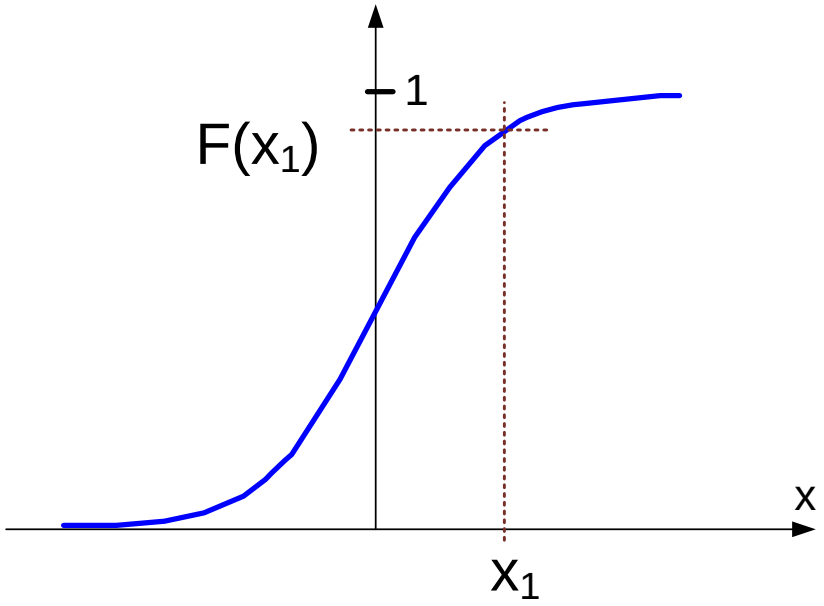




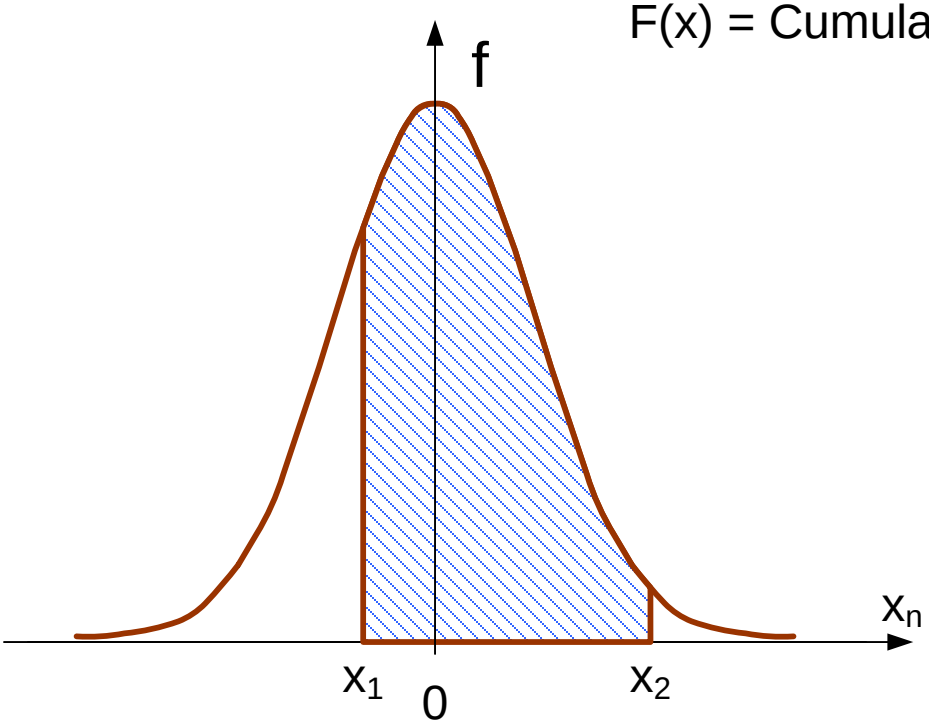
$$P\{x \le x_1\} = \int_{x=-\infty}^{x_1} f(x)\,dx$$

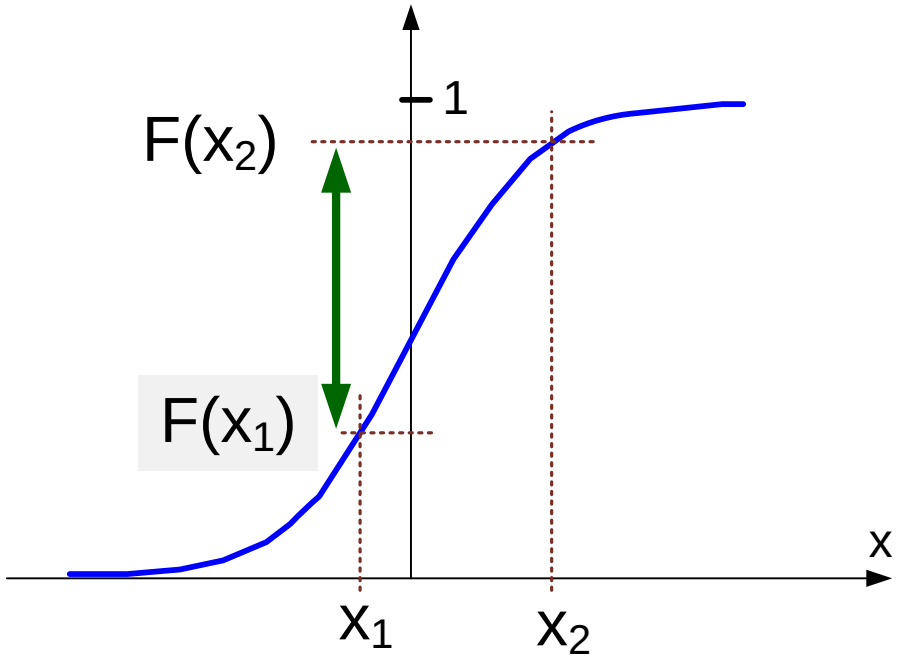
$$P\{x \le X_1\} = F(X_1)$$

Statistics Review

f(x) = Probability Density Function for x

F(x) = Cumulative Density Function for x

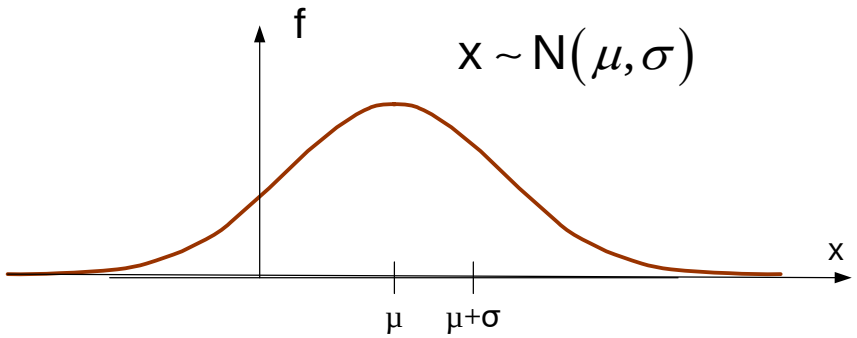


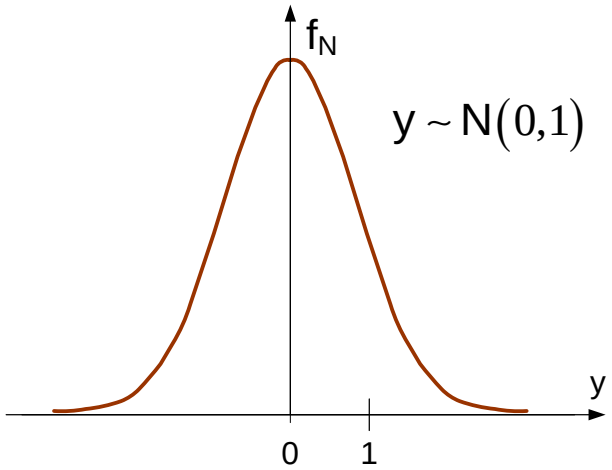


$$P\{X_1 \le x \le X_2\} = \int_{x_1}^{x_2} f(x)\,dx$$

$$P\{X_1 \le x \le X_2\} = F(X_2) - F(X_1)$$

Statistics Review





$$\int_{x=-\infty}^{\infty} f(x)\,dx = 1$$

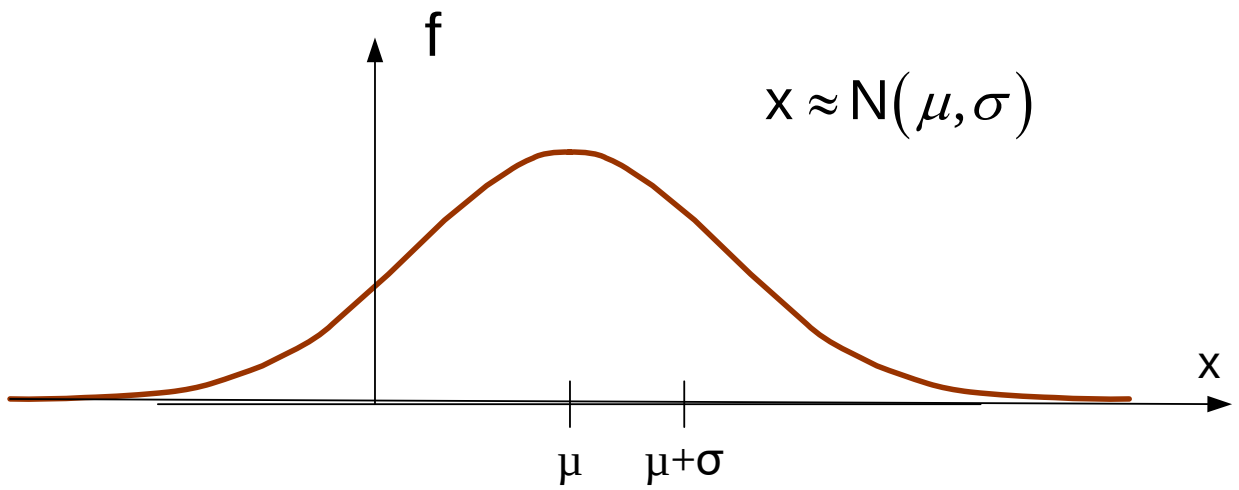
$$y = \frac{x-\mu}{\sigma}$$

$$\int_{y=-\infty}^{\infty} f_N(y)\,dy = 1$$

Theorem 1: If the random variable x in normally distributed with mean μ and standard deviation σ, then $y = \frac{x-\mu}{\sigma}$ is also a random variable that is normally distributed with mean 0 and standard deviation of 1.

(Normal Distribution and Gaussian Distribution are the same)

Statistics Review



The random part of many parameters of microelectronic circuits is often assumed to be Normally distributed and experimental observations confirm that this assumption provides close agreement between theoretical and experimental results

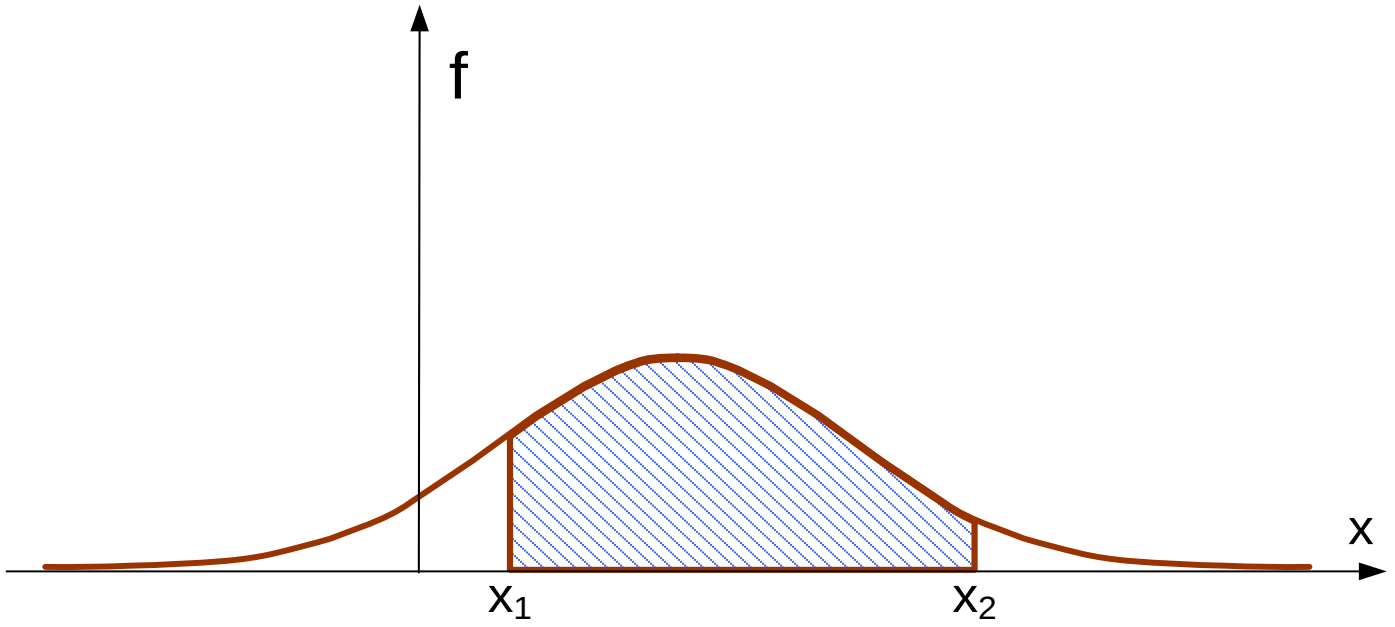
The mapping $y = \frac{x - \mu}{\sigma}$ is often used to simplify the statistical characterization of the random parameters in microelectronic circuits

Background Information

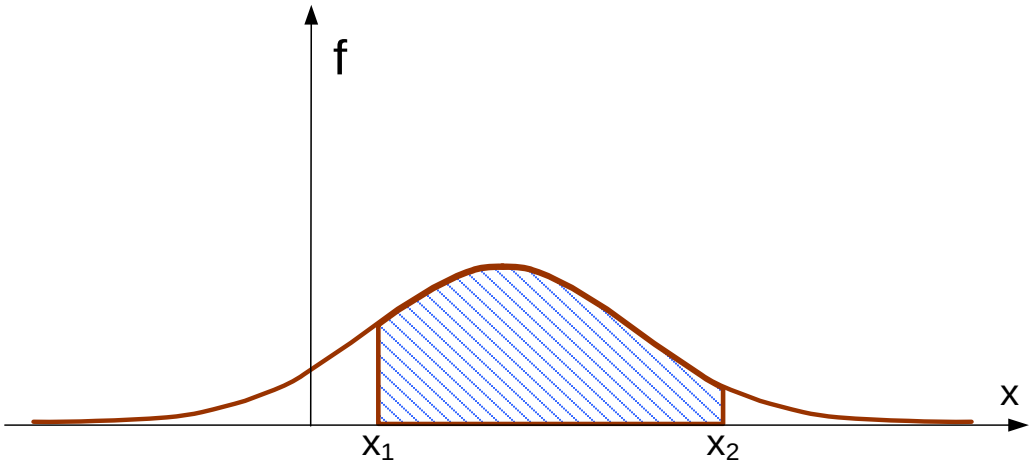
Theorem 2: If x is a Normal (Gaussian) random variable with mean μ and standard deviation σ, then the probability that x is between x_1 and x_2 is given by

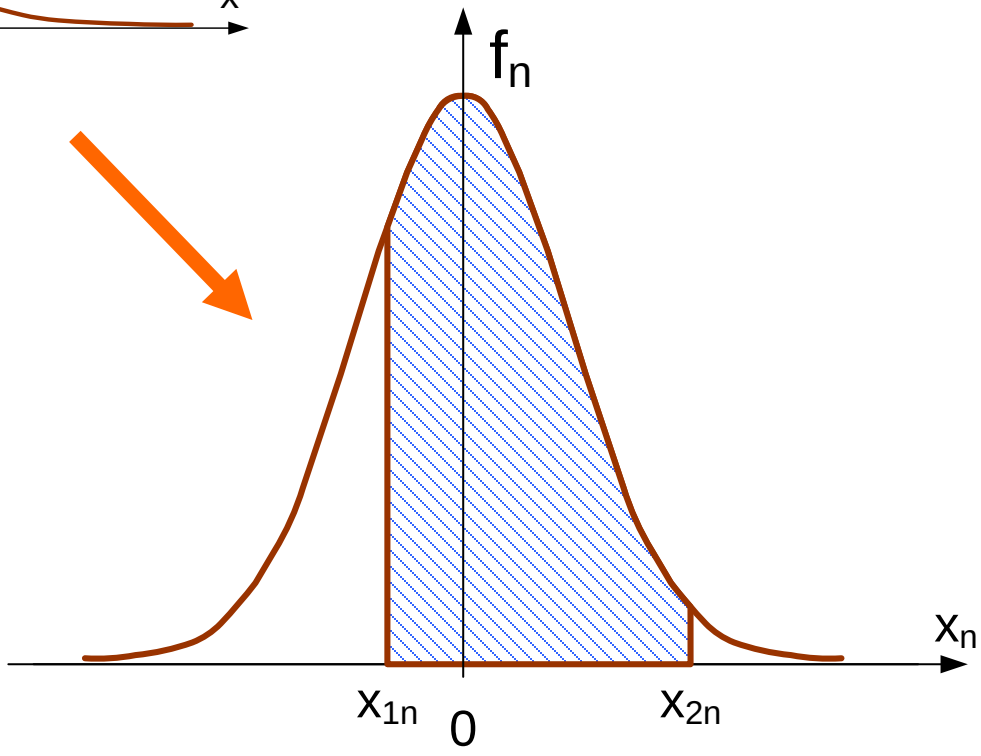
$$p = \int_{x_1}^{x_2} f(x)\,dx = \int_{x_{1n}}^{x_{2n}} f_n(x)\,dx \quad \text{where} \quad x_{1n} = \frac{x_1 - \mu}{\sigma} \quad \text{and} \quad x_{2n} = \frac{x_2 - \mu}{\sigma}$$

and where $f_n(x)$ is N(0,1)



Background Information



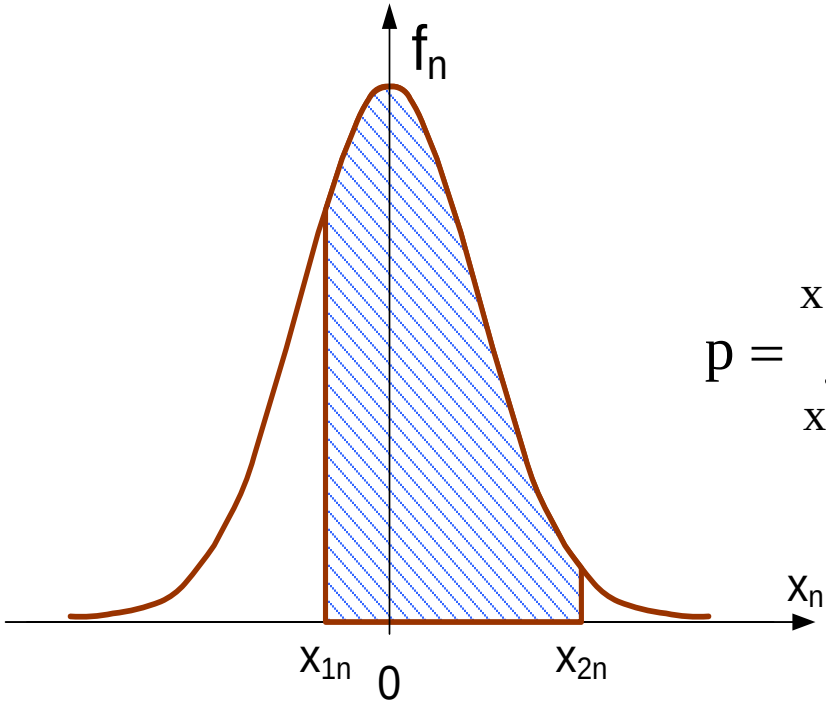


Background Information

Observation: The probability that the N(0,1) random variable x_n satisfies the relationship $x_{1n}<x_n<x_{2n}$ is also given by

$$p = F_n\left(x_{2n}\right) - F_n\left(x_{1n}\right)$$

where $F_n(x)$ is the CDF of x_n.



$$p = \int_{x_{1n}}^{x_{2n}} f_n\left(x\right)dx$$

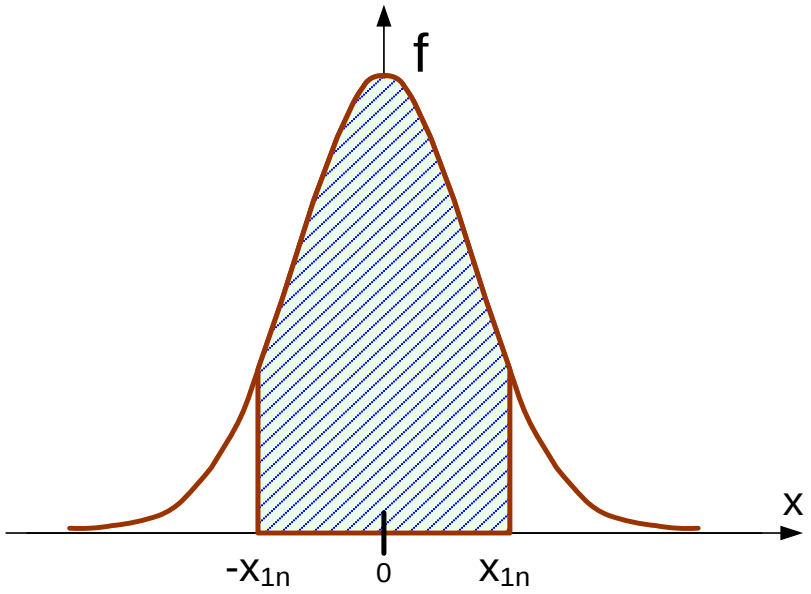
Since the N(0,1) distribution is symmetric around 0, p can also be expressed as

$$p = F_n\left(x_{2n}\right) - \left(1 - F_n\left(-x_{1n}\right)\right)$$

Background Information

Observation: In many electronic circuits, the random variables of interest are 0 mean Gaussian and the probabilities of interest are characterized by a region defined by the magnitude of the random variable. In these cases,

$$p = \int_{-x_{1n}}^{x_{1n}} f_n(x)\,dx = F_n(x_{1n}) - F_n(-x_{1n}) = 2F_n(x_{1n}) - 1$$



Background Information

Tables of the CDF of the N(0,1) random variable are readily available. It is also available in Matlab, Excel, and a host of other sources.

Probability Content from -oo to Z

Z	0.00	0.01	0.02	0.03	0.04	0.05	0.06	0.07	0.08	0.09
0.0	0.5000	0.5040	0.5080	0.5120	0.5160	0.5199	0.5239	0.5279	0.5319	0.5359
0.1	0.5398	0.5438	0.5478	0.5517	0.5557	0.5596	0.5636	0.5675	0.5714	0.5753
0.2	0.5793	0.5832	0.5871	0.5910	0.5948	0.5987	0.6026	0.6064	0.6103	0.6141
0.3	0.6179	0.6217	0.6255	0.6293	0.6331	0.6368	0.6406	0.6443	0.6480	0.6517
0.4	0.6554	0.6591	0.6628	0.6664	0.6700	0.6736	0.6772	0.6808	0.6844	0.6879
0.5	0.6915	0.6950	0.6985	0.7019	0.7054	0.7088	0.7123	0.7157	0.7190	0.7224
0.6	0.7257	0.7291	0.7324	0.7357	0.7389	0.7422	0.7454	0.7486	0.7517	0.7549
0.7	0.7580	0.7611	0.7642	0.7673	0.7704	0.7734	0.7764	0.7794	0.7823	0.7852
0.8	0.7881	0.7910	0.7939	0.7967	0.7995	0.8023	0.8051	0.8078	0.8106	0.8133
0.9	0.8159	0.8186	0.8212	0.8238	0.8264	0.8289	0.8315	0.8340	0.8365	0.8389
1.0	0.8413	0.8438	0.8461	0.8485	0.8508	0.8531	0.8554	0.8577	0.8599	0.8621
1.1	0.8643	0.8665	0.8686	0.8708	0.8729	0.8749	0.8770	0.8790	0.8810	0.8830
1.2	0.8849	0.8869	0.8888	0.8907	0.8925	0.8944	0.8962	0.8980	0.8997	0.9015
1.3	0.9032	0.9049	0.9066	0.9082	0.9099	0.9115	0.9131	0.9147	0.9162	0.9177
1.4	0.9192	0.9207	0.9222	0.9236	0.9251	0.9265	0.9279	0.9292	0.9306	0.9319
1.5	0.9332	0.9345	0.9357	0.9370	0.9382	0.9394	0.9406	0.9418	0.9429	0.9441
1.6	0.9452	0.9463	0.9474	0.9484	0.9495	0.9505	0.9515	0.9525	0.9535	0.9545
1.7	0.9554	0.9564	0.9573	0.9582	0.9591	0.9599	0.9608	0.9616	0.9625	0.9633
1.8	0.9641	0.9649	0.9656	0.9664	0.9671	0.9678	0.9686	0.9693	0.9699	0.9706
1.9	0.9713	0.9719	0.9726	0.9732	0.9738	0.9744	0.9750	0.9756	0.9761	0.9767
2.0	0.9772	0.9778	0.9783	0.9788	0.9793	0.9798	0.9803	0.9808	0.9812	0.9817
2.1	0.9821	0.9826	0.9830	0.9834	0.9838	0.9842	0.9846	0.9850	0.9854	0.9857
2.2	0.9861	0.9864	0.9868	0.9871	0.9875	0.9878	0.9881	0.9884	0.9887	0.9890
2.3	0.9893	0.9896	0.9898	0.9901	0.9904	0.9906	0.9909	0.9911	0.9913	0.9916
2.4	0.9918	0.9920	0.9922	0.9925	0.9927	0.9929	0.9931	0.9932	0.9934	0.9936
2.5	0.9938	0.9940	0.9941	0.9943	0.9945	0.9946	0.9948	0.9949	0.9951	0.9952
2.6	0.9953	0.9955	0.9956	0.9957	0.9959	0.9960	0.9961	0.9962	0.9963	0.9964
2.7	0.9965	0.9966	0.9967	0.9968	0.9969	0.9970	0.9971	0.9972	0.9973	0.9974
2.8	0.9974	0.9975	0.9976	0.9977	0.9977	0.9978	0.9979	0.9979	0.9980	0.9981
2.9	0.9981	0.9982	0.9982	0.9983	0.9984	0.9984	0.9985	0.9985	0.9986	0.9986
3.0	0.9987	0.9987	0.9987	0.9988	0.9988	0.9989	0.9989	0.9989	0.9990	0.9990

http://www.math.unb.ca/~knight/utility/NormTble.htm

Background Information

Tables of the CDF of the N(0,1) random variable are readily available. It is also available in Matlab, Excel, and a host of other sources.

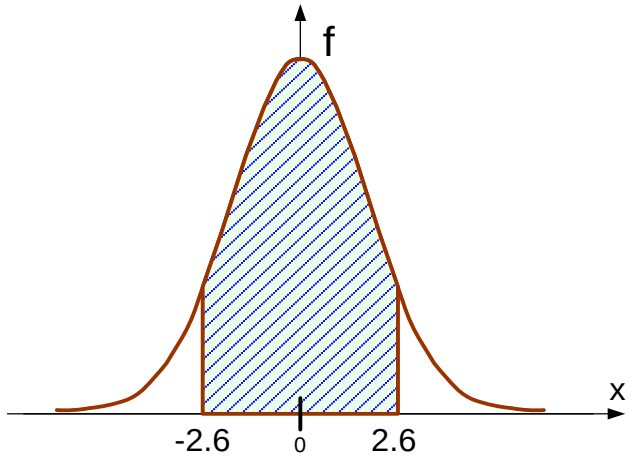
Far Right Tail Probabilities

Z	P{Z to oo}	Z	P{Z to oo}	Z	P{Z to oo}	Z	P{Z to oo}
2.0	0.02275	3.0	0.001350	4.0	0.00003167	5.0	2.867 E-7
2.1	0.01786	3.1	0.0009676	4.1	0.00002066	5.5	1.899 E-8
2.2	0.01390	3.2	0.0006871	4.2	0.00001335	6.0	9.866 E-10
2.3	0.01072	3.3	0.0004834	4.3	0.00000854	6.5	4.016 E-11
2.4	0.00820	3.4	0.0003369	4.4	0.000005413	7.0	1.280 E-12
2.5	0.00621	3.5	0.0002326	4.5	0.000003398	7.5	3.191 E-14
2.6	0.004661	3.6	0.0001591	4.6	0.000002112	8.0	6.221 E-16
2.7	0.003467	3.7	0.0001078	4.7	0.000001300	8.5	9.480 E-18
2.8	0.002555	3.8	0.00007235	4.8	7.933 E-7	9.0	1.129 E-19
2.9	0.001866	3.9	0.00004810	4.9	4.792 E-7	9.5	1.049 E-21

Background Information

Example: Determine the probability that the N(0,1) random variable has magnitude less than 2.6

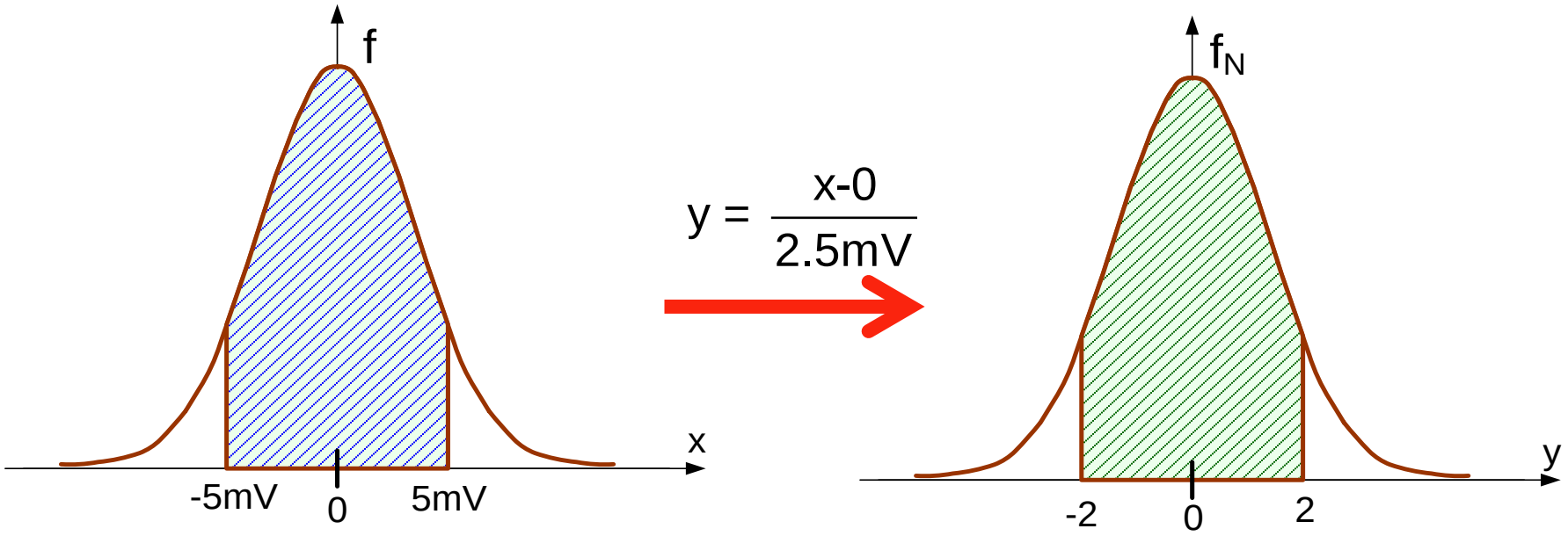
$$p = 2F_n(2.6) - 1$$



From the table of the CDF, $F_n(2.6) = 0.9953$ so $p=.9906$

Background Information

Example: Determine the soft yield of an operational amplifier that has an offset voltage requirement of 5mV if the standard deviation of the offset voltage is 2.5mV and the mean is 0V.



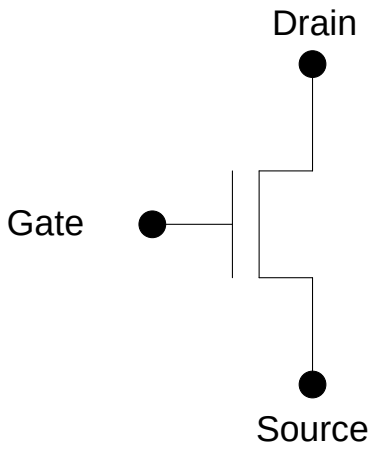
$$p = \int_{-2}^{2} f_N(x)\,dx = F_N(2) - F_N(-2) = 2F_N(2) - 1$$

$$p = 2F_N(2) - 1 = 2*.9772 - 1 = .9544$$

Key Historical Developments

- 1925,1935 Concept of MOS Transistor Proposed (Lilienfield and Heil)
- 1947 BJT Conceived and Experimentally Verified (Bardeen, Bratin and Shockley of Bell Labs)
- 1959 Jack Kilby (TI) and Bob Noyce (Fairchild) invent IC
- 1963 Wanless (Fairchild) Experimentally verifies MOS Gate

The MOS Transistor (Field Effect Transistor)



Initially an idea but little more !

1926 - Field Effect Semiconductor Device Concepts Patented

Julius Lilienfeld files a patent describing a three-electrode amplifying device based on the semiconducting properties of copper sulfide. Attempts to build such a device continue through the 1930s.

Julius E. Lilienfeld, passport photo

Polish-American physicist and inventor Julius E. Lilienfeld filed a patent in 1926, "Method and Apparatus for Controlling Electric Currents," in which he proposed a three-electrode structure using copper-sulfide semiconductor material. Today this device would be called a field-effect transistor. While working at Cambridge University in 1934, German electrical engineer and inventor Oskar Heil filed a patent on controlling current flow in a semiconductor via capacitive coupling at an electrode – essentially a field-effect transistor. Although both patents were granted, no records exist to prove that Heil or Lilienfeld actually constructed functioning devices.

Lilienfeld, J. E. "Method and apparatus for controlling electric currents," *U. S. Patent No. 1,745,175* (Filed October 8, 1926. Issued January 18, 1930).
Lilienfeld, J. E. "Device for controlling electric current," *U. S. Patent No. 1,900,018* (Filed March 28, 1928. Issued March 7, 1933).
Heil, O. "Improvements in or relating to electrical amplifiers and other control arrangements and devices," *British Patent No. 439, 457* (Filed March 5, 1935. Issued December 6, 1935).

http://www.computerhistory.org/semiconductor/timeline/1926-field.html

1935 Oskar Heil improved MOSFET

From Wikipedia:

Oskar Heil (20 March 1908, in Langwieden – 15 May 1994, San Mateo, California) was a German electrical engineer and inventor. He studied physics, chemistry, mathematics, and music at the Georg-August University of Göttingen and was awarded his PhD in 1933, for his work on molecular spectroscopy.

Lilienfeld, J. E. "Method and apparatus for controlling electric currents," *U. S. Patent No. 1,745,175* (Filed October 8, 1926. Issued January 18, 1930).
Lilienfeld, J. E. "Device for controlling electric current," *U. S. Patent No. 1,900,018* (Filed March 28, 1928. Issued March 7, 1933).
Heil, O. "Improvements in or relating to electrical amplifiers and other control arrangements and devices," *British Patent No. 439, 457* (Filed March 5, 1935. Issued December 6, 1935).

https://www.google.com/search?q=Oskar+Heil&biw=1097&bih=568&tbm=isch&imgil=19nt7iXoiQ-X0M%253A%253B8o3VY91vkR5qnM%253Bhttp%25253A%25252F%25252Fwww.avguide.ch%25252Fmagazin%25252Flautsprecher-made-in-ticino-martin-duerrenmatt-perfektioniert-den-heil&source=iu&pf=m&fir=19nt7iXoiQ-X0M%253A%252C8o3VY91vkR5qnM%252C_&usg=__67U7QCOIp8tsrLWv8y_YzTy9c7I%3D#imgrc=dv9-icif2DsZ0M%3A&usg=__67U7QCOIp8tsrLWv8y_YzTy9c7I%3D

http://www.computerhistory.org/semiconductor/timeline/1926-field.html

Patented Jan. 28, 1930 1,745,175

UNITED STATES PATENT OFFICE

JULIUS EDGAR LILIENFELD, OF BROOKLYN, NEW YORK

METHOD AND APPARATUS FOR CONTROLLING ELECTRIC CURRENTS

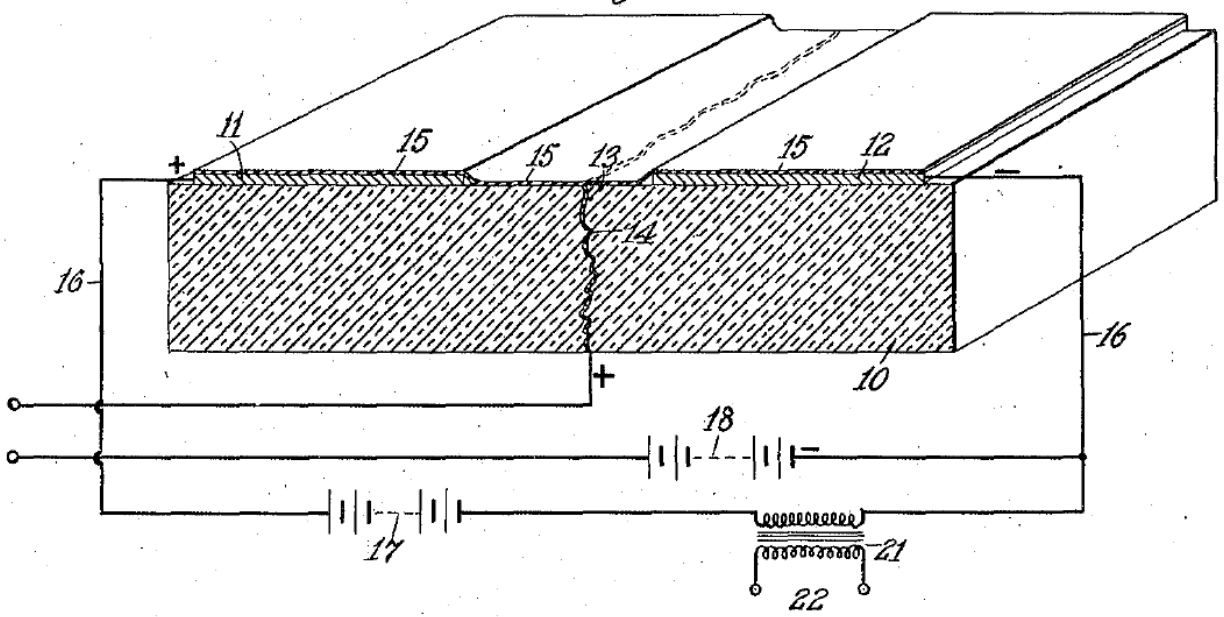
Application filed October 8, 1926, Serial No. 140,363, and in Canada October 22, 1925.

Jan. 28, 1930. J. E. LILIENFELD 1,745,175

METHOD AND APPARATUS FOR CONTROLLING ELECTRIC CURRENTS

Filed Oct. 8, 1926

Fig. 1.



March 7, 1933. J. E. LILIENFELD 1,900,018

DEVICE FOR CONTROLLING ELECTRIC CURRENT

Filed March 28, 1928 3 Sheets-Sheet 1

Fig. 1.

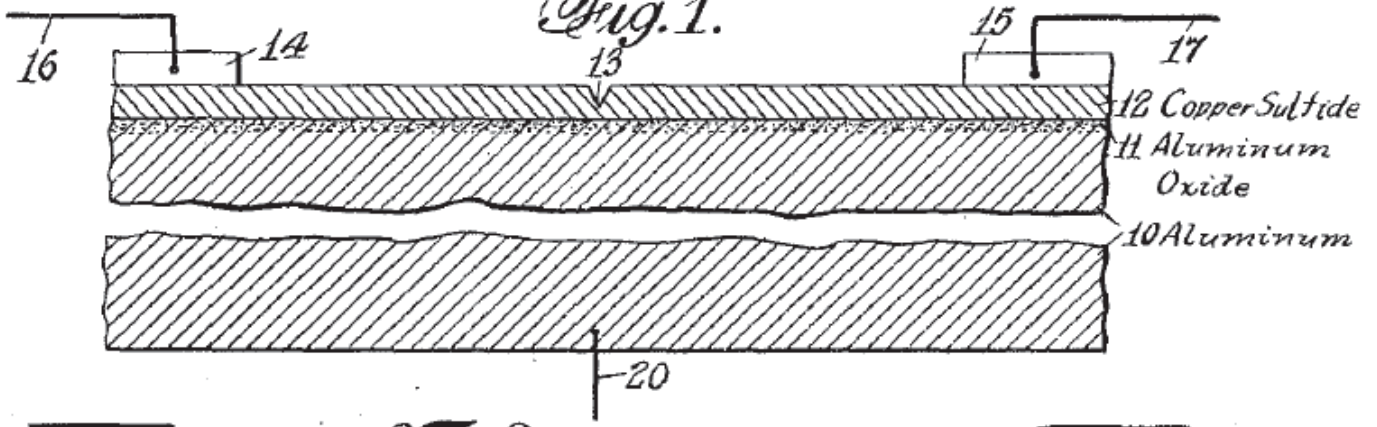
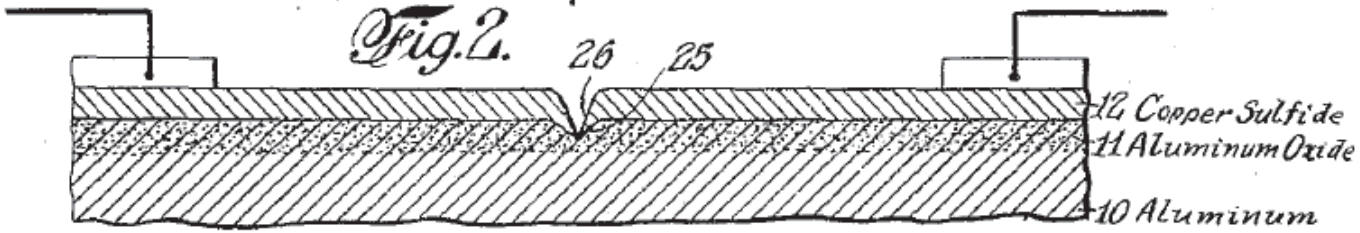


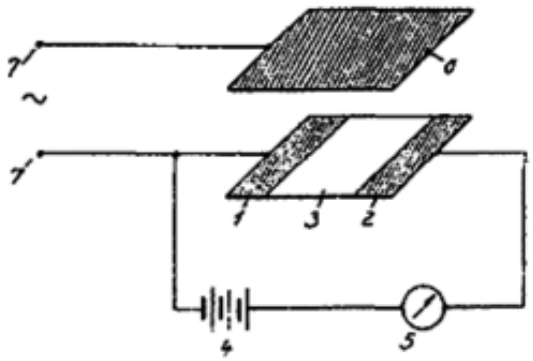
Fig. 2.



Figures from Heil 1935 patent

Insulated gate controls field between other two terminals

Fig. 1



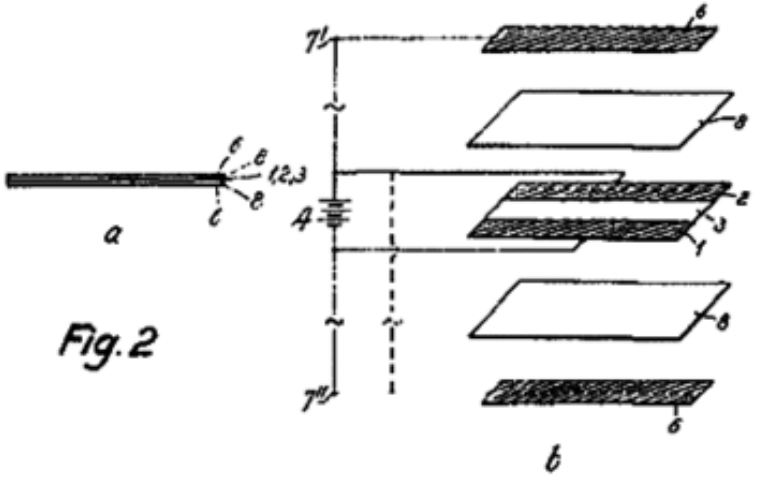


Fig. 2

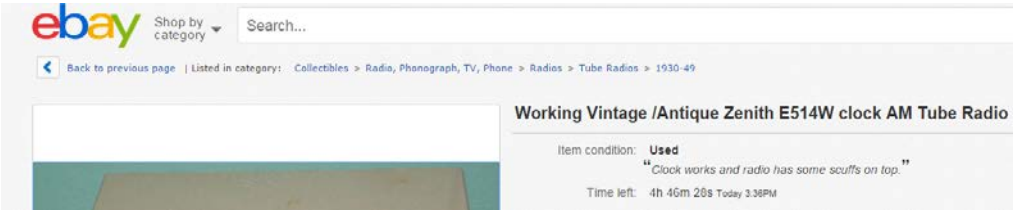
The Vacuum Tube Era

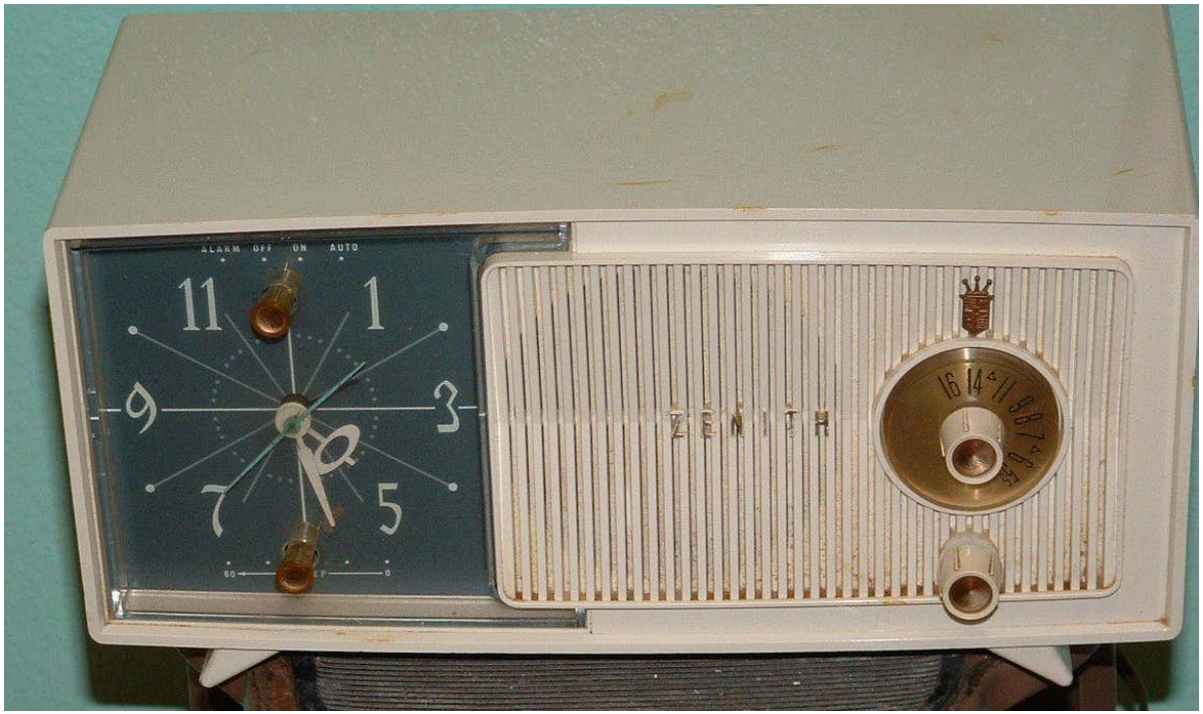
1910 to 1970

The vacuum tube (invented in 1910)

- A major breakthrough in electronics technology
- 6+ decade life span
- Vacuum tube systems not readily affordable by all of society
- Heavy, hot, expensive, large, poor reliability, fragile

The 5-Tube am radio





The 5-Tube am radio

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All American Five

From Wikipedia, the free encyclopedia

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Featured content
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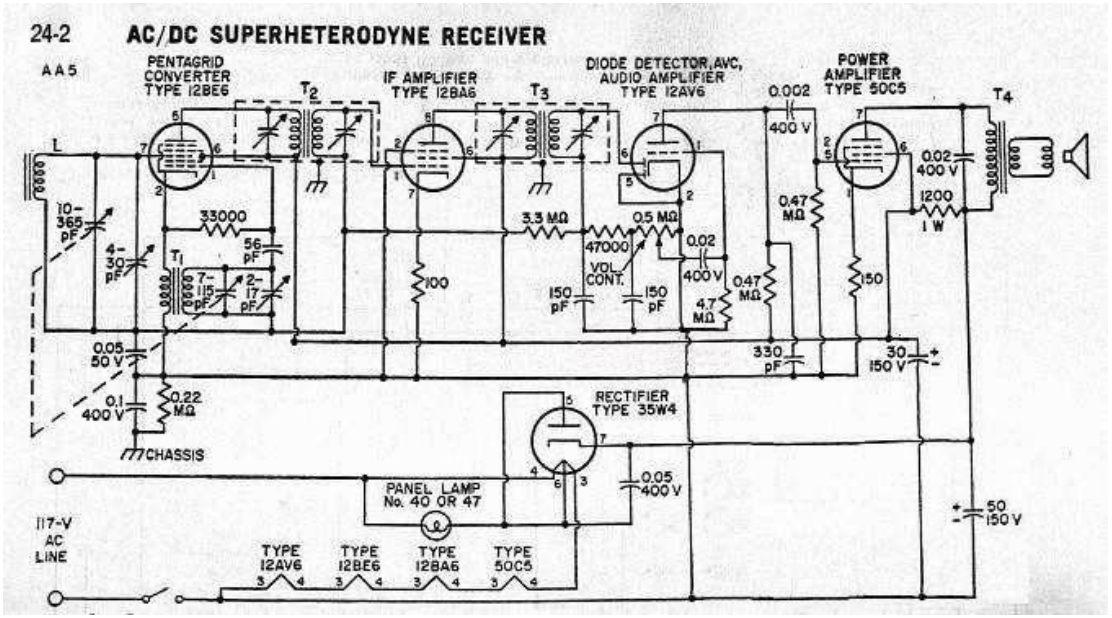
The term **All American Five** is a colloquial name for mass-produced, superheterodyne radio receivers that used five vacuum tubes in their design. These radio sets were designed to receive amplitude modulation (AM) broadcasts in the medium wave band, and were manufactured in the United States from the mid-1930s until the early 1960s[1] By

The 5-Tube am radio

(pictures from WEB pages of images)



Schematics were simple !!

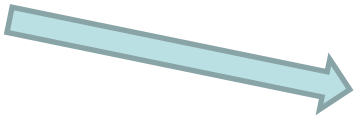
The Vacuum Tube Era

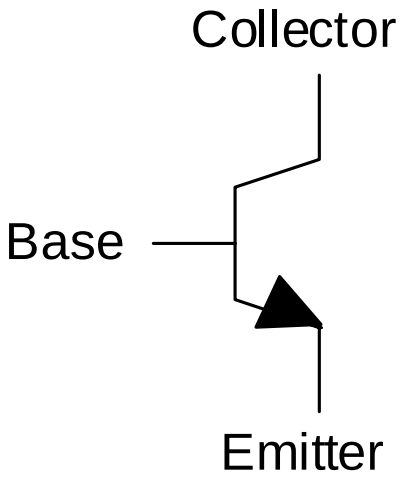
Lots of people supported the industry (primarily radio, later radio and TV) with repair shops throughout the country

(pictures from WEB pages of companies)

Tubes as well as resistors and capacitors had poor reliability

The Bipolar Transistor (Bipolar Junction Transistor – BJT)





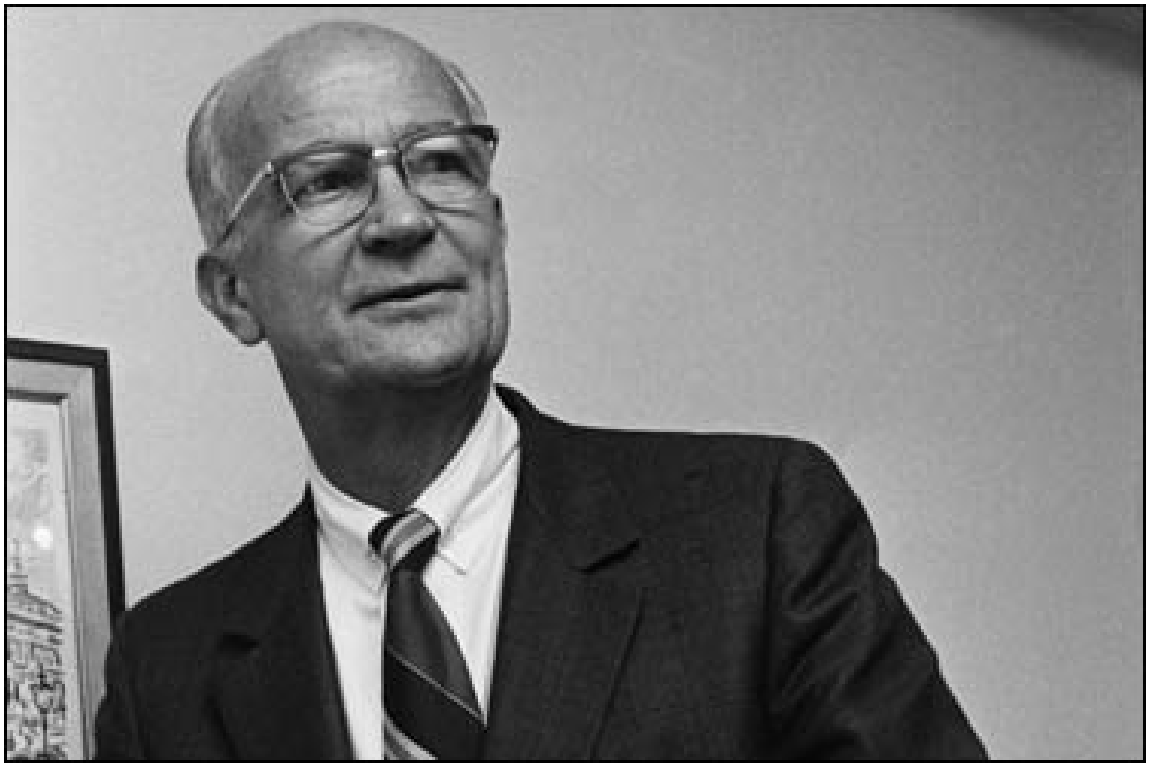
Late 1947

A solution to a major bottleneck limiting the development of electronics technology !

Naming the Transistor

From the group at Bell Labs

"We have called it the transistor, T-R-A-N-S-I-S-T-O-R, because it is resistor or semiconductor device which can amplify electrical signals as they are transferred through it from input to output terminals. It is, if you will, the electrical equivalent of a vacuum tube amplifier. But there the similarity ceases. It has no vacuum, no filament, no glass tube. It is composed entirely of cold, solid substances."



William Shockley

http://www.time.com/time/time100/scientist/profile/shockley03.html

William Shockley

He fathered the transistor and brought the silicon to Silicon Valley but is remembered by many only for his noxious racial views

By GORDON MOORE

Gordon Moore

The transistor was born just before Christmas 1947 when John Bardeen and Walter Brattain, two scientists working for William Shockley at Bell Telephone Laboratories in Murray Hill, N.J., observed that when electrical signals were applied to contacts on a crystal of germanium, the output power was larger than the input. Shockley was not present at that first observation. And though he fathered the discovery in the same way Einstein fathered the atom bomb, by advancing the idea and pointing the way, he felt left out of the momentous occasion.

Shockley, a very competitive and sometimes infuriating man, was determined to make his imprint on the discovery. He searched for an explanation of the effect from what was then known of the quantum physics of semiconductors. In a remarkable series of insights made over a few short weeks, he greatly extended the understanding of semiconductor materials and developed the underlying theory of another, much more robust amplifying device — a kind of sandwich made of a crystal with varying impurities added, which came to be known as the junction transistor. By 1951 Shockley's co-workers made his semiconductor sandwich and demonstrated that it behaved much as his theory had predicted.

Not content with his lot at Bell Labs, Shockley set out to capitalize on his invention. In doing so, he played a key role in the industrial development of the region at the base of the San Francisco Peninsula. It was Shockley who brought the silicon to Silicon Valley.

In February 1956, with financing from Beckman Instruments Inc., he founded Shockley Semiconductor Laboratory with the goal of developing and producing a silicon transistor. He chose to establish this start-up near Palo Alto, where he had grown up and where his mother still lived. He set up operations in a storefront — little more than a Quonset hut — and hired a group of young scientists (I was one of them) to develop the necessary technology. By the spring of 1956 he had a small staff in place and was beginning to undertake research and development.

…. (in early 1957 a group of the key people involved with Shockley left and formed a new company named Fairchild Semiconductor …) This new company, financed by Fairchild Camera & Instrument Corp., became the mother organization for several dozen new companies in Silicon Valley. Nearly all the scores of companies that are or have been active in semiconductor technology can trace the technical lineage of their founders back through Fairchild to the Shockley Semiconductor Laboratory. Unintentionally, Shockley contributed to one of the most spectacular and successful industry expansions in history.

Editor's note:

In 1963 Shockley left the electronics industry and accepted an appointment at Stanford. There he became interested in the origins of human intelligence. Although he had no formal training in genetics or psychology, he began to formulate a theory of what he called dysgenics. Using data from the U.S. Army's crude pre-induction IQ tests, he concluded that African Americans were inherently less intelligent than Caucasians — an analysis that stirred wide controversy among laymen and experts in the field alike.

(Fairchild was formed in 1957 – Moore and Noyce were 2 or 8 co-founders)

End of Lecture 3