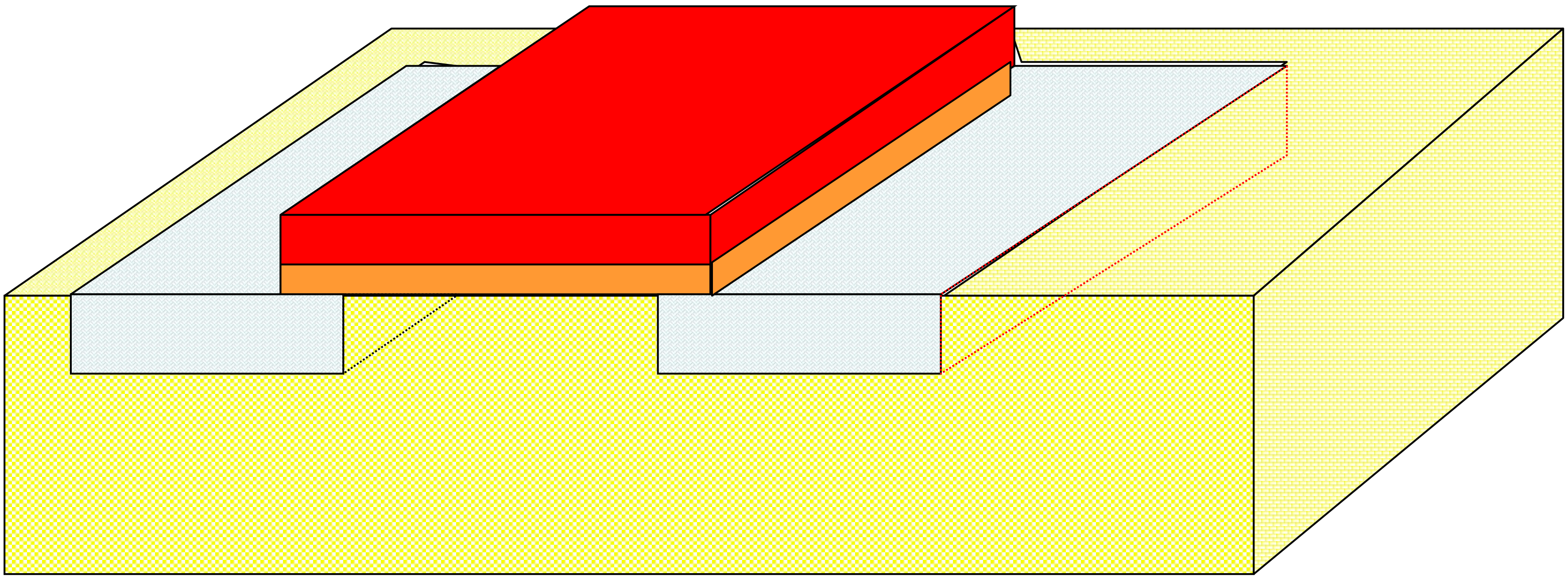
EE 330

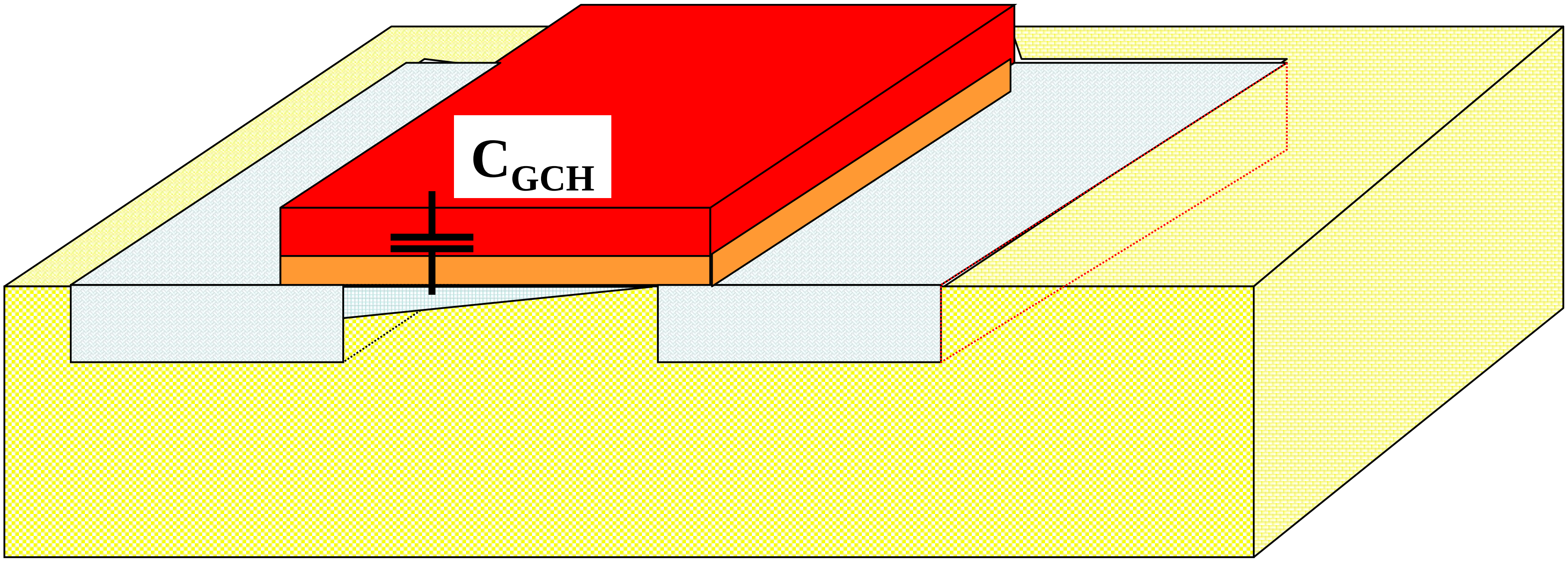
Lecture 35

- Parasitic Capacitances in MOS Devices
- Digital Systems

Parasitic Capacitors in MOSFET

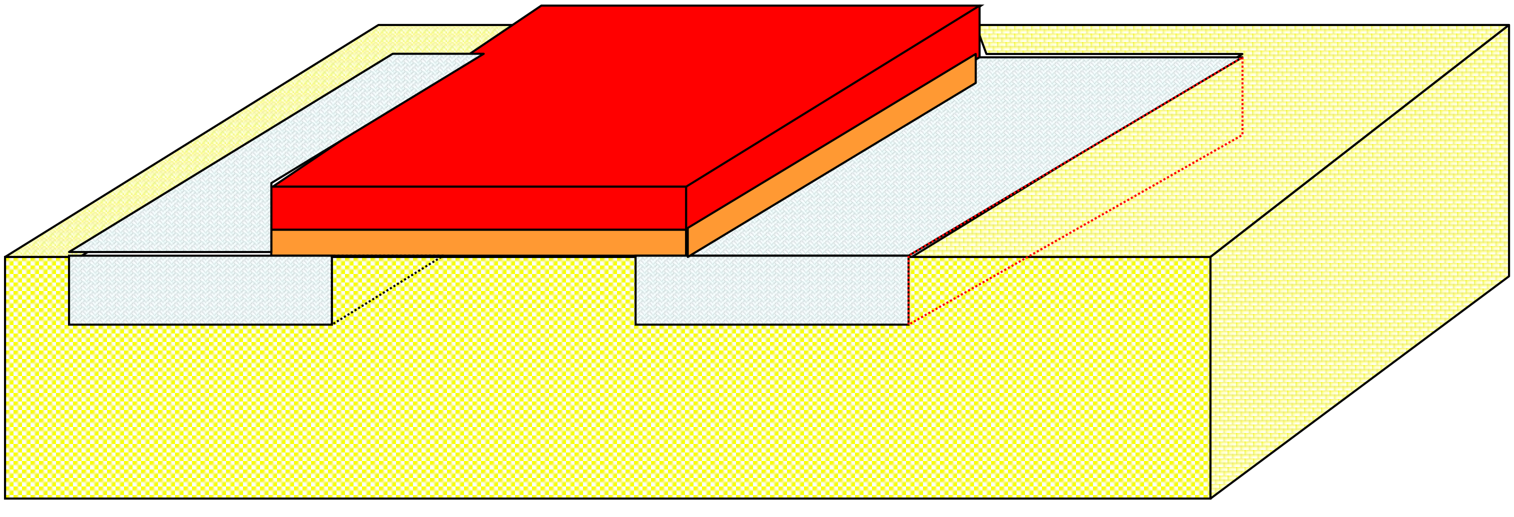


Parasitic Capacitors in MOSFET

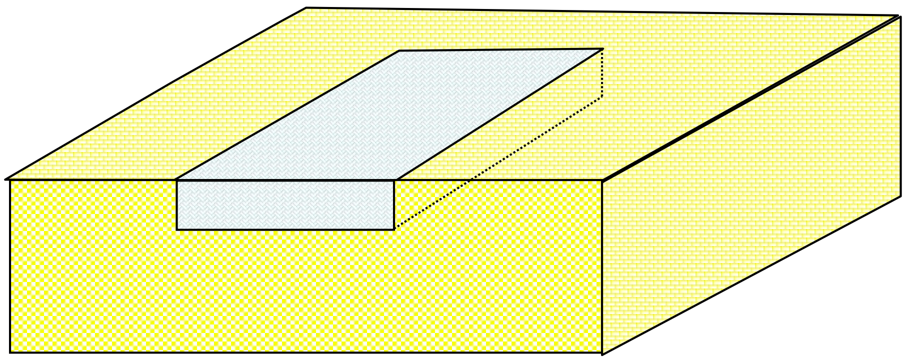


- This capacitance was modeled previously and exists when the transistor is operating in triode or saturation
- But there are others that also affect high-frequency or high-speed operation

Parasitic Capacitors in MOSFET

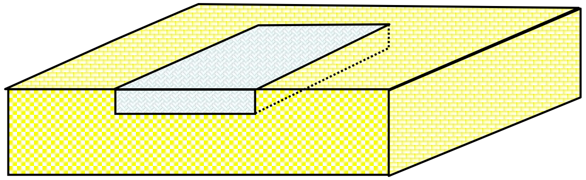


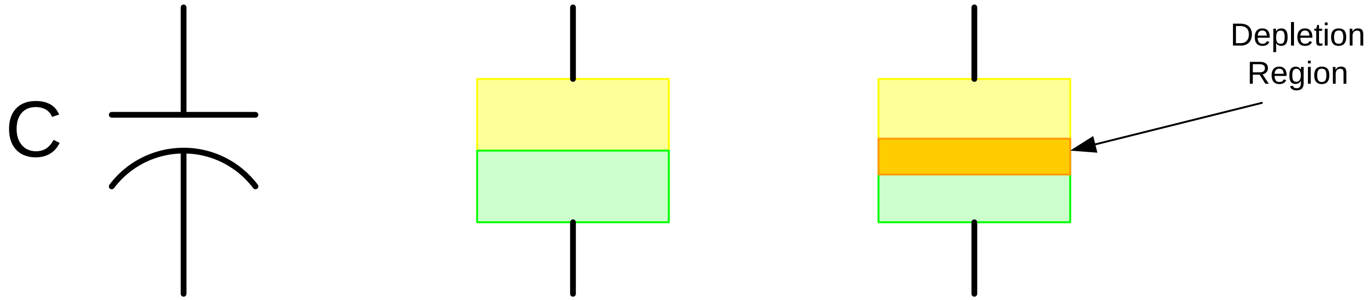
Recall that pn junctions have a depletion region!



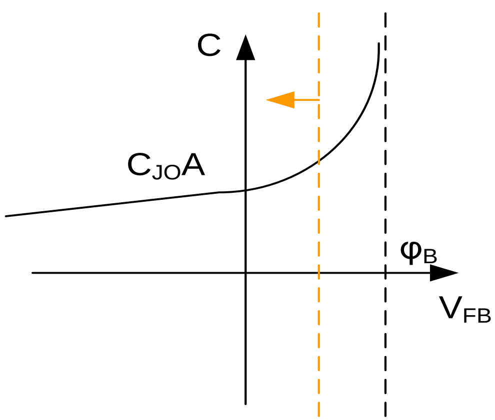
Parasitic Capacitors in MOSFET

pn junction capacitance





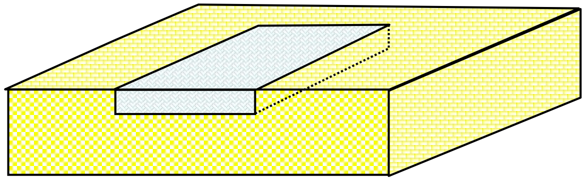
For $V_{FB}<\varphi_B/2$



$$C = \frac{C_{J0}A}{\left(1-\frac{V_{FB}}{\varphi_B}\right)^m}$$

Parasitic Capacitors in MOSFET

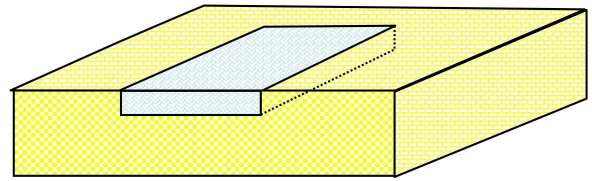
pn junction capacitance

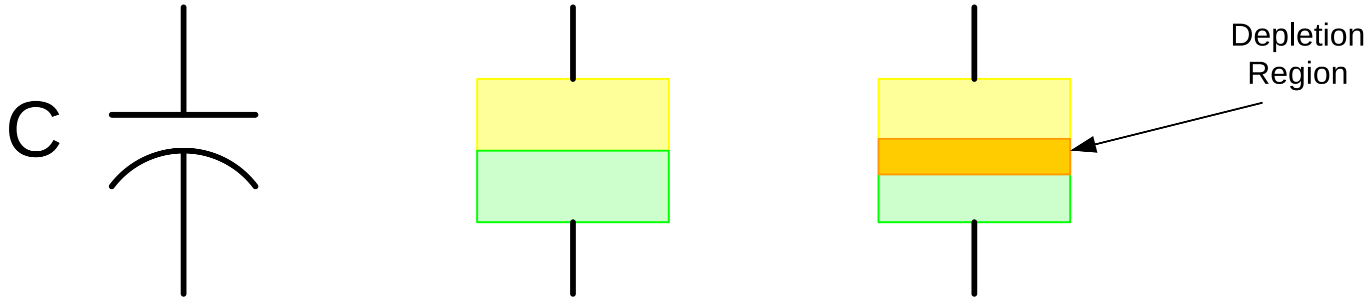


The bottom and the sidewall:

Parasitic Capacitors in MOSFET

pn junction capacitance





For a pn junction capacitor

$$C_J = C_{BOT} A + C_{SW} P$$

$$C_{BOT} = \frac{C_{BOT} A}{\left(1 - \frac{V_{FB}}{\varphi_B}\right)^m} \qquad C_{SW} = \frac{C_{SW} P}{\left(1 - \frac{V_{FB}}{\varphi_B}\right)^m}$$

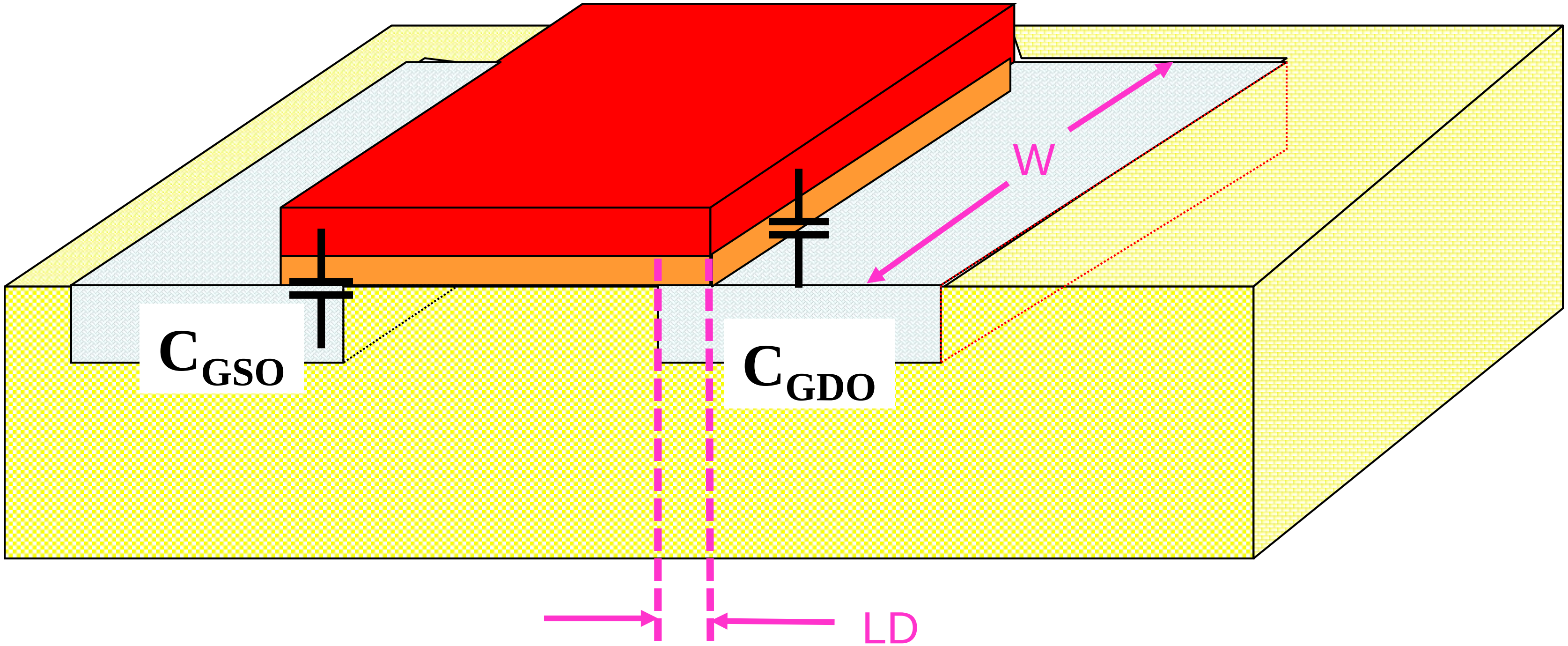
Types of Capacitors in MOSFETs

1. Fixed Capacitors
    a. Fixed Geometry
    b. Junction

2. Operating Region Dependent

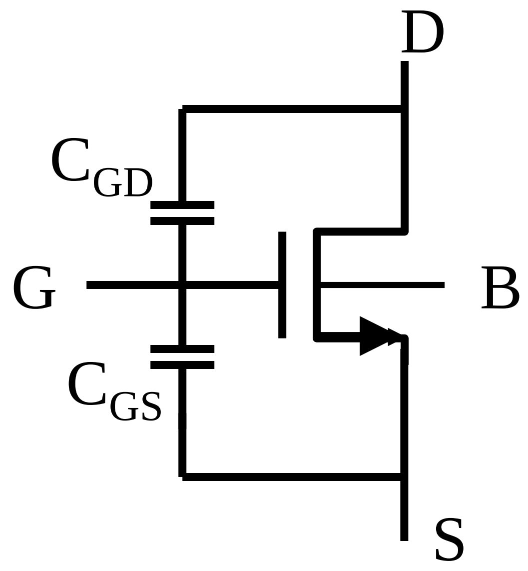
Parasitic Capacitors in MOSFET

Fixed Capacitors – Fixed Geometry



Overlap Capacitors: C_{GDO}, C_{GSO}

Parasitic Capacitance Summary



	Cutoff	Ohmic	Saturation
C_{GS}	$CoxWL_D$	$CoxWL_D$	$CoxWL_D$
C_{GD}	$CoxWL_D$	$CoxWL_D$	$CoxWL_D$

L_D is a model parameter

Overlap Capacitance Model Parameters

CAPACITANCE PARAMETERS	N+	P+	POLY	M1	M2	M3	M4	M5	M6	R_W	D_N_W	M5P	N_W	UNITS
Area (substrate)	942	1163	106	34	14	9	6	5	3		123		125	aF/um^2
Area (N+active)			8484	55	20	13	11	9	8					aF/um^2
Area (P+active)			8232											aF/um^2
Area (poly)				66	17	10	7	5	4					aF/um^2
Area (metal1)					37	14	9	6	5					aF/um^2
Area (metal2)						35	14	9	6					aF/um^2
Area (metal3)							37	14	9					aF/um^2
Area (metal4)								36	14					aF/um^2
Area (metal5)									34			984		aF/um^2
Area (r well)	920													aF/um^2
Area (d well)										582				aF/um^2
Area (no well)	137													aF/um^2
Fringe (substrate)	212	235		41	35	29	21	14						aF/um
Fringe (poly)				70	39	29	23	20	17					aF/um
Fringe (metal1)					52	34		22	19					aF/um
Fringe (metal2)						48	35	27	22					aF/um
Fringe (metal3)							53	34	27					aF/um
Fringe (metal4)								58	35					aF/um
Fringe (metal5)									55					aF/um
Overlap (N+active)			895											aF/um
Overlap (P+active)			737											aF/um

Types of Capacitors in MOSFETs

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    a. Fixed Geometry
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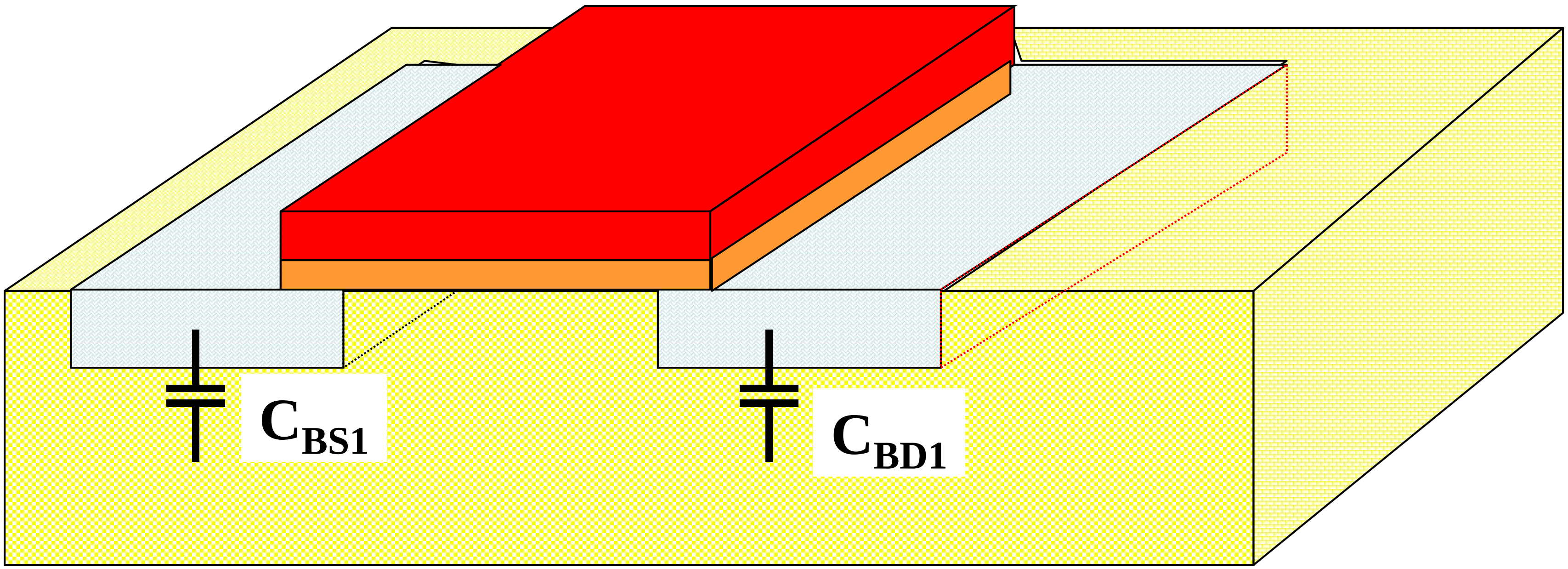
2. Operating Region Dependent

Parasitic Capacitors in MOSFET

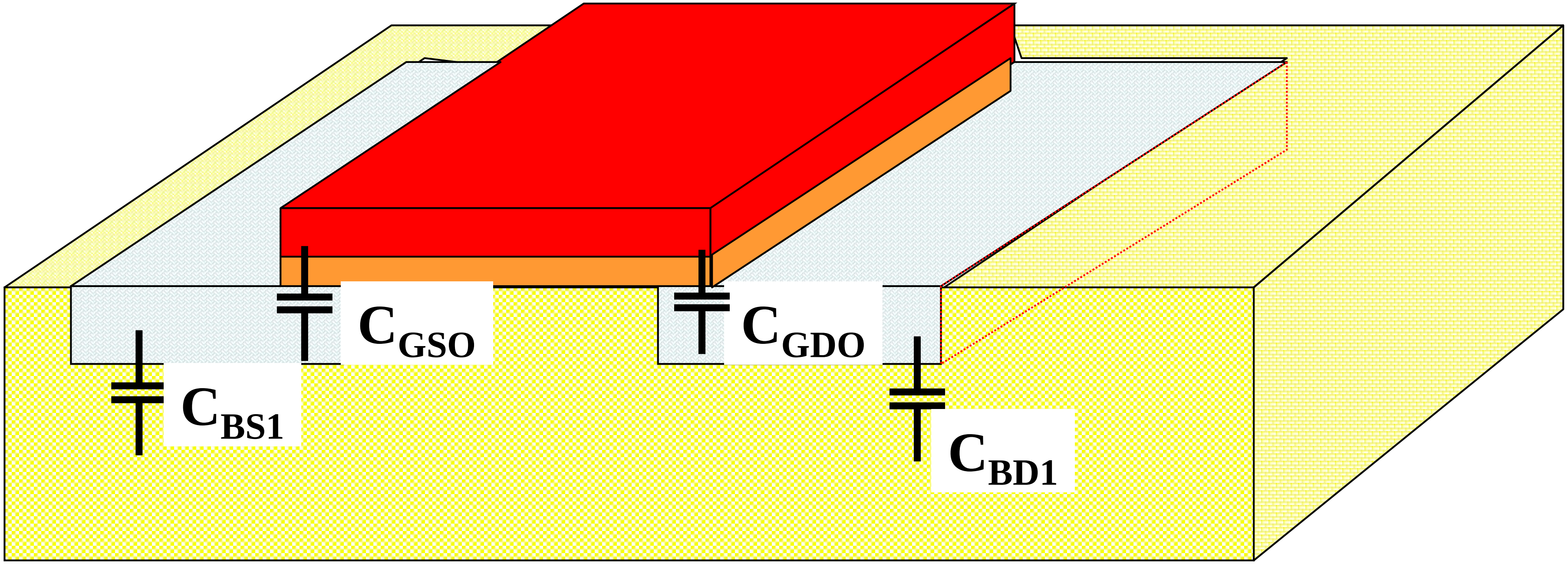
Fixed Capacitors- Junction



Junction Capacitors: C_{BS1}, C_{BD1}

Parasitic Capacitors in MOSFET

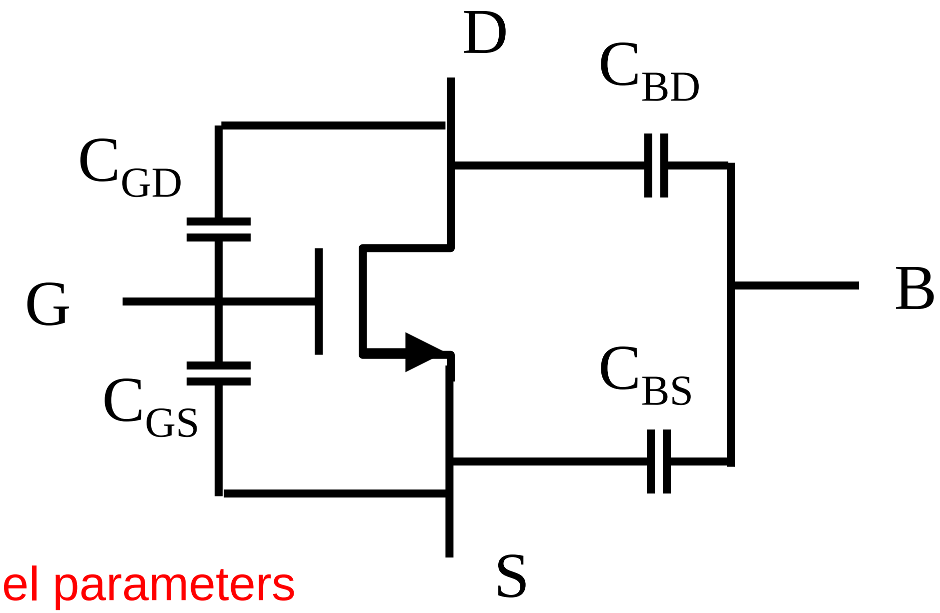
Fixed Capacitors



Overlap Capacitors: C_{GDO}, C_{GSO}

Junction Capacitors: C_{BS1}, C_{BD1}

Fixed Parasitic Capacitance Summary



C_{BOT} and C_{SW} are model parameters

	Cutoff	Ohmic	Saturation
C_{GS}	$C_{ox}WL_D$	$C_{ox}WL_D$	$C_{ox}WL_D$
C_{GD}	$C_{ox}WL_D$	$C_{ox}WL_D$	$C_{ox}WL_D$
C_{BG}			
C_{BS}	$C_{BS1} = C_{BOT}A_S+C_{SW}P_S$	$C_{BS1} = C_{BOT}A_S+C_{SW}P_S$	$C_{BS1} = C_{BOT}A_S+C_{SW}P_S$
C_{BD}	$C_{BD1} = C_{BOT}A_D+C_{SW}P_D$	$C_{BD1} = C_{BOT}A_D+C_{SW}P_D$	$C_{BD1} = C_{BOT}A_D+C_{SW}P_D$

C_{BOT} and C_{SW} model parameters

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Types of Capacitors in MOSFETs

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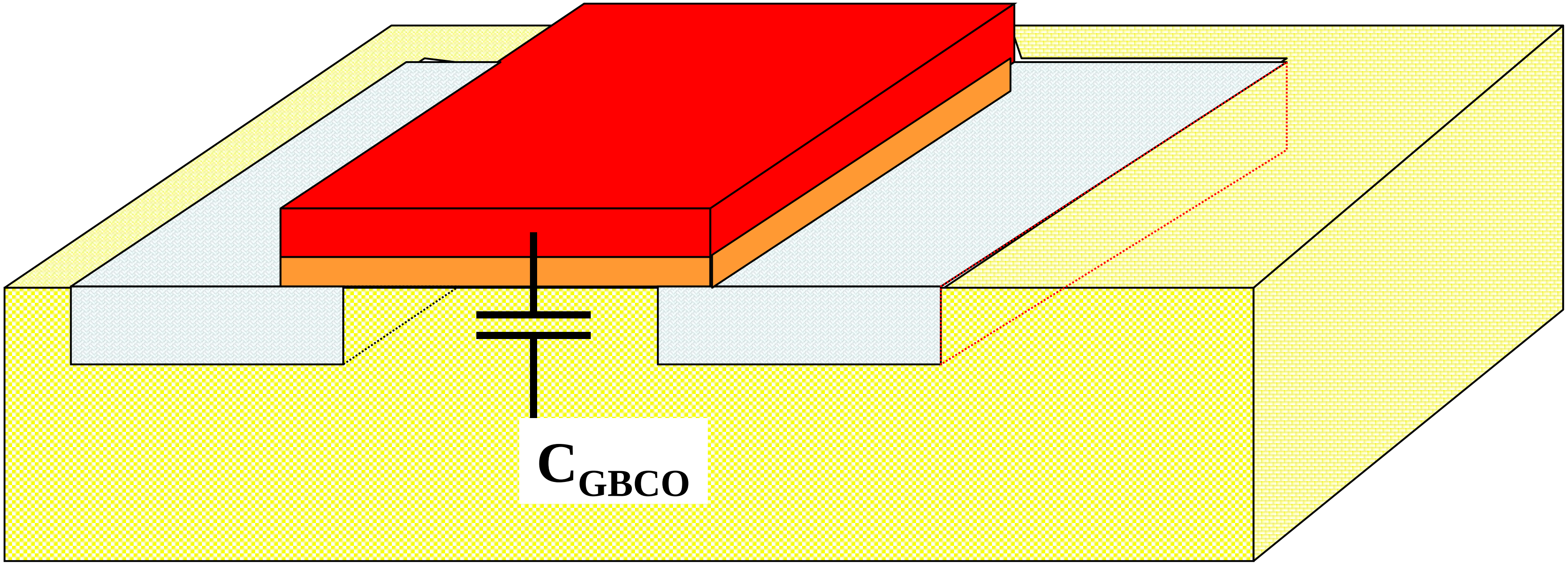
2. Operating Region Dependent

Parasitic Capacitors in MOSFET

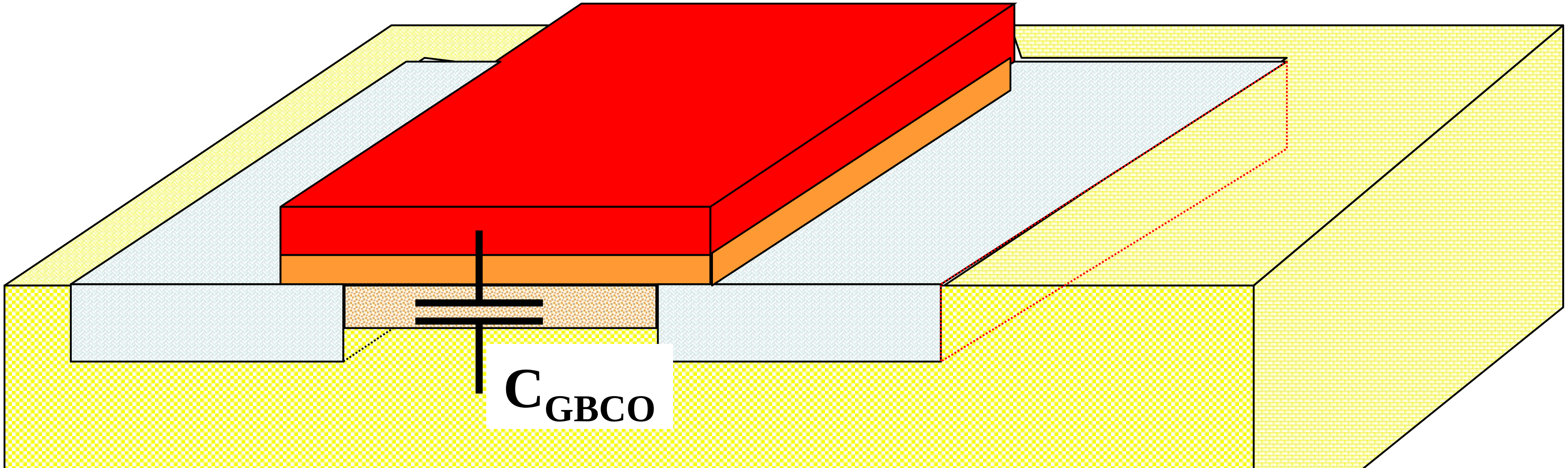
Operation Region Dependent -- Cutoff



Cutoff Capacitor: C_{GBCO}

Parasitic Capacitors in MOSFET

Operation Region Dependent -- Cutoff

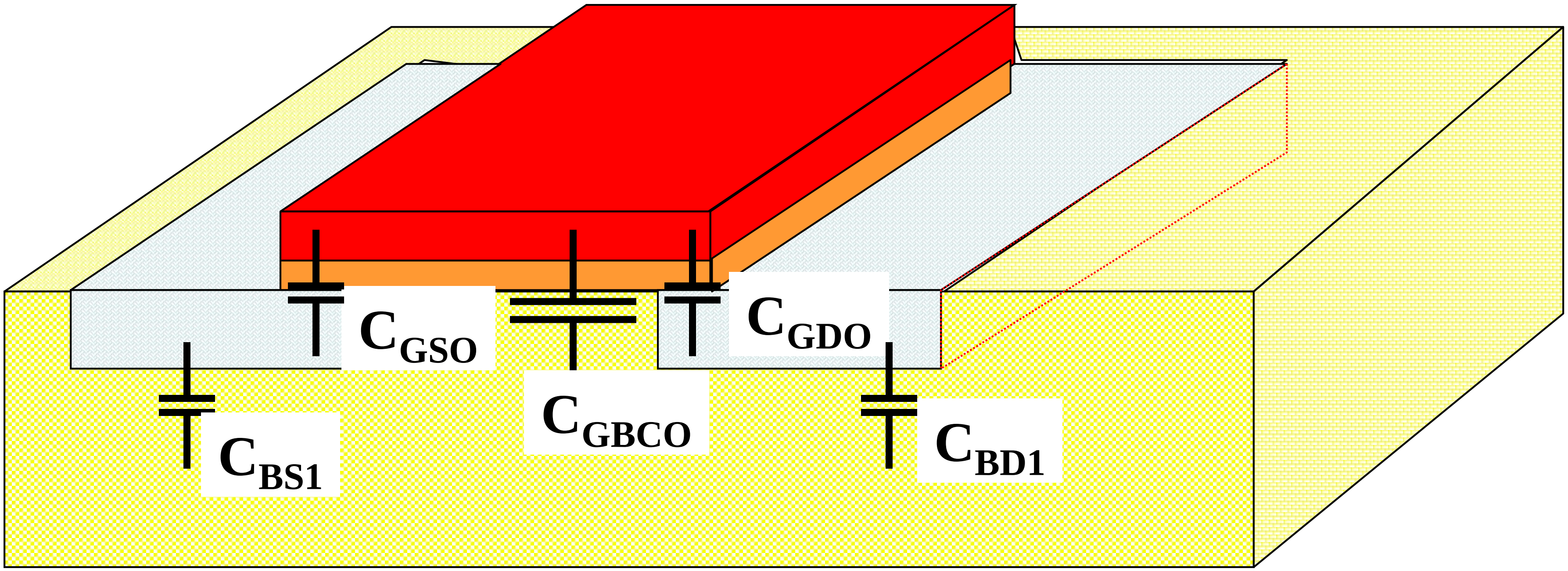


Note: A depletion region will form under the gate if a positive Gate voltage is applied thus decreasing the capacitance density

Cutoff Capacitor: C_{GBCO}

Parasitic Capacitors in MOSFET

Operation Region Dependent and Fixed -- Cutoff

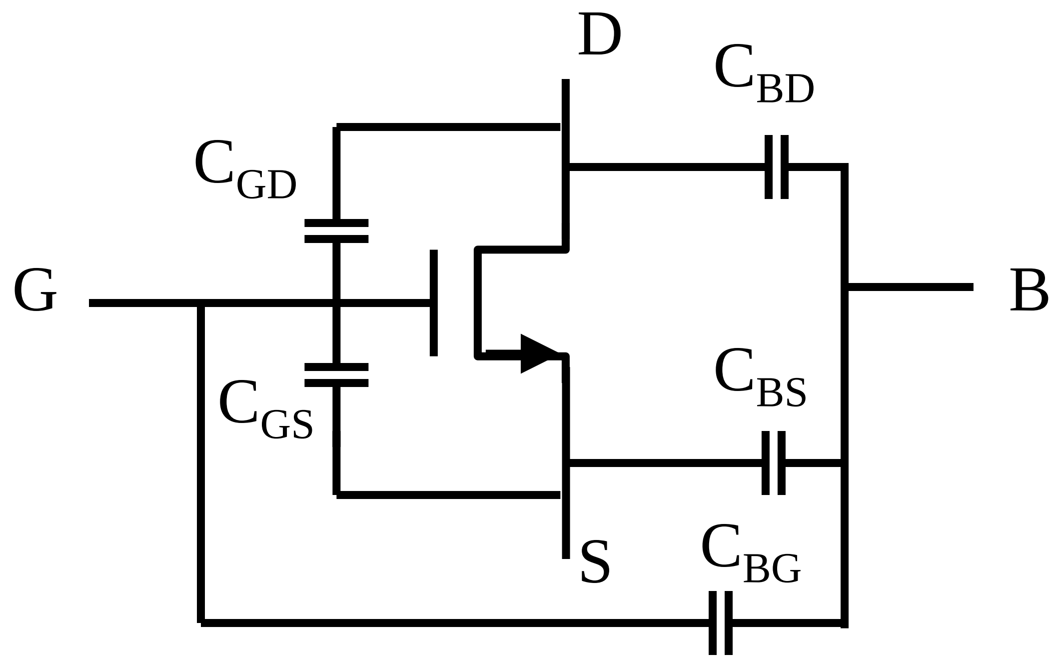


Overlap Capacitors: C_{GDO}, C_{GSO}

Junction Capacitors: C_{BS1}, C_{BD1}

Cutoff Capacitor: C_{GBCO}

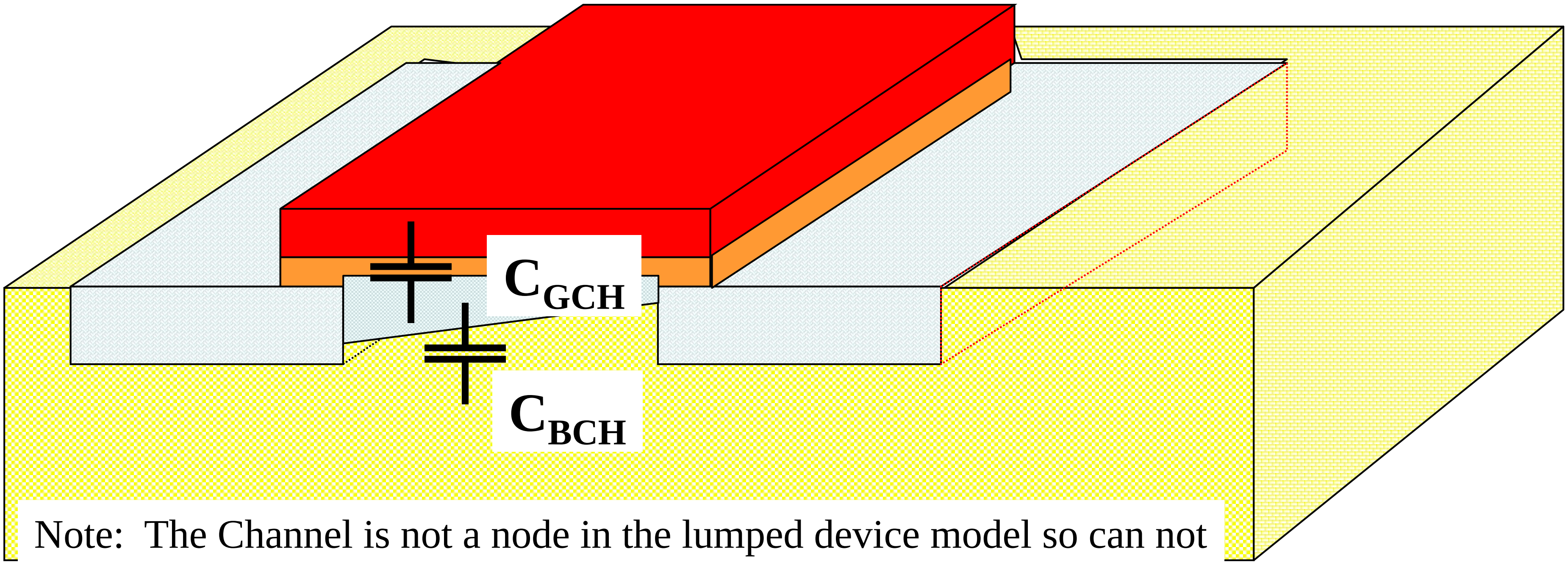
Parasitic Capacitance Summary



	Cutoff	Ohmic	Saturation
C_{GS}	$C_{ox}WL_D$		
C_{GD}	$C_{ox}WL_D$		
C_{BG}	$C_{ox}WL$ (or less)		
C_{BS}	$C_{BOT}A_S+C_{SW}P_S$		
C_{BD}	$C_{BOT}A_D+C_{SW}P_D$		

Parasitic Capacitors in MOSFET

Operation Region Dependent -- Ohmic



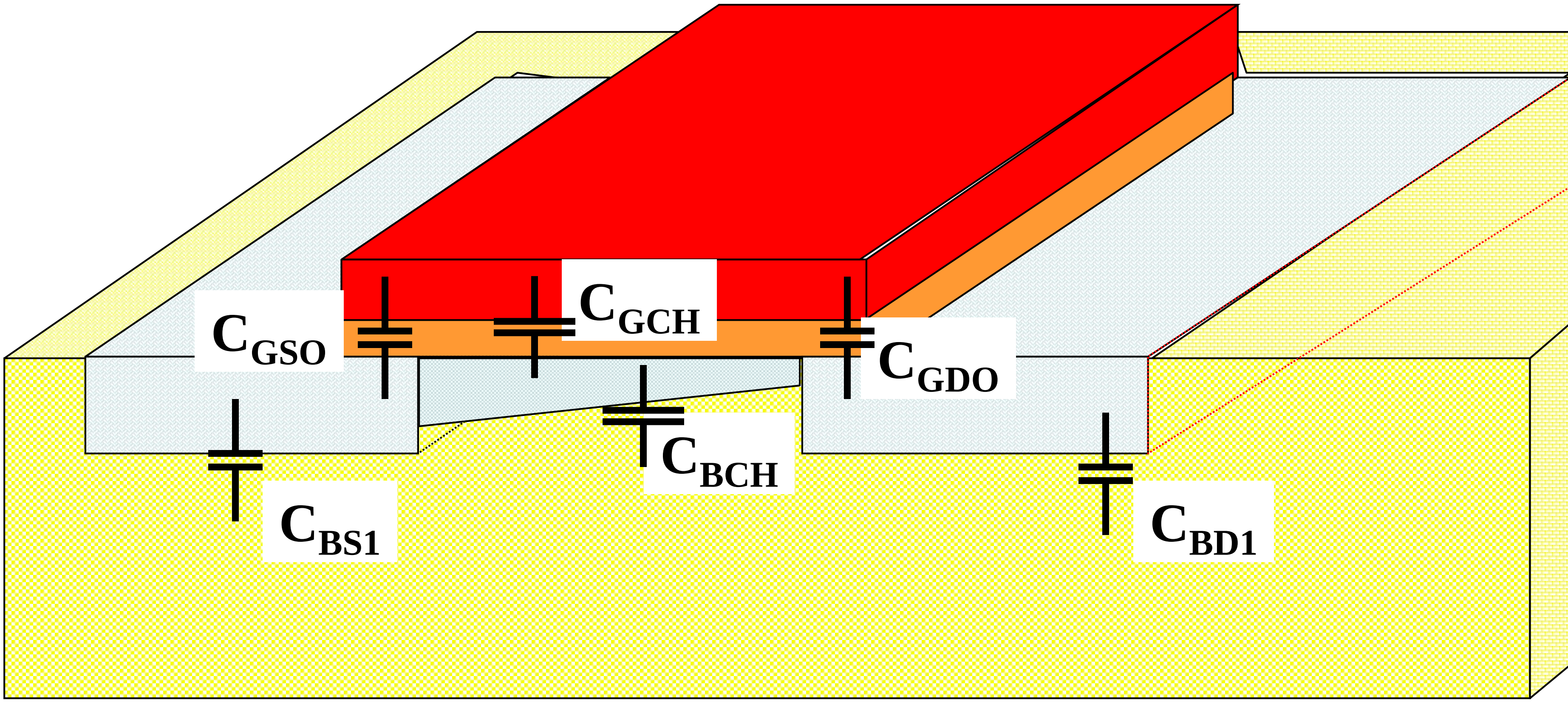
Note: The Channel is not a node in the lumped device model so can not directly include this distributed capacitance in existing models

Note: The distributed channel capacitance is usually lumped and split evenly between the source and drain nodes

Ohmic Capacitor: C_{GCH} , C_{BCH}

Parasitic Capacitors in MOSFET

Operation Region Dependent and Fixed -- Ohmic

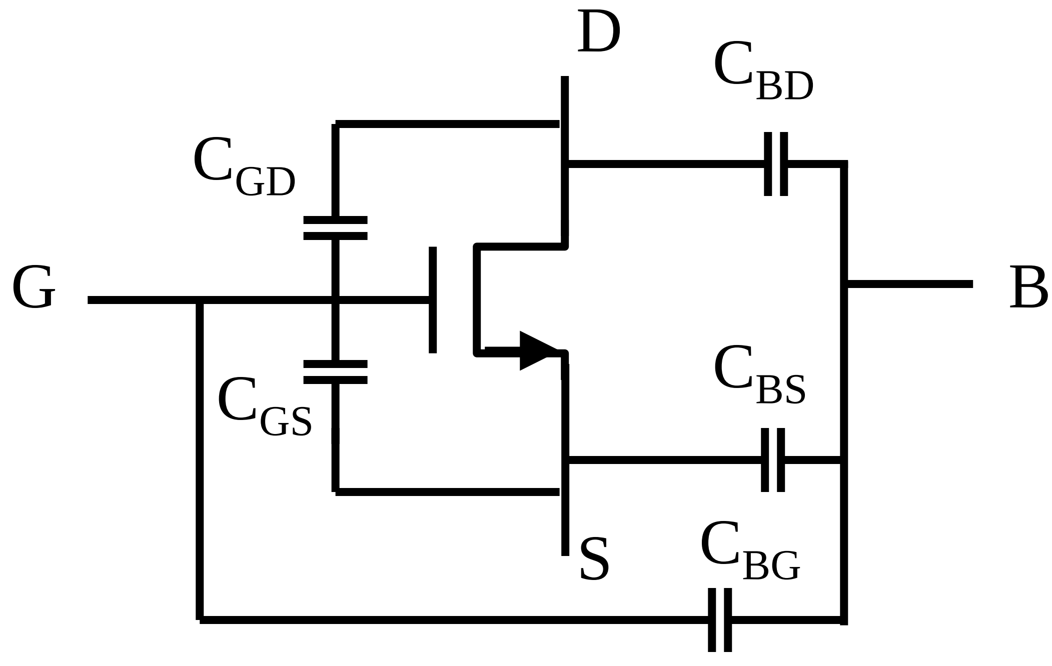


Overlap Capacitors: C_{GDO}, C_{GSO}

Junction Capacitors: C_{BS1}, C_{BD1}

Ohmic Capacitor: C_{GCH} , C_{BCH}

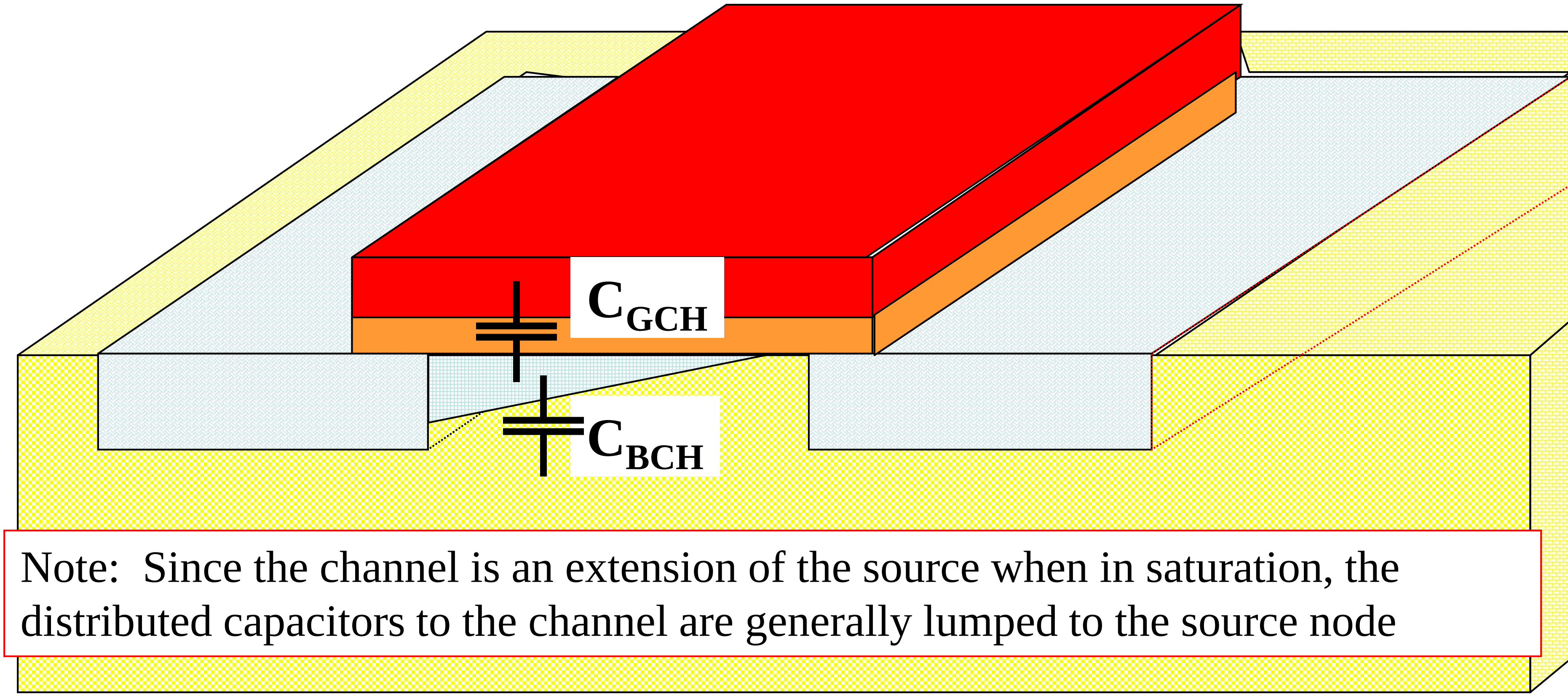
Parasitic Capacitance Summary



	Cutoff	Ohmic	Saturation
C_{GS}	$C_{ox}WL_D$	$C_{ox}WL_D$	
C_{GD}	$C_{ox}WL_D$	$C_{ox}WL_D$	
C_{BG}	$C_{ox}WL$ (or less)	0	
C_{BS}	$C_{BOT}A_S+C_{SW}P_S$	$C_{BS1} = C_{BOT}A_S+C_{SW}P_S$	
C_{BD}	$C_{BOT}A_D+C_{SW}P_D$	$C_{BD1} = C_{BOT}A_D+C_{SW}P_D$	

Parasitic Capacitors in MOSFET

Operation Region Dependent -- Saturation

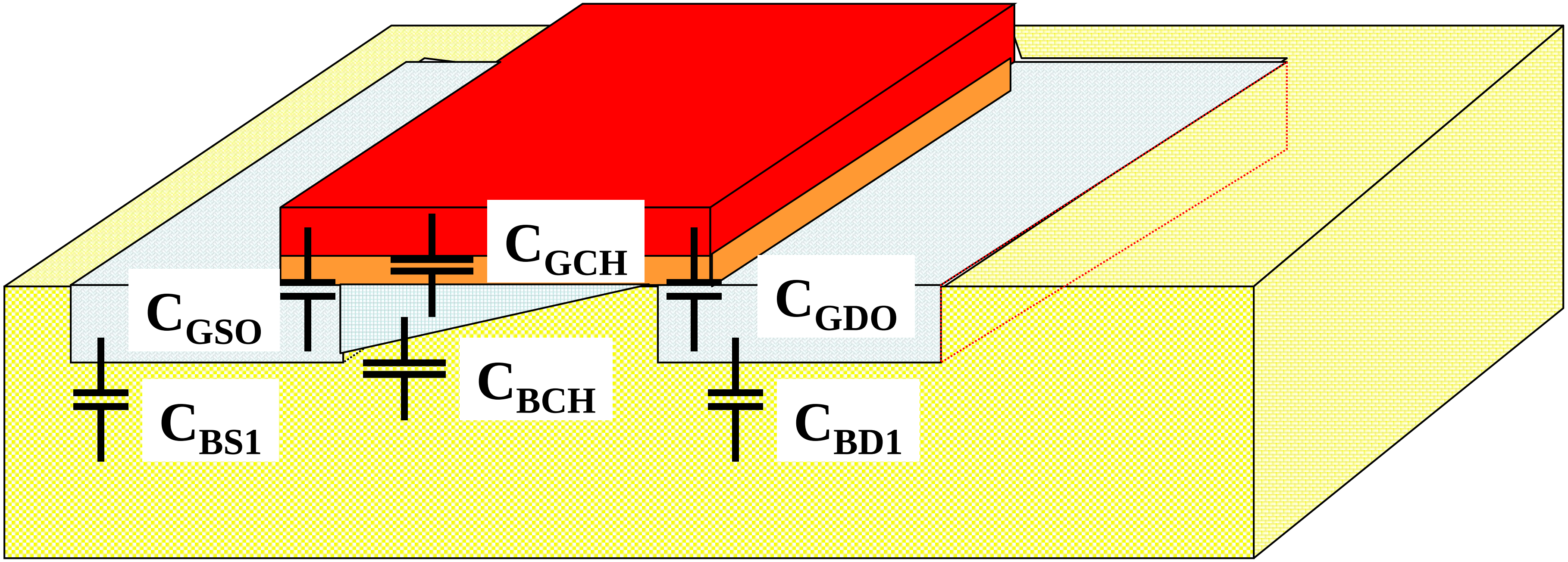


Note: Since the channel is an extension of the source when in saturation, the distributed capacitors to the channel are generally lumped to the source node

Saturation Capacitors: C_{GCH} , C_{BCH}

Parasitic Capacitors in MOSFET

Operation Region Dependent and Fixed --Saturation



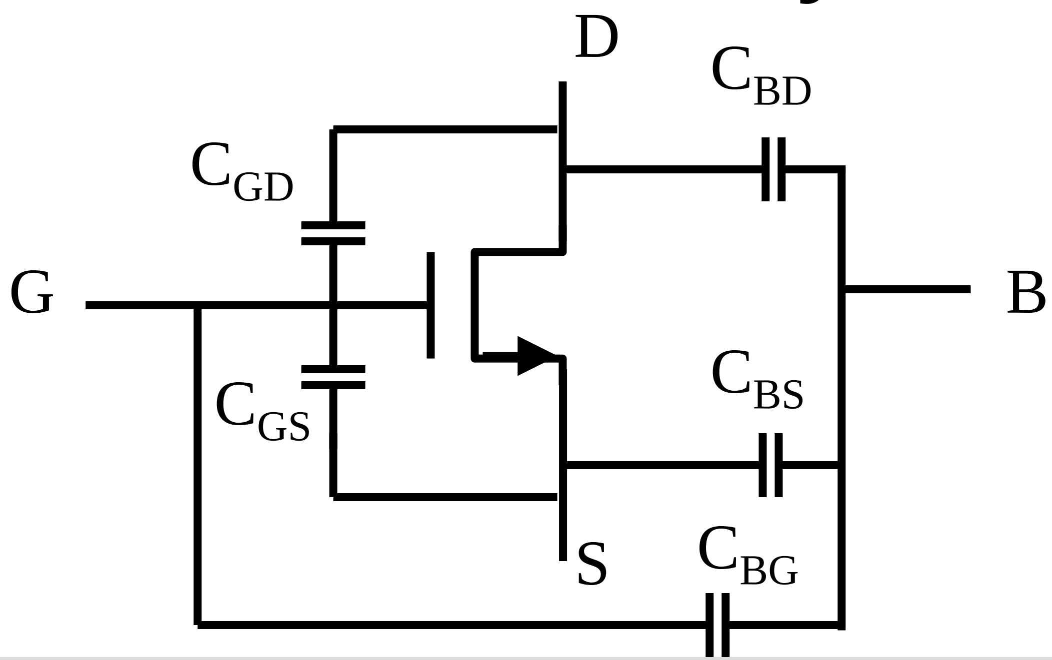
Overlap Capacitors: C_{GDO}, C_{GSO}

Junction Capacitors: C_{BS1}, C_{BD1}

Saturation Capacitors: C_{GCH} , C_{BCH}

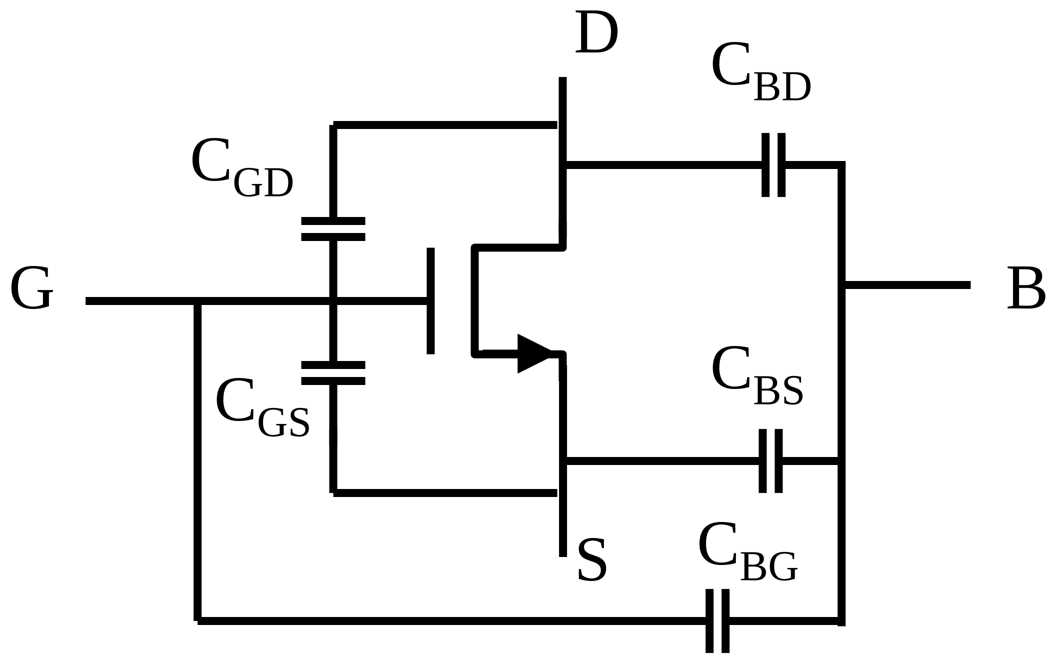
- 2/3 $C_{OX}WL$ is often attributed to C_{GCH} to account for LD and saturation
- This approximation is reasonable for minimum-length devices but not so good for longer devices

Parasitic Capacitance Summary



	Cutoff	Ohmic	Saturation
C_{GS}	$C_{ox}WL_D$	$C_{ox}WL_D + 0.5C_{OX}WL$	$C_{ox}WL_D+(2/3)C_{OX}WL$
C_{GD}	$C_{ox}WL_D$	$C_{ox}WL_D + 0.5C_{OX}WL$	$C_{ox}WL_D$
C_{BG}	$C_{ox}WL$ (or less)	0	0
C_{BS}	$C_{BOT}A_S+C_{SW}P_S$	$C_{BOT}A_S+C_{SW}P_S+0.5WLC_{BOTCH}$	$C_{BOT}A_S+C_{SW}P_S +(2/3)WLC_{BOTCH}$
C_{BD}	$C_{BOT}A_D+C_{SW}P_D$	$C_{BOT}A_D+C_{SW}P_D+0.5WLC_{BOTCH}$	$C_{BOT}A_D+C_{SW}P_D$

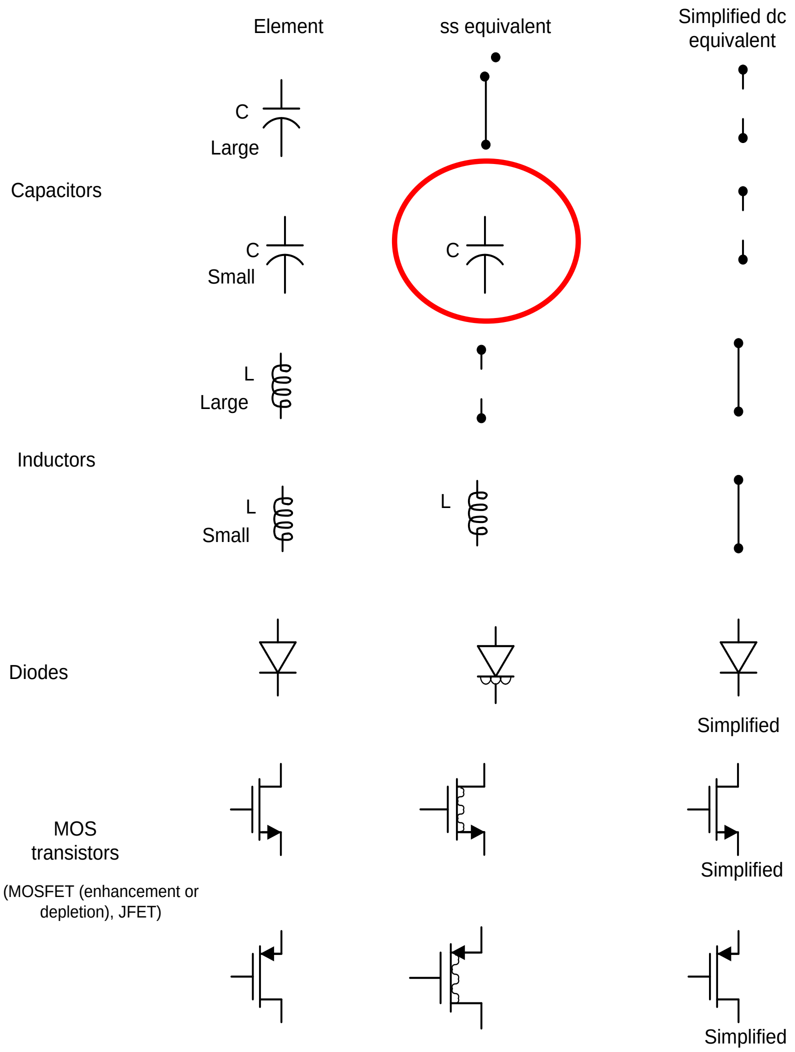
Parasitic Capacitance Summary



	Cutoff	**Ohmic**	**Saturation**
C_{GS}	$C_{ox}WL_D$	$C_{ox}WL_D + 0.5C_{OX}WL$	$C_{ox}WL_D+(2/3)C_{OX}WL$
C_{GD}	$C_{ox}WL_D$	$C_{ox}WL_D + 0.5C_{OX}WL$	$C_{ox}WL_D$
C_{BG}	$C_{ox}WL$ (or less)	0	0
C_{BS}	$C_{BOT}A_S+C_{SW}P_S$	$C_{BOT}A_S+C_{SW}P_S+0.5WLC_{BOTCH}$	$C_{BOT}A_S+C_{SW}P_S+(2/3)WLC_{BOTCH}$
C_{BD}	$C_{BOT}A_D+C_{SW}P_D$	$C_{BOT}A_D+C_{SW}P_D+0.5WLC_{BOTCH}$	$C_{BOT}A_D+C_{SW}P_D$

Recall:

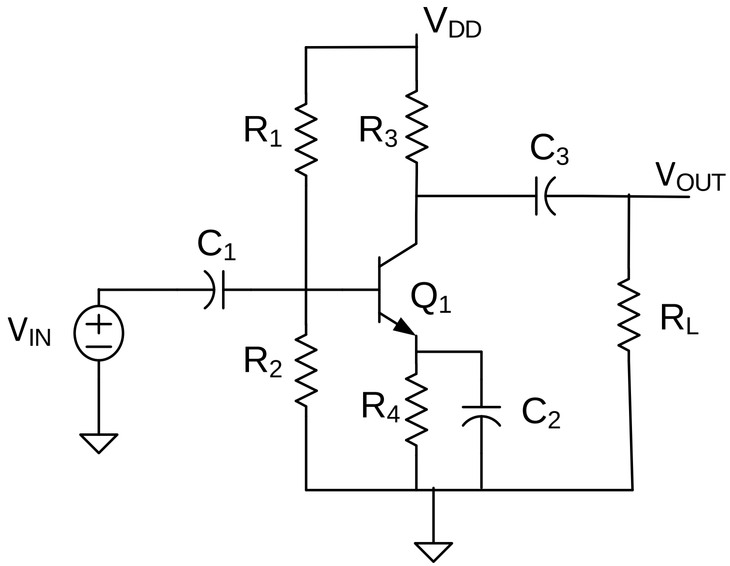
Small-signal and simplified dc equivalent elements



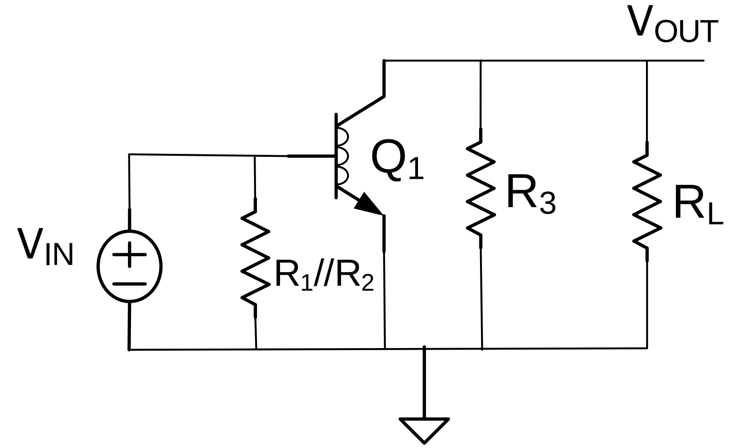
Have not yet considered situations where the small capacitor is relevant in small-signal analysis

Amplifiers with Small Capacitors

Recall:



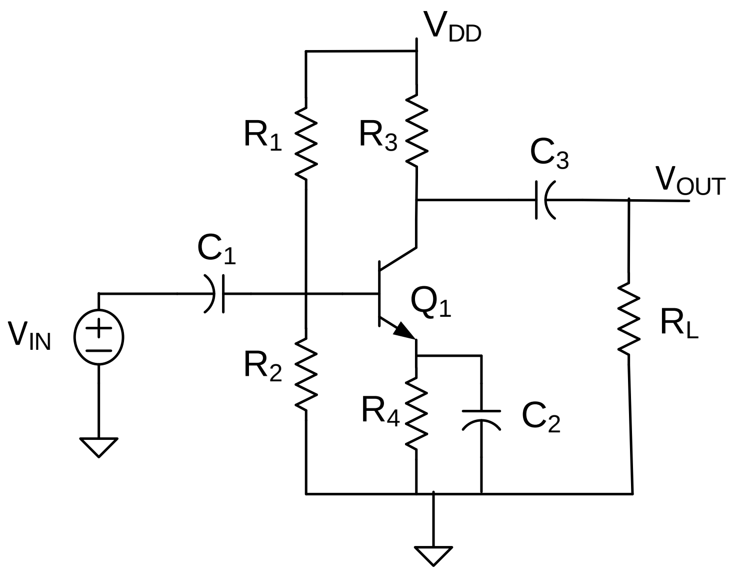
If capacitors are large

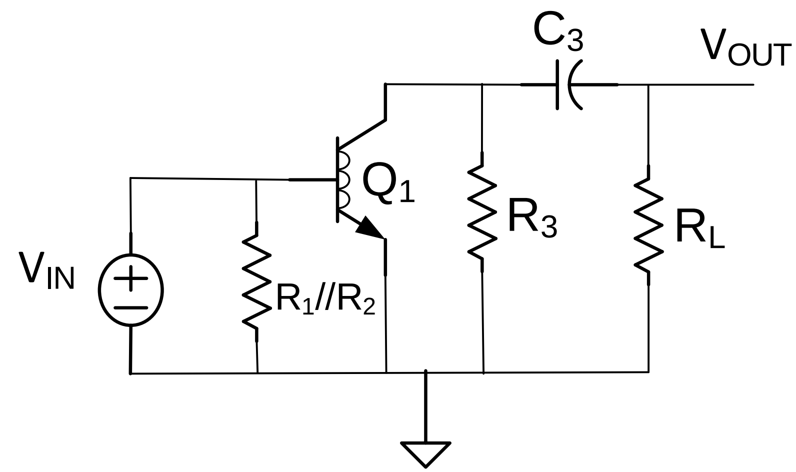


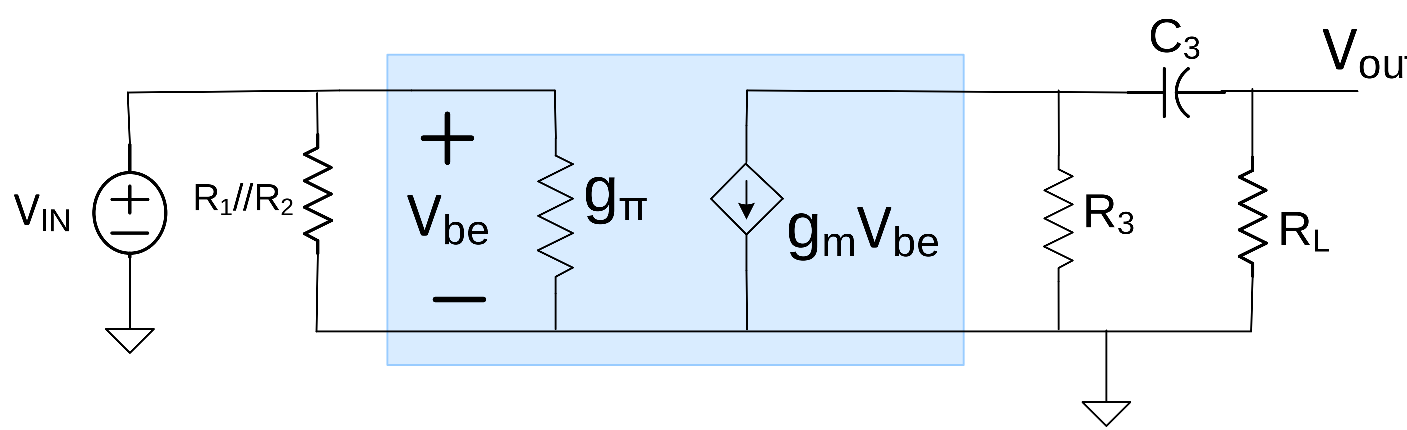
$$A_V = -g_{m1} \bullet R_3 // R_L$$

Amplifiers with Small Capacitors

What if C_1 and C_2 large but C_3 not large?:

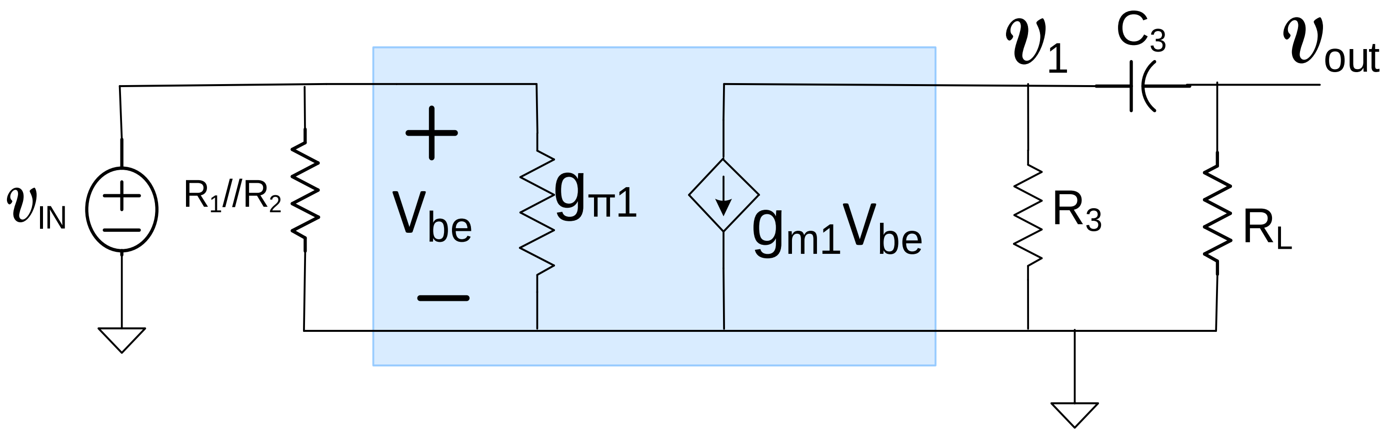






Amplifiers with Small Capacitors

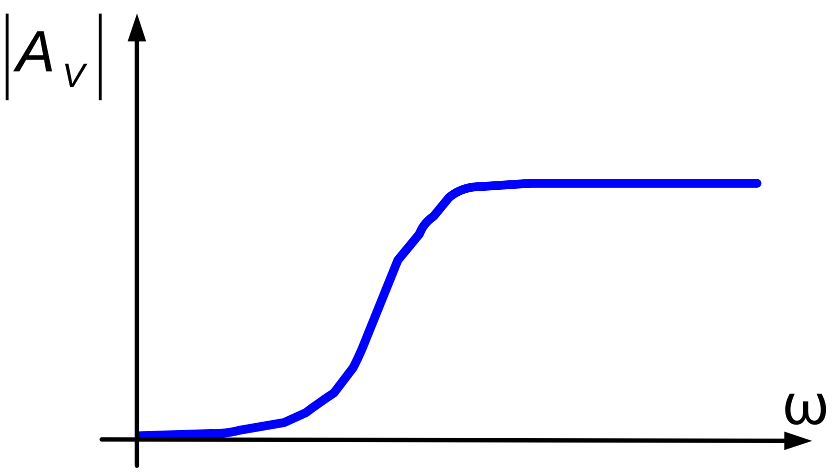
What if C_1 and C_2 large but C_3 not large?:



From KCL:

$$\left.\begin{aligned} v_{OUT}\left(sC_3+G_L\right) &= v_1 sC_3 \\ v_1\left(sC_3+G_3\right)+g_{m1}v_{IN} &= v_{OUT}sC_3 \end{aligned}\right\}$$

Serves as a first-order high-pass filter



Solving:

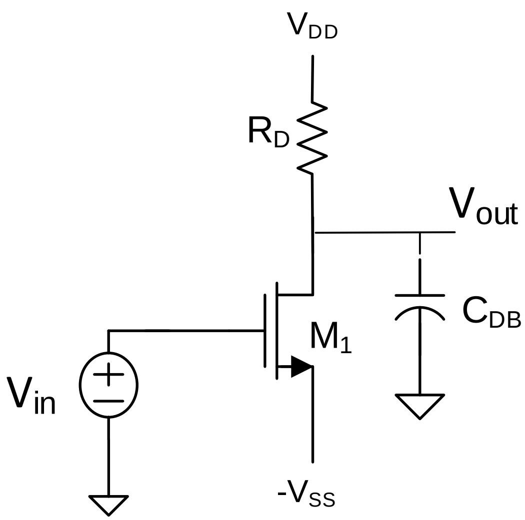
$$\frac{v_{OUT}}{v_{IN}} = -\frac{-sC_3 g_{m1}}{sC_3\left(G_L+G_3\right)+G_3G_L}$$

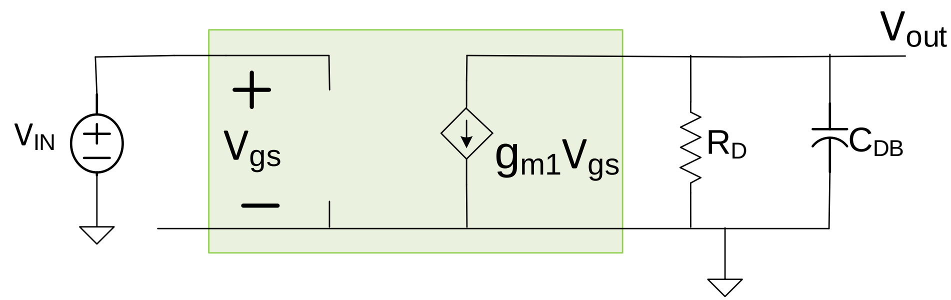
Equivalently:

$$\frac{v_{OUT}}{v_{IN}} = -\frac{g_{m1}sC_3R_3R_L}{sC_3\left(R_L+R_3\right)+1}$$

Amplifiers with Small Capacitors

Consider parasitic C_{DB}





By KCL:

$$v_{OUT}\left(sC_{DB}+G_D\right)=-g_{m1}v_{IN}$$

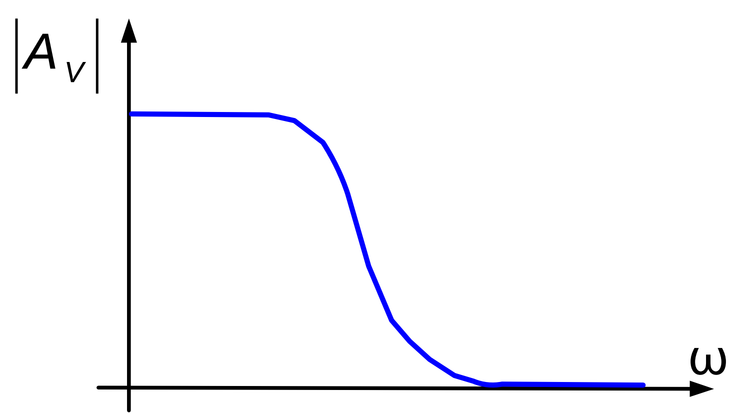
Causes gain to decrease at high frequencies

Solving:

$$\frac{v_{OUT}}{v_{IN}}=-\frac{-g_{m1}}{sC_{DB}+G_D}$$

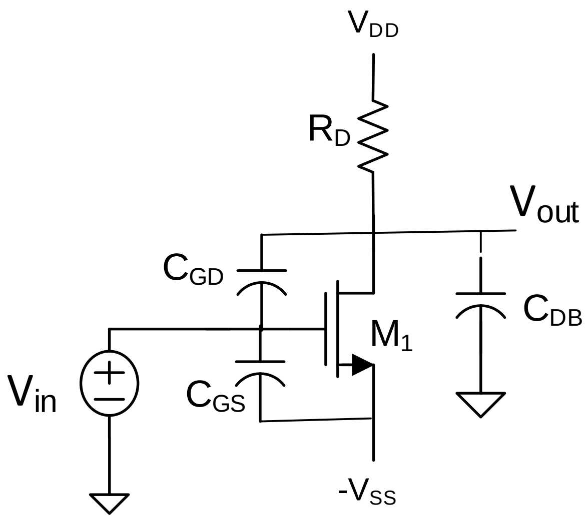
Equivalently:

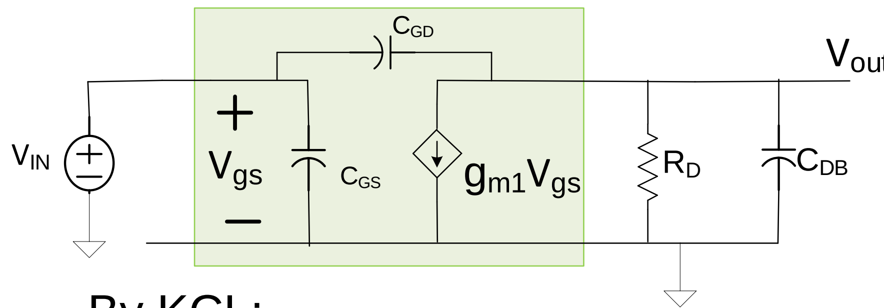
$$\frac{v_{OUT}}{v_{IN}}=-\frac{-g_{m1}R_D}{sC_{DB}R_D+1}$$



Amplifiers with Small Capacitors

Consider parasitic C_{GS}, C_{GD}, and C_{DB}





By KCL:

$$v_{OUT}\left(s\left[C_{DB}+C_{GD}\right]+G_D\right)=-g_{m1}v_{IN}+sC_{GD}v_{IN}$$

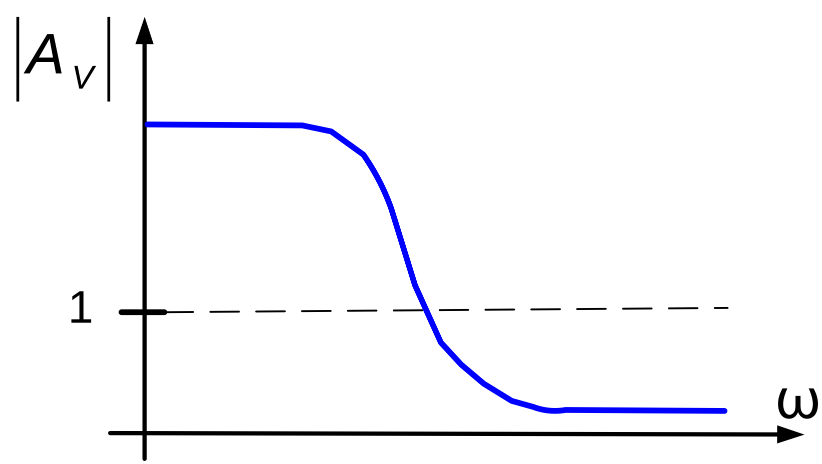
Causes gain to decrease at high frequencies
Has one LHP pole and one RHP zero

Solving:

$$\frac{v_{OUT}}{v_{IN}}=-\frac{-g_{m1}+sC_{GD}}{s\left[C_{DB}+C_{GD}\right]+G_D}$$

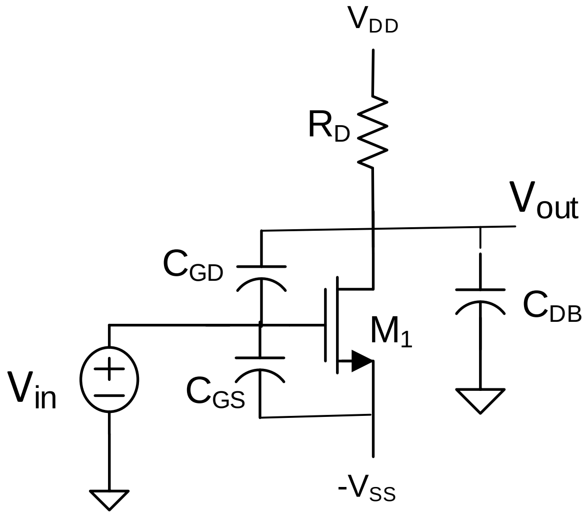
Equivalently:

$$\frac{v_{OUT}}{v_{IN}}=-\frac{-R_D\left(g_{m1}-sC_{GD}\right)}{s\left[C_{DB}+C_{GD}\right]R_D+1}$$



Amplifiers with Small Capacitors

Consider parasitic C_{GS}, C_{GD}, and C_{DB}



Device parasitics problematic at high frequencies

C_{DB}, C_{GD} and C_{GS} effects can be significant

Value of parasitic capacitances strongly dependent upon layout

Device parasitics usually not a problem at audio frequencies

Causes gain to decrease at high frequencies:
has one high frequency LHP pole and one high frequency RHP zero.

End of Lecture 35