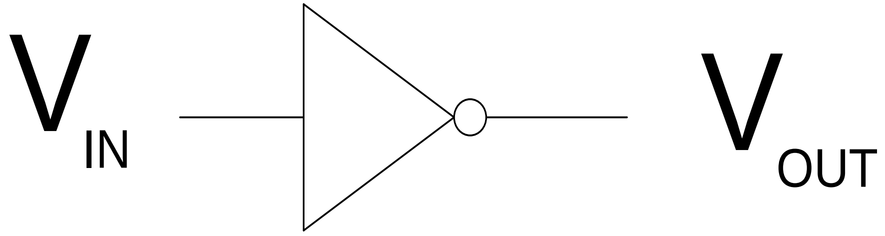
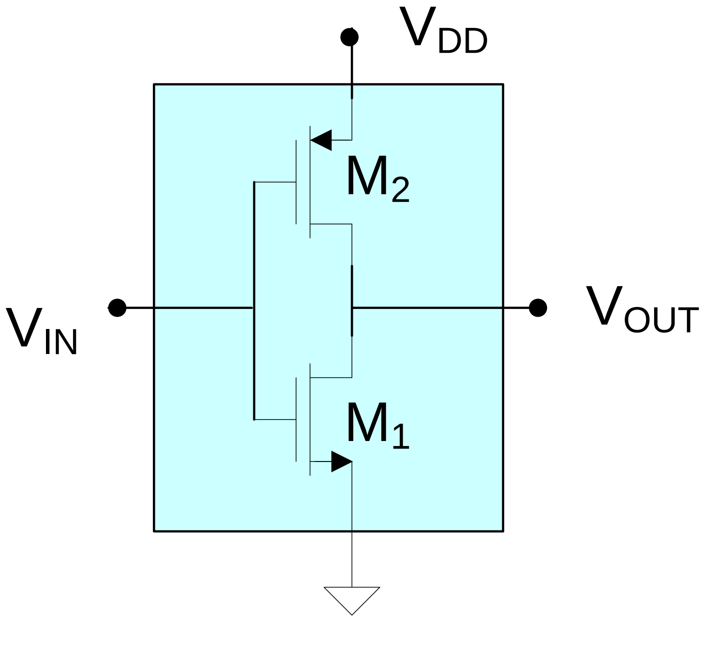
EE 330
Lecture 37

Digital Circuit Design

- Characterization of CMOS Inverter
- One device sizing strategy

Transfer characteristics of the static CMOS inverter

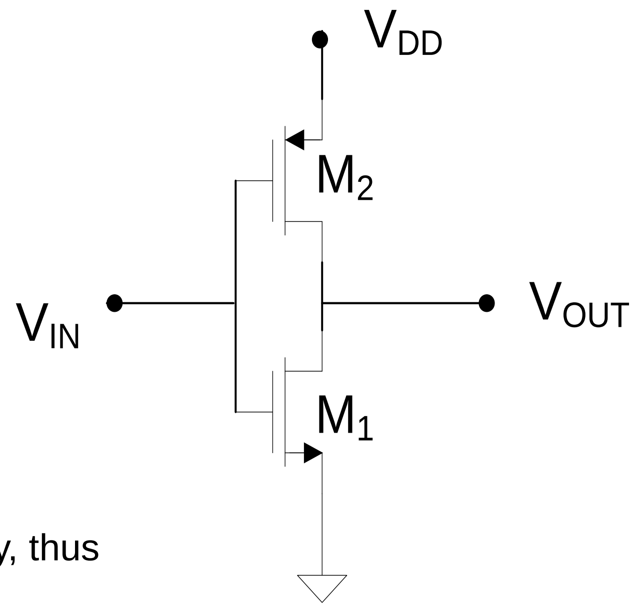




Transfer characteristics of the static CMOS inverter

(Neglect λ effects)

Case 1 Vin is so high that M_1 triode, M_2 cutoff



$$I_{D1} = \mu_n C_{OXn} \frac{W_1}{L_1}\left(V_{IN} - V_{Tn} - \frac{V_{OUT}}{2}\right)V_{OUT}$$

$$I_{D2} = 0$$

Equating I_{D1} and $-I_{D2}$ we obtain:

$$0 = \mu_n C_{OXn} \frac{W_1}{L_1}\left(V_{IN} - V_{Tn} - \frac{V_{OUT}}{2}\right)V_{OUT}$$

It can be shown that setting the first product term to 0 will not verify, thus

$$V_{OUT} = 0$$

valid for:

$$V_{GS1} \geq V_{Tn} \qquad V_{DS1} < V_{GS1} - V_{Tn} \qquad V_{GS2} \geq V_{Tp}$$

thus, valid for:

$$V_{IN} \geq V_{Tn} \qquad V_{OUT} < V_{IN} - V_{Tn} \qquad V_{IN} - V_{DD} \geq V_{Tp}$$

Graphical Interpretation of these conditions:

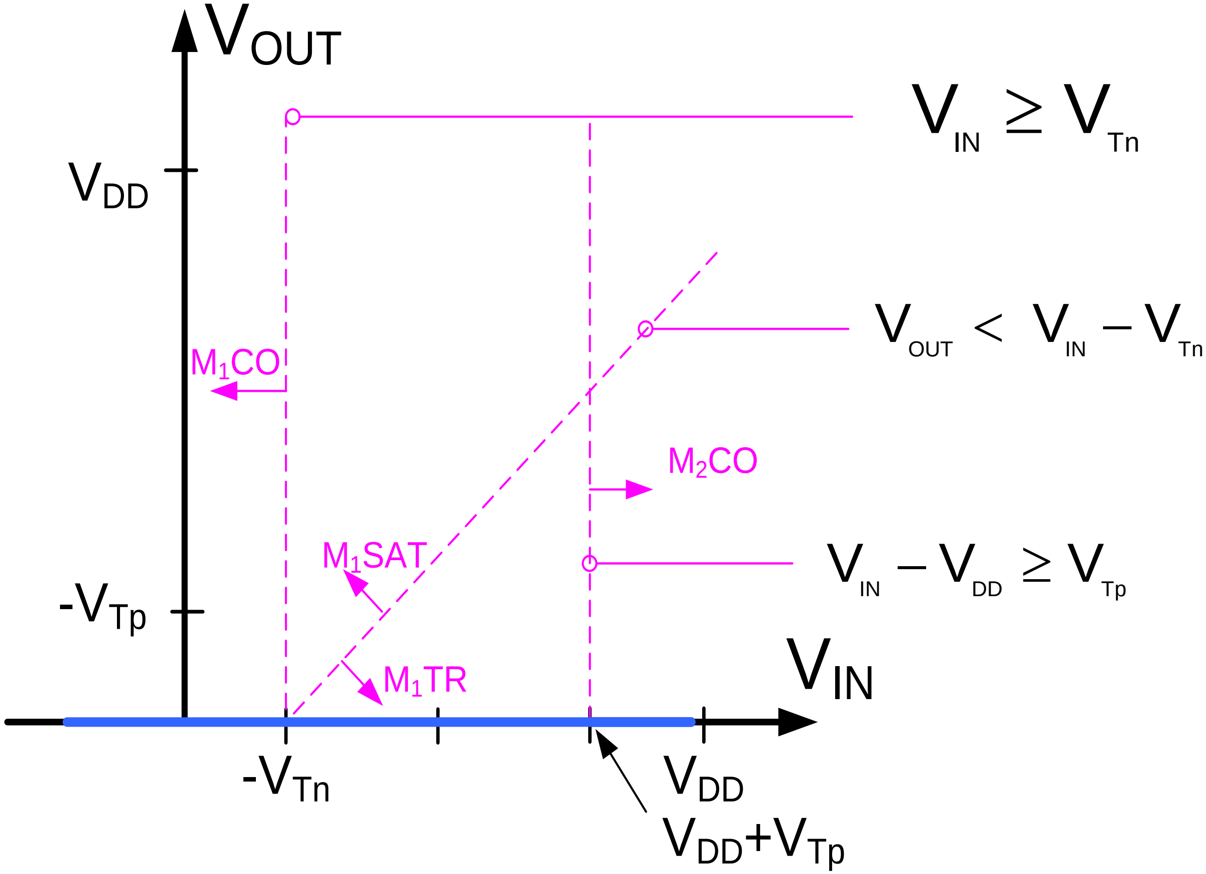
$V_{IN} \geq V_{Tn}$ $\quad$ $V_{OUT} < V_{IN} - V_{Tn}$ $\quad$ $V_{IN} - V_{DD} \geq V_{Tp}$

Transfer characteristics of the static CMOS inverter

(Neglect λ effects)

Case 1 M_1 triode, M_2 cutoff

$$V_{OUT} = 0$$

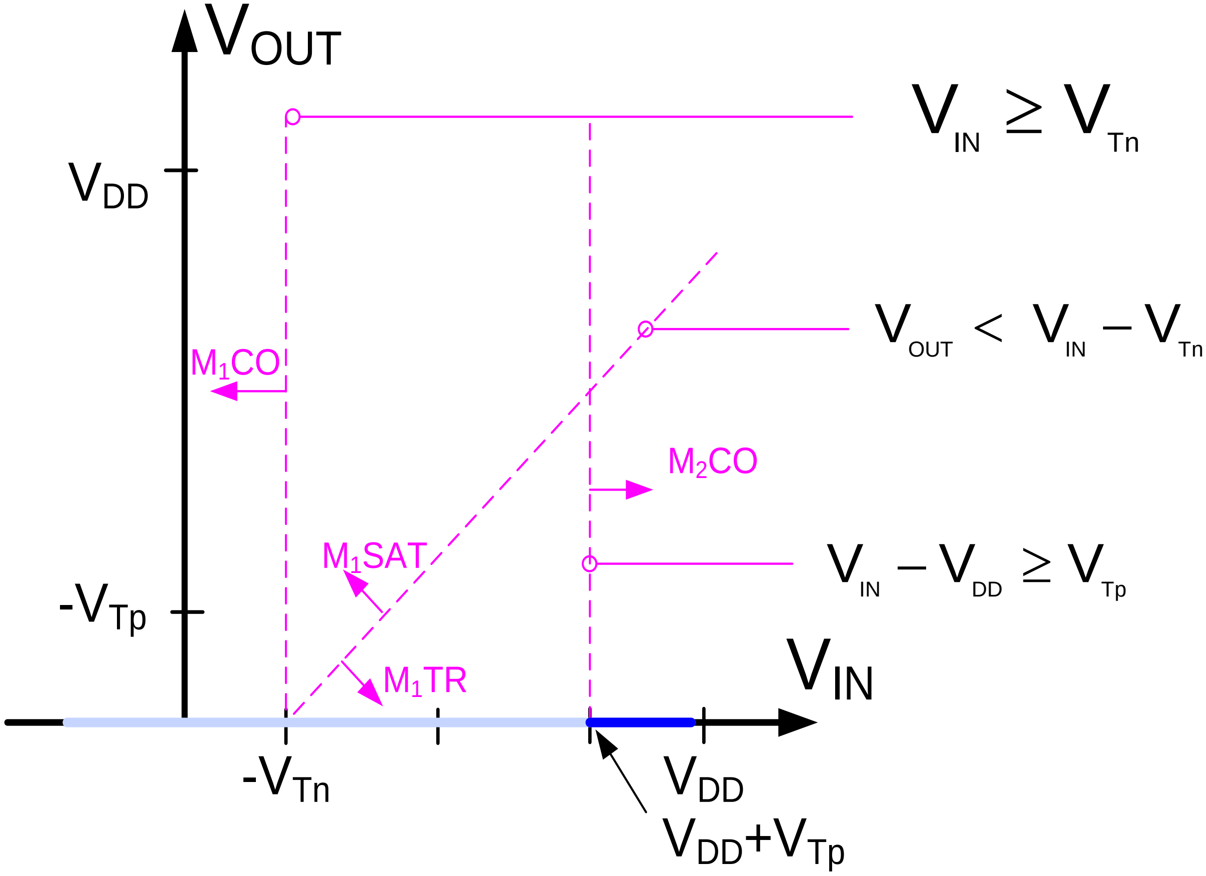


Transfer characteristics of the static CMOS inverter

(Neglect λ effects)

Case 1 M_1 triode, M_2 cutoff

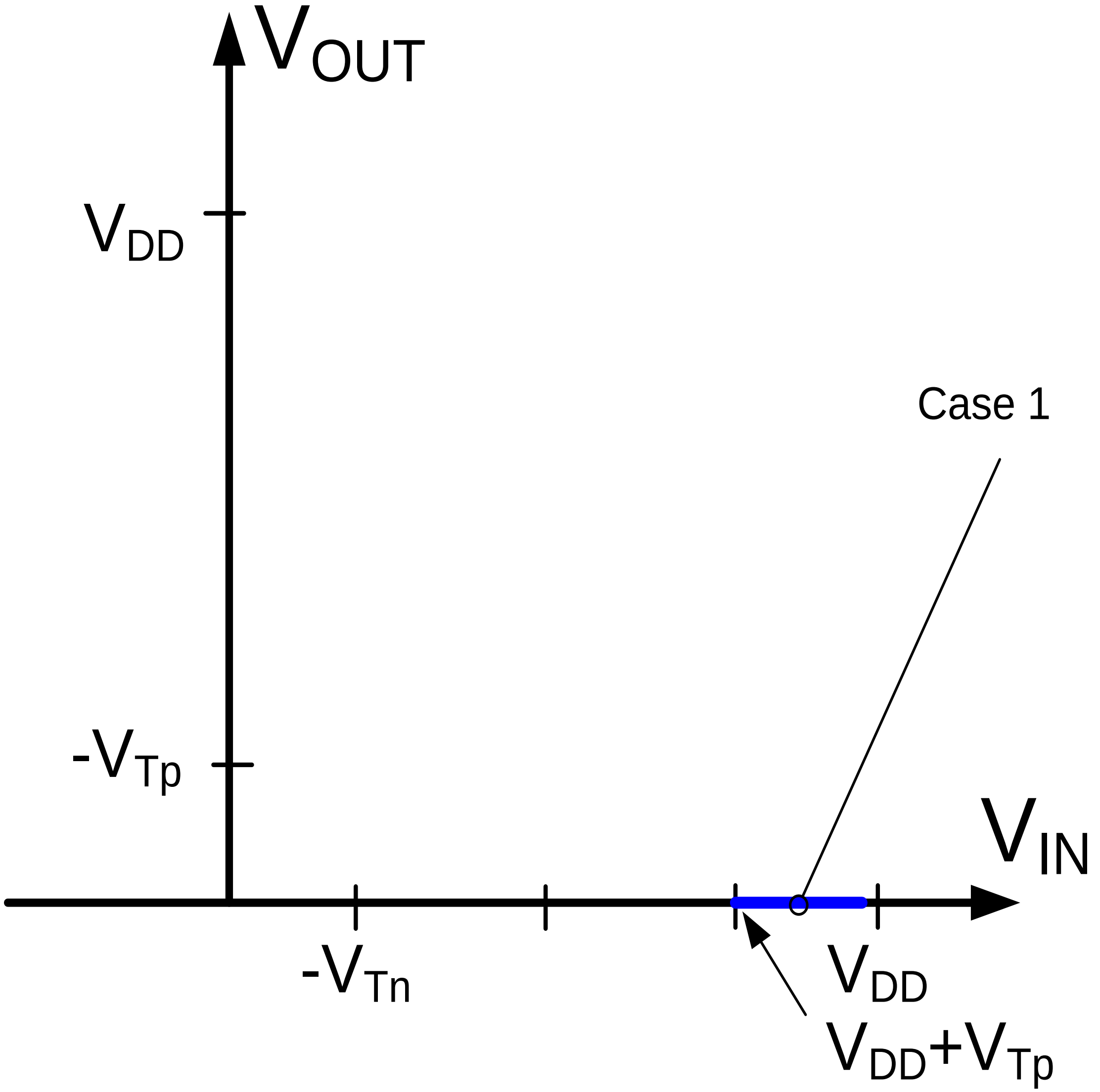
$$V_{OUT} = 0$$



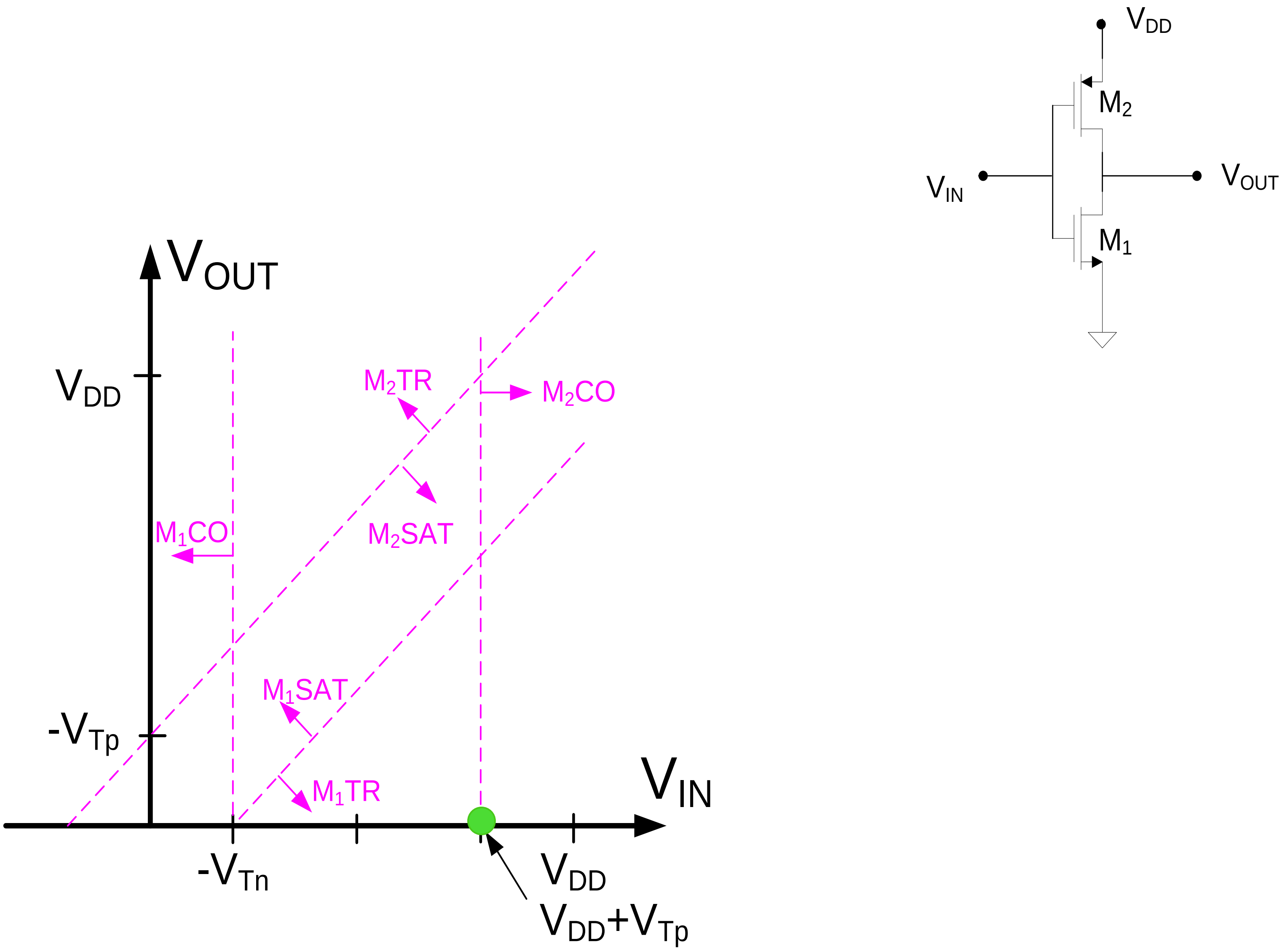
Transfer characteristics of the static CMOS inverter

(Neglect λ effects)

Partial solution:



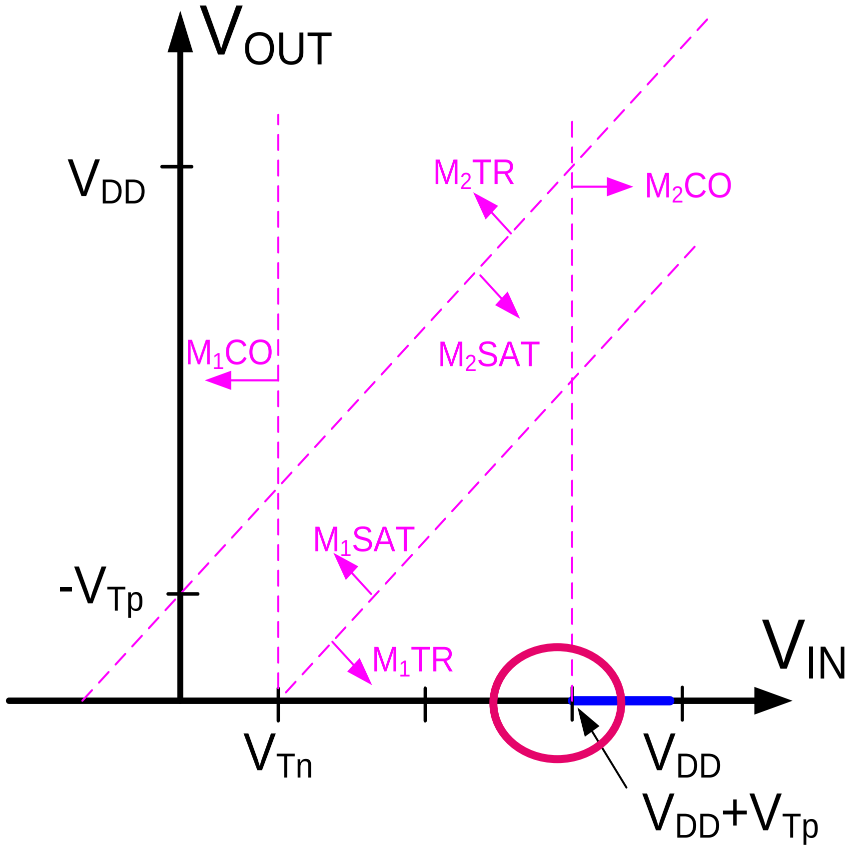
Regions of Operation for Devices in CMOS inverter



Transfer characteristics of the static CMOS inverter

(Neglect λ effects)

Case 2 M_1 triode, M_2 sat



M2: Square law ID

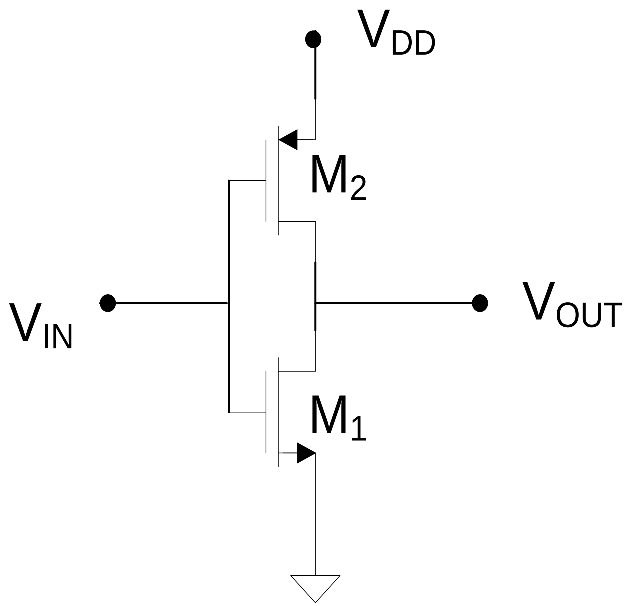
M1: like a resistor

➔: square law Vout

Transfer characteristics of the static CMOS inverter

(Neglect λ effects)

Case 2 M_1 triode, M_2 sat



$$I_{D1} = \mu_n C_{OXn} \frac{W_1}{L_1}\left(V_{IN} - V_{Tn} - \frac{V_{OUT}}{2}\right)V_{OUT}$$

$$I_{D2} = -\frac{\mu_p C_{OXp}}{2}\frac{W_2}{L_2}\left(V_{IN} - V_{DD} - V_{Tp}\right)^2$$

Equating I_{D1} and $-I_{D2}$ we obtain:

$$\frac{\mu_p C_{OXp}}{2}\frac{W_2}{L_2}\left(V_{IN} - V_{DD} - V_{Tp}\right)^2 = \mu_n C_{OXn} \frac{W_1}{L_1}\left(V_{IN} - V_{Tn} - \frac{V_{OUT}}{2}\right)V_{OUT}$$

valid for:

$$V_{GS1} \geq V_{Tn} \qquad V_{DS1} < V_{GS1} - V_{Tn} \qquad V_{GS2} \leq V_{Tp} \qquad V_{DS2} \leq V_{GS2} - V_{T2}$$

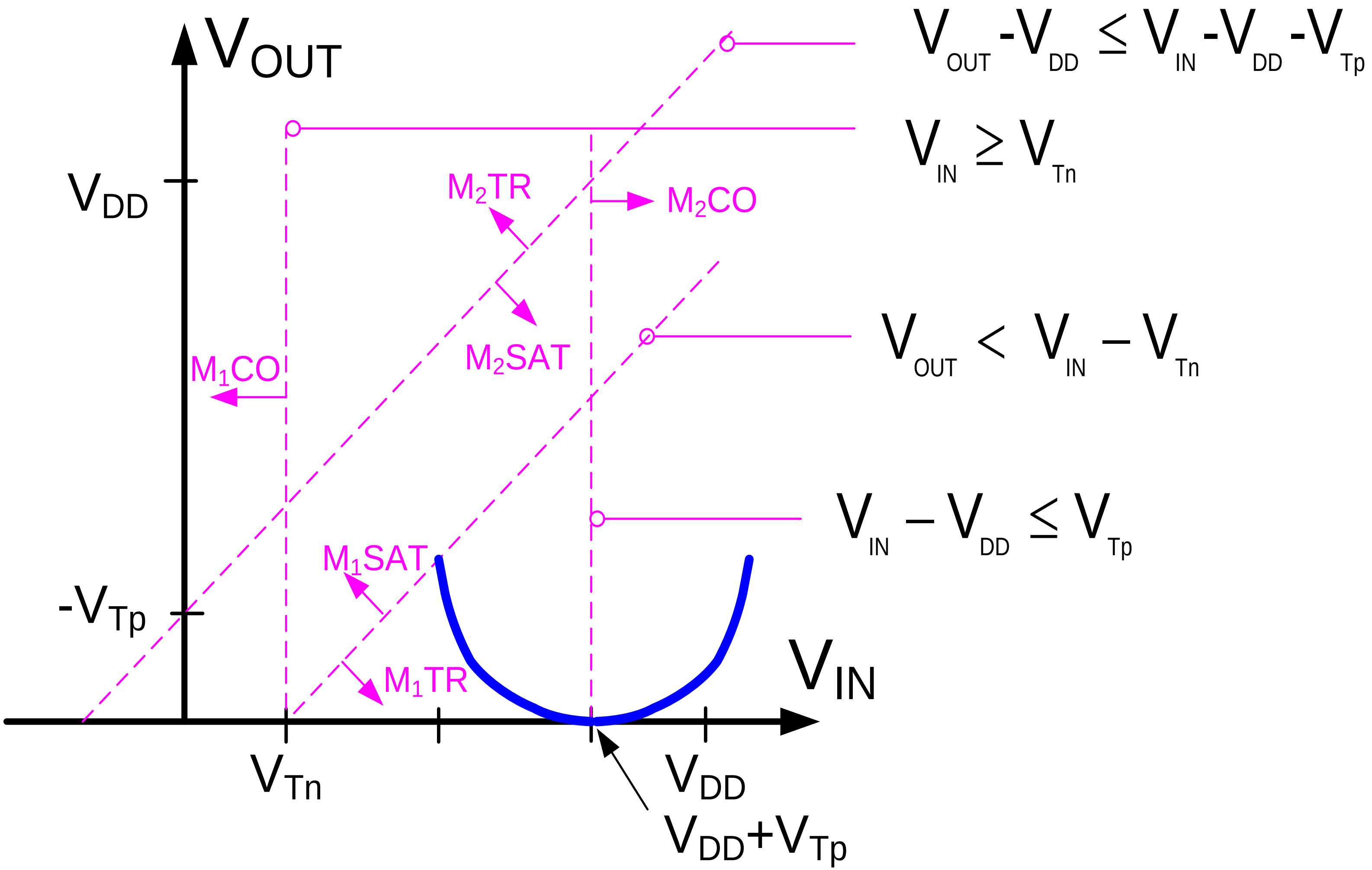
thus, valid for:

$$V_{IN} \geq V_{Tn} \qquad V_{OUT} < V_{IN} - V_{Tn} \qquad V_{IN} - V_{DD} \leq V_{Tp} \qquad V_{OUT} - V_{DD} \leq V_{IN} - V_{DD} - V_{Tp}$$

Transfer characteristics of the static CMOS inverter

(Neglect λ effects)

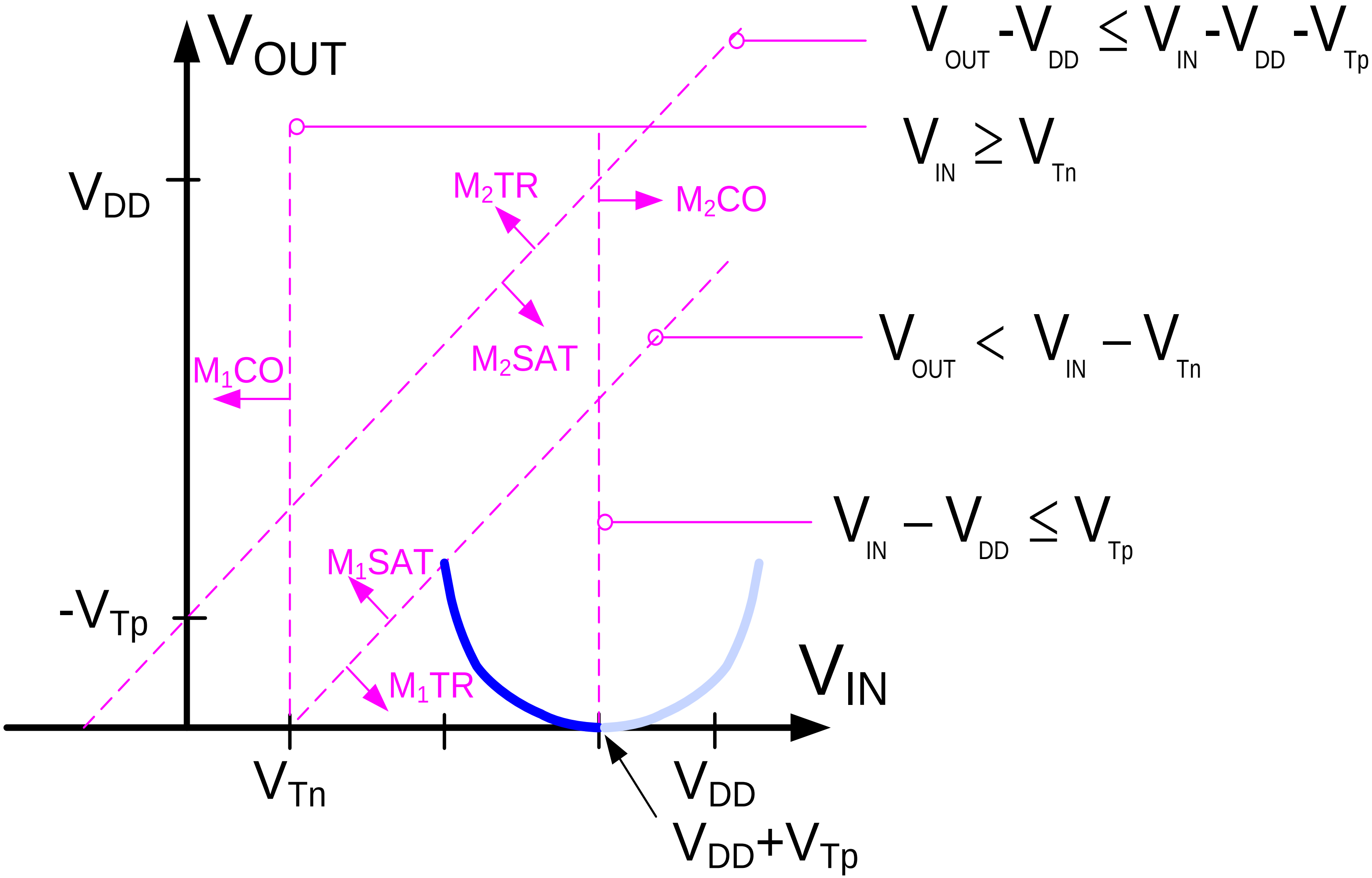
Case 2 M_1 triode, M_2 sat



Transfer characteristics of the static CMOS inverter

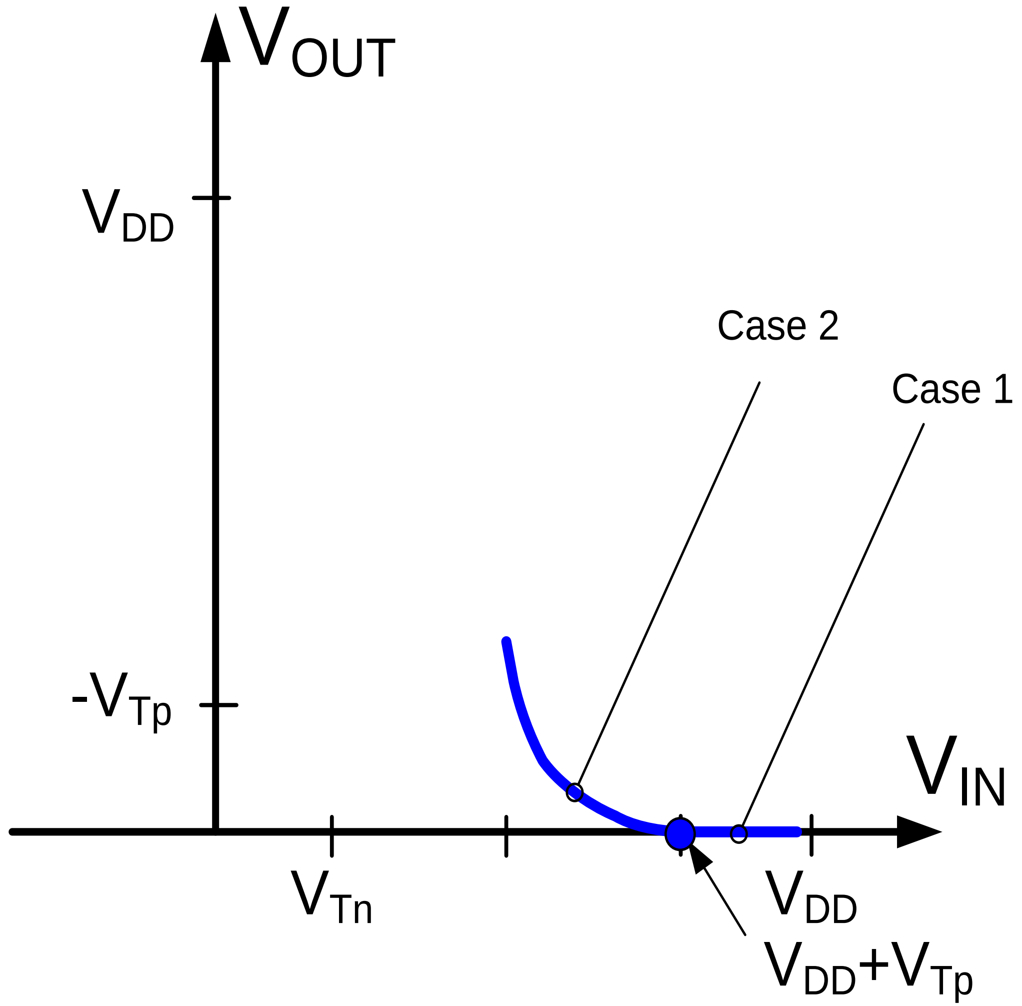
(Neglect λ effects)

Case 2 M_1 triode, M_2 sat



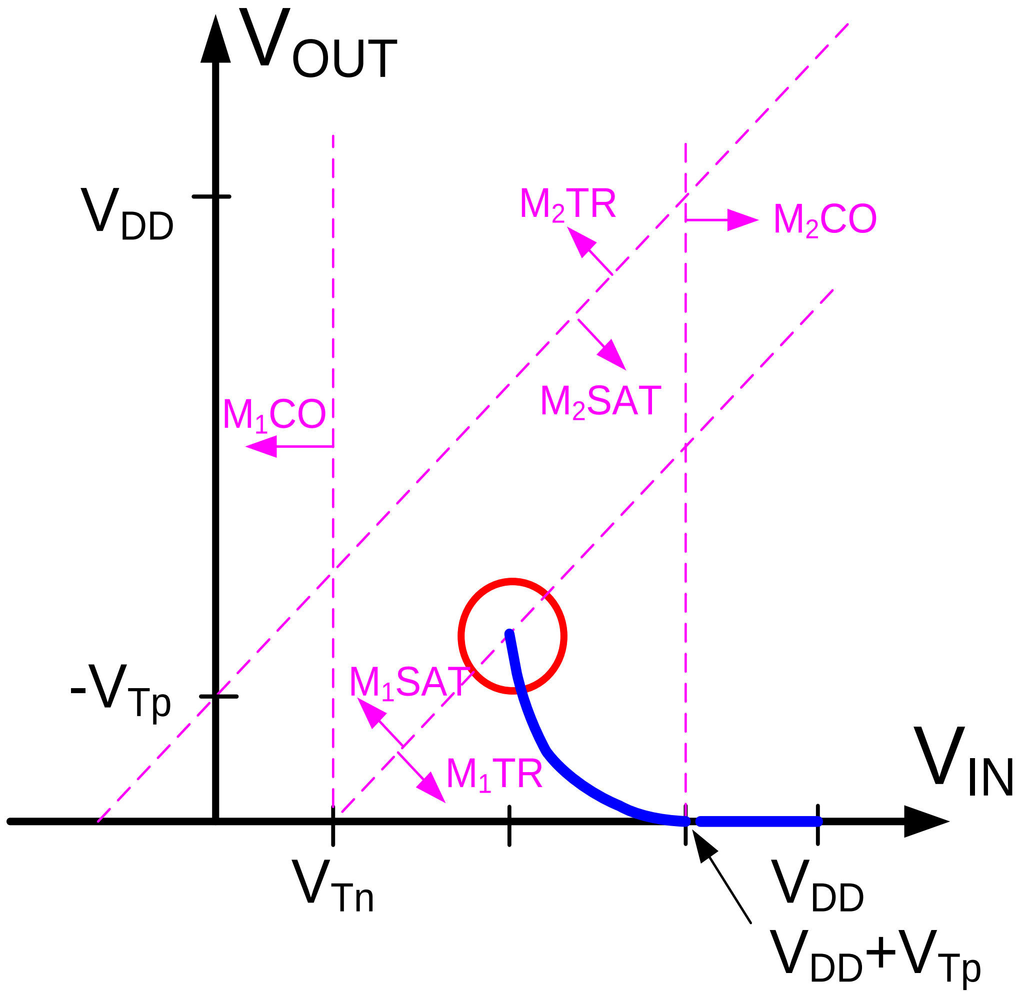
Transfer characteristics of the static CMOS inverter

Partial solution:



Transfer characteristics of the static CMOS inverter
(Neglect λ effects)

Case 3 M_1 sat, M_2 sat



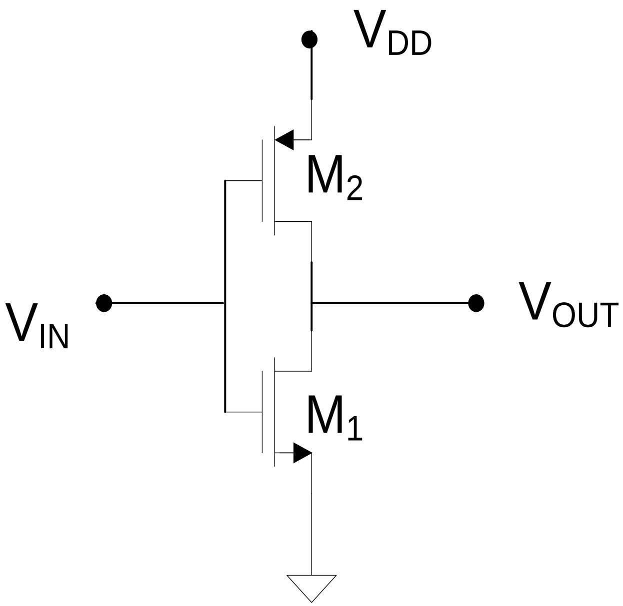
Transfer characteristics of the static CMOS inverter

(Neglect λ effects)

Case 3 M_1 sat, M_2 sat

$$I_{D1} = \frac{\mu_n C_{OXn}}{2}\frac{W_1}{L_1}\left(V_{IN} - V_{Tn}\right)^2$$

$$I_{D2} = \frac{\mu_p C_{OXp}}{2}\frac{W_2}{L_2}\left(V_{IN} - V_{DD} - V_{Tp}\right)^2$$



Equating I_{D1} and $-I_{D2}$ we obtain:

$$\frac{\mu_p C_{OXp}}{2}\frac{W_2}{L_2}\left(V_{IN} - V_{DD} - V_{Tp}\right)^2 = \frac{\mu_n C_{OXn}}{2}\frac{W_1}{L_1}\left(V_{IN} - V_{Tn}\right)^2$$

Which can be rewritten as:

$$\sqrt{\frac{\mu_p C_{OXp}}{2}\frac{W_2}{L_2}}\left(V_{DD} + V_{Tp} - V_{IN}\right) = \sqrt{\frac{\mu_n C_{OXn}}{2}\frac{W_1}{L_1}}\left(V_{IN} - V_{Tn}\right)$$

Which can be simplified to:

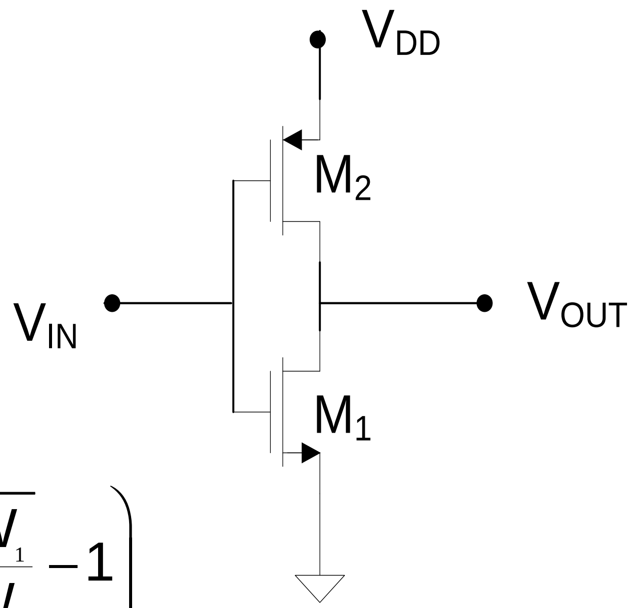
$$V_{IN} = \frac{\left(V_{Tn}\right)\sqrt{\frac{\mu_n C_{OXn}}{2}\frac{W_1}{L_1}} + \left(V_{DD} + V_{Tp}\right)\sqrt{\frac{\mu_p C_{OXp}}{2}\frac{W_2}{L_2}}}{\sqrt{\frac{\mu_n C_{OXn}}{2}\frac{W_1}{L_1}} + \sqrt{\frac{\mu_p C_{OXp}}{2}\frac{W_2}{L_2}}}$$

This is a vertical line

Transfer characteristics of the static CMOS inverter

(Neglect λ effects)

Case 3 M_1 sat, M_2 sat



$$V_{IN} = \frac{(V_{Tn})\sqrt{\frac{\mu_n C_{OXn}}{2}\frac{W_1}{L_1}} + (V_{DD}+V_{Tp})\sqrt{\frac{\mu_p C_{OXp}}{2}\frac{W_2}{L_2}}}{\sqrt{\frac{\mu_n C_{OXn}}{2}\frac{W_1}{L_1}} + \sqrt{\frac{\mu_p C_{OXp}}{2}\frac{W_2}{L_2}}}$$

If $C_{OXn} \cong C_{OXp} = C_{OX}$, $V_{TP} = -V_{TN}$ this can be simplified to:

$$V_{IN} = \frac{V_{DD}}{1+\sqrt{\frac{\mu_n}{\mu_p}\frac{W_1}{W_2}}} + \frac{V_T\left(\sqrt{\frac{\mu_n}{\mu_p}\frac{W_1}{W_2}}-1\right)}{1+\sqrt{\frac{\mu_n}{\mu_p}\frac{W_1}{W_2}}}$$

valid for:

$$V_{GS1} \geq V_{Tn} \qquad V_{DS1} \geq V_{GS1} - V_{Tn} \qquad V_{GS2} \leq V_{Tp} \qquad V_{DS2} \leq V_{GS2} - V_{T2}$$

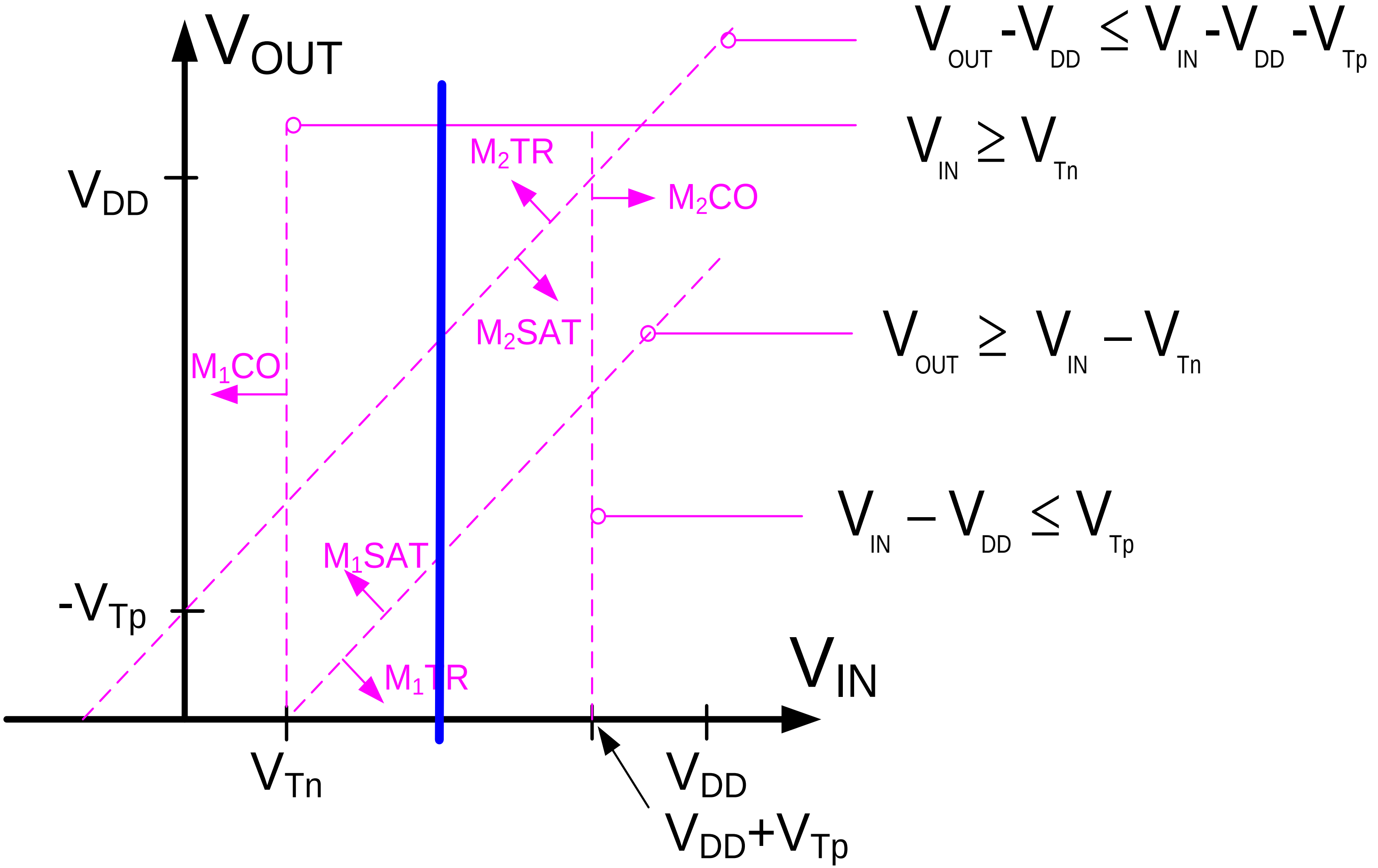
thus, valid for:

$$V_{IN} \geq V_{Tn} \qquad V_{OUT} \geq V_{IN} - V_{Tn} \qquad V_{IN} - V_{DD} \leq V_{Tp} \qquad V_{OUT} - V_{DD} \leq V_{IN} - V_{DD} - V_{Tp}$$

Transfer characteristics of the static CMOS inverter

(Neglect λ effects)

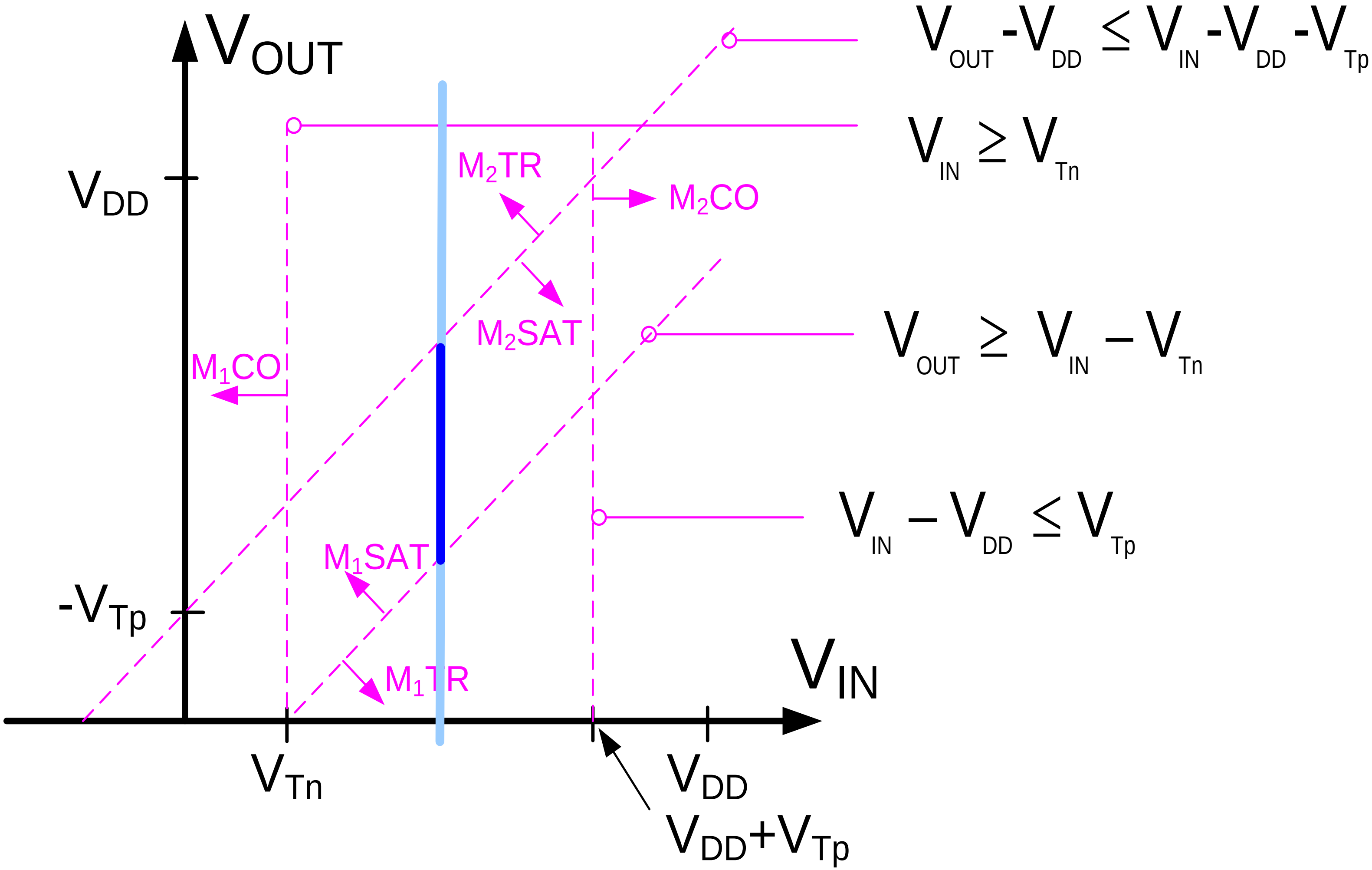
Case 3 M_1 sat, M_2 sat



Transfer characteristics of the static CMOS inverter

(Neglect λ effects)

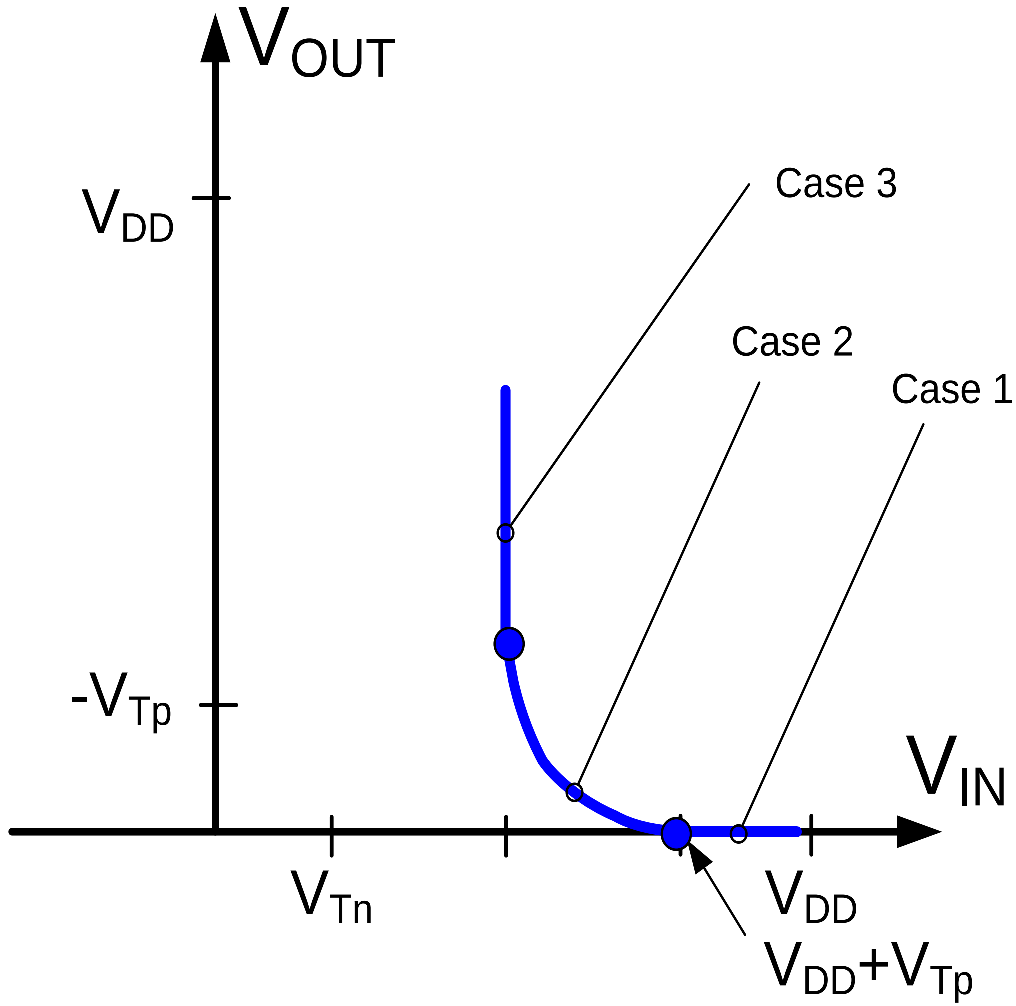
Case 3 M_1 sat, M_2 sat



Transfer characteristics of the static CMOS inverter

(Neglect λ effects)

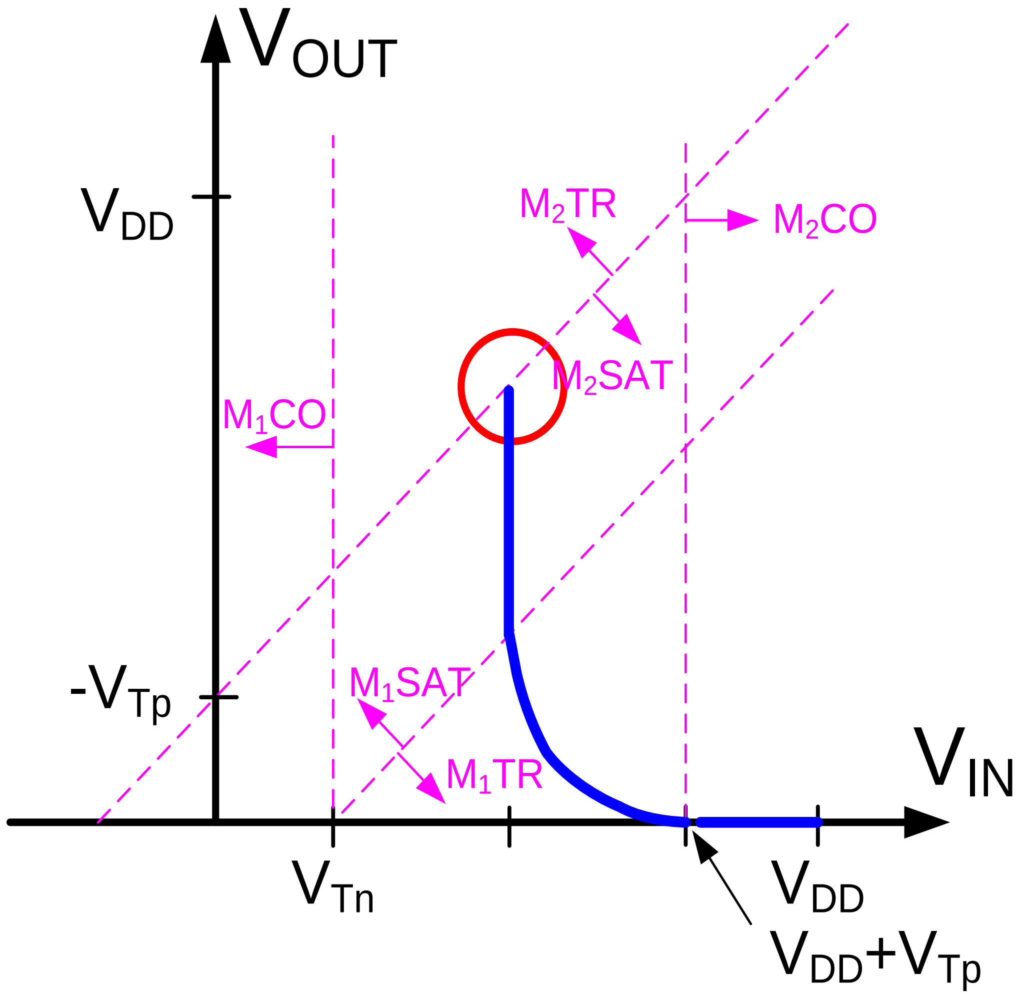
Partial solution:



Transfer characteristics of the static CMOS inverter

(Neglect λ effects)

Case 4 M_1 sat, M_2 triode



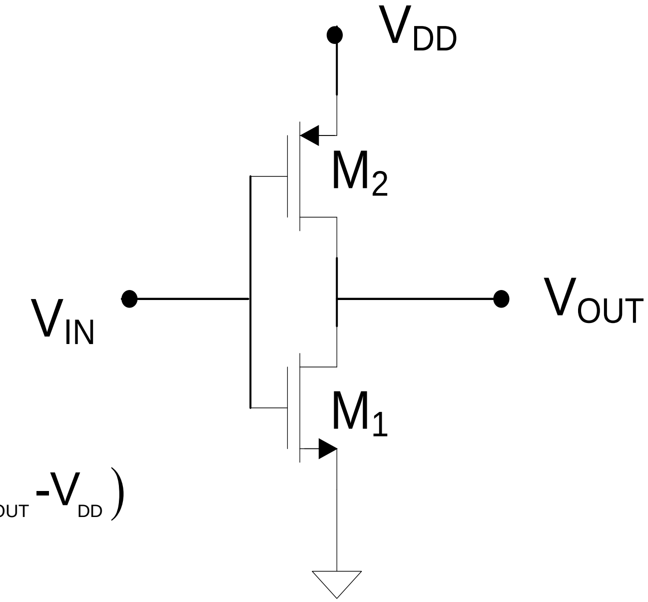
Transfer characteristics of the static CMOS inverter

(Neglect λ effects)

Case 4 M_1 sat, M_2 triode

$$I_{D1} = \frac{\mu_n C_{OXn}}{2}\frac{W_1}{L_1}\left(V_{IN} - V_{Tn}\right)^2$$

$$I_{D2} = -\mu_p C_{OXp}\frac{W_2}{L_2}\left(V_{IN} - V_{DD} - V_{Tp} - \frac{V_{OUT}\text{-}V_{DD}}{2}\right)\bullet\left(V_{OUT}\text{-}V_{DD}\right)$$



Equating I_{D1} and $-I_{D2}$ we obtain:

$$\frac{\mu_n C_{OXn}}{2}\frac{W_1}{L_1}\left(V_{IN} - V_{Tn}\right)^2 = \mu_p C_{OXp}\frac{W_2}{L_2}\left(V_{IN} - V_{DD} - V_{Tp} - \frac{V_{OUT}\text{-}V_{DD}}{2}\right)\bullet\left(V_{OUT}\text{-}V_{DD}\right)$$

valid for:

$$V_{GS1} \geq V_{Tn} \qquad V_{DS1} \geq V_{GS1} - V_{Tn} \qquad V_{GS2} \leq V_{Tp} \qquad V_{DS2} > V_{GS2}\text{-}V_{T2}$$

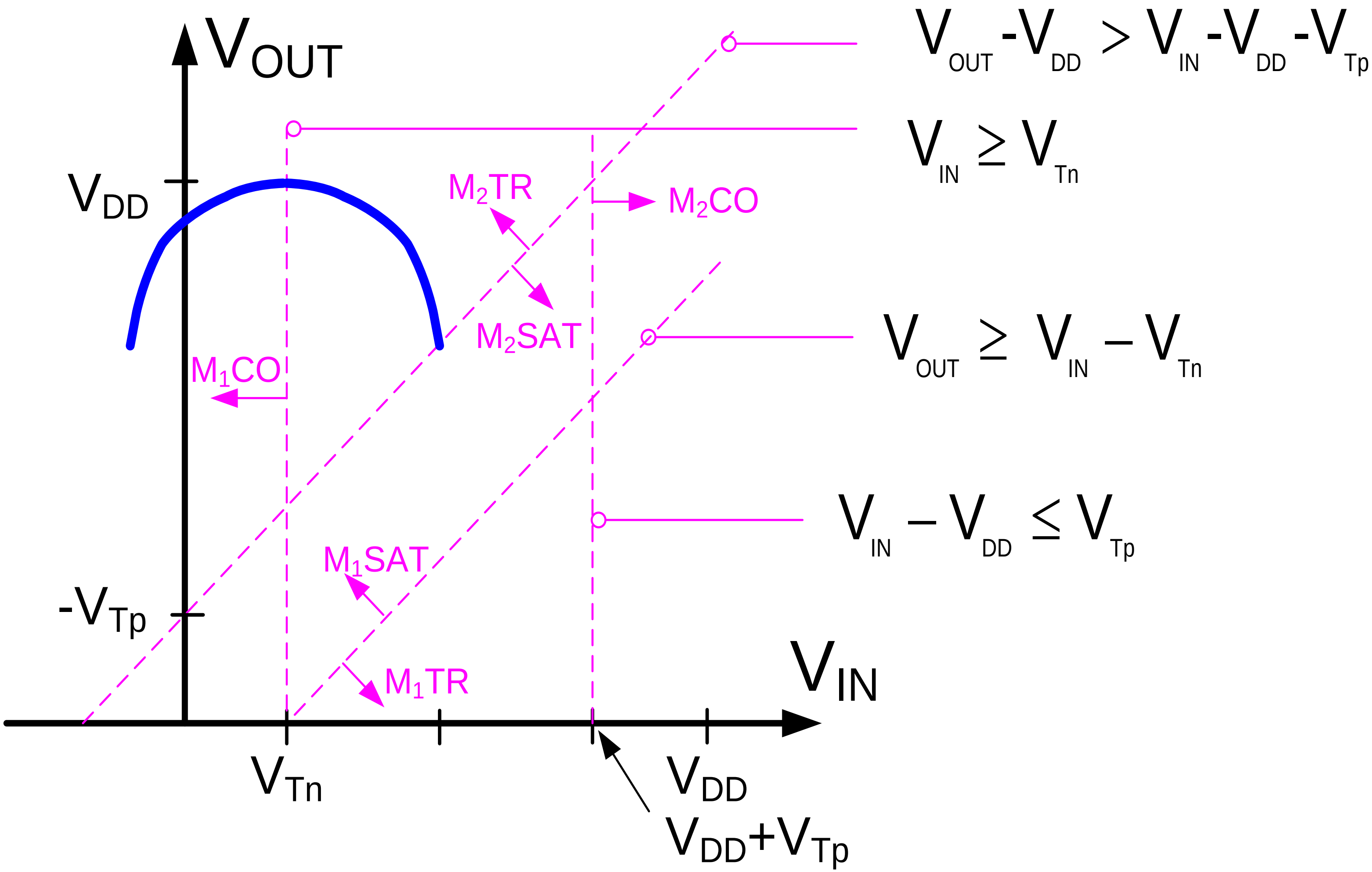
thus, valid for:

$$V_{IN} \geq V_{Tn} \qquad V_{OUT} \geq V_{IN} - V_{Tn} \qquad V_{IN} - V_{DD} \leq V_{Tp} \qquad V_{OUT}\text{-}V_{DD} > V_{IN}\text{-}V_{DD}\text{-}V_{Tp}$$

Transfer characteristics of the static CMOS inverter

(Neglect λ effects)

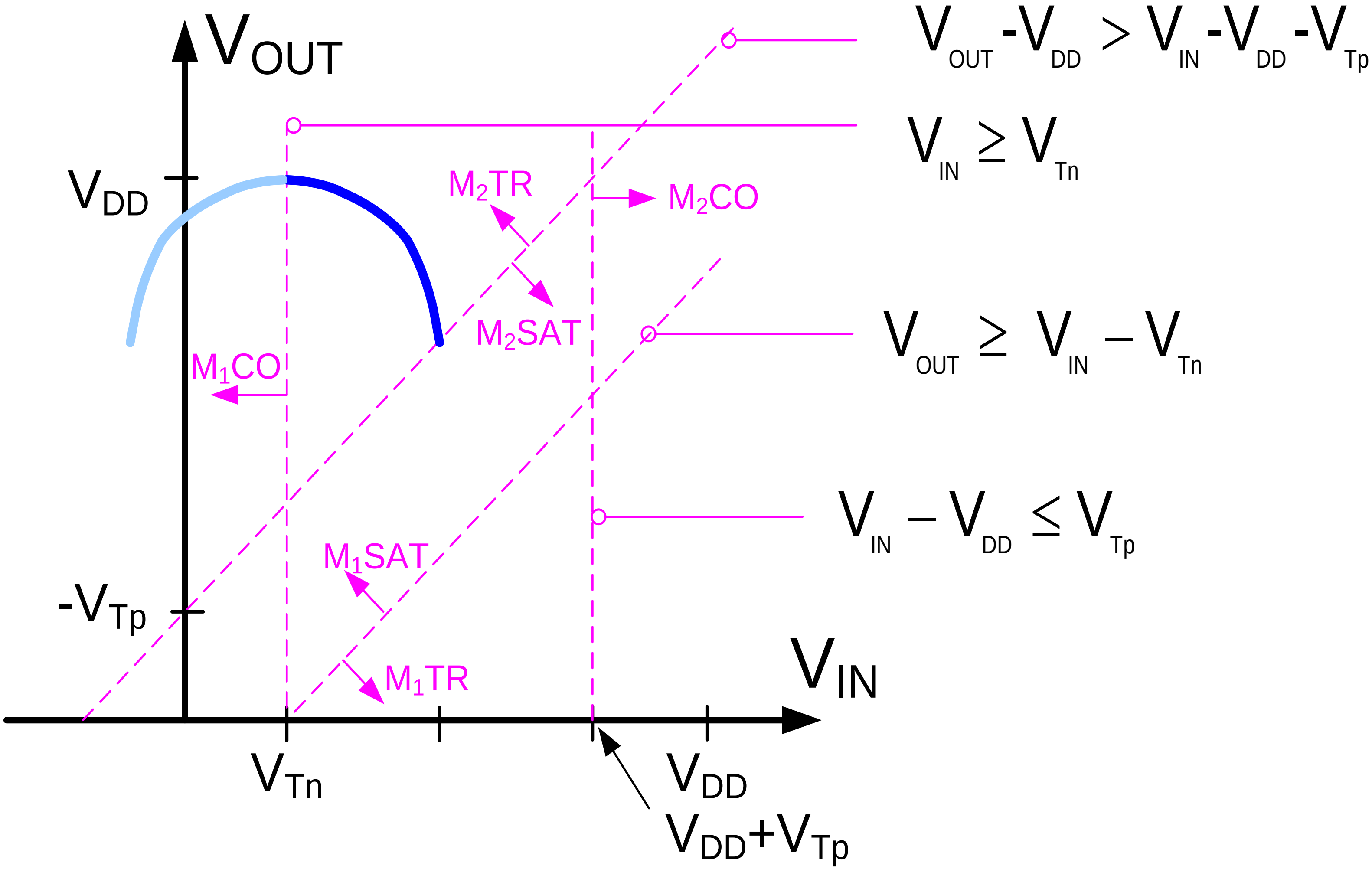
Case 4 M_1 sat, M_2 triode



Transfer characteristics of the static CMOS inverter

(Neglect λ effects)

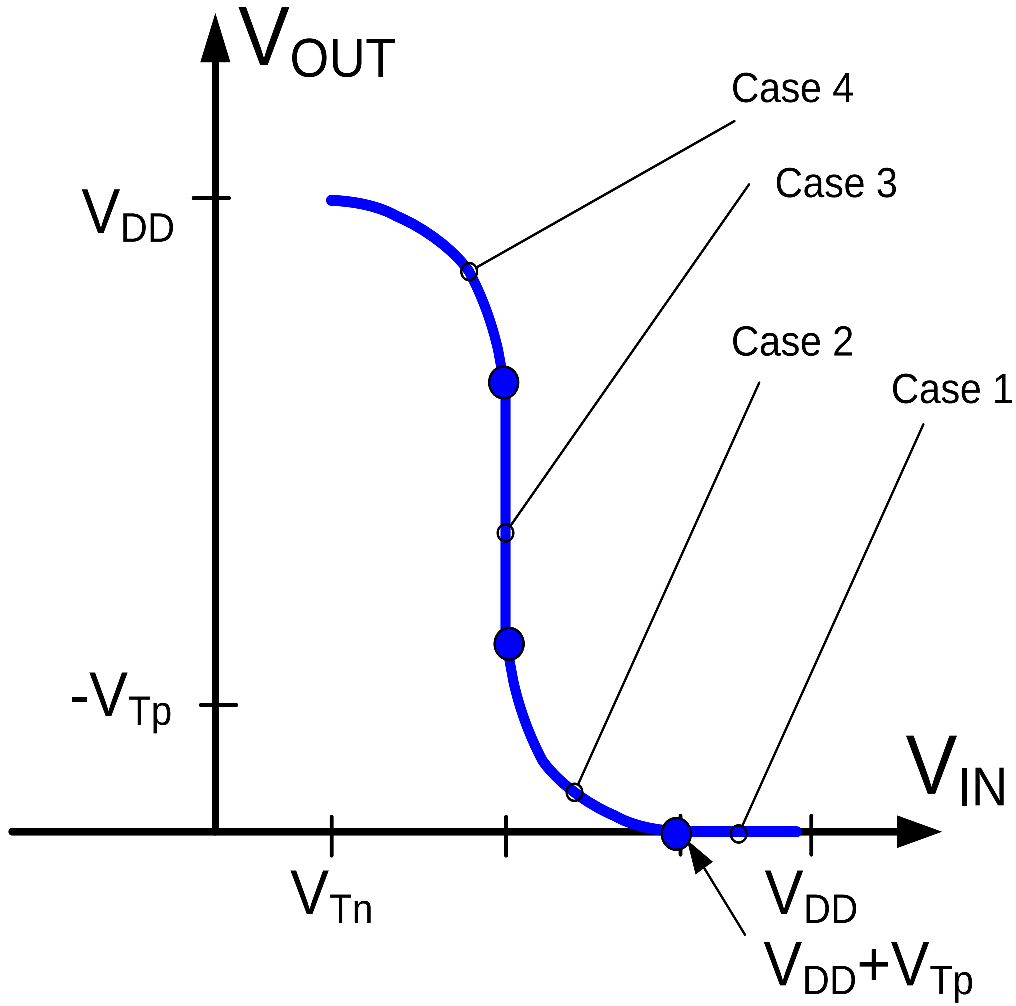
Case 4 M_1 sat, M_2 triode



Transfer characteristics of the static CMOS inverter

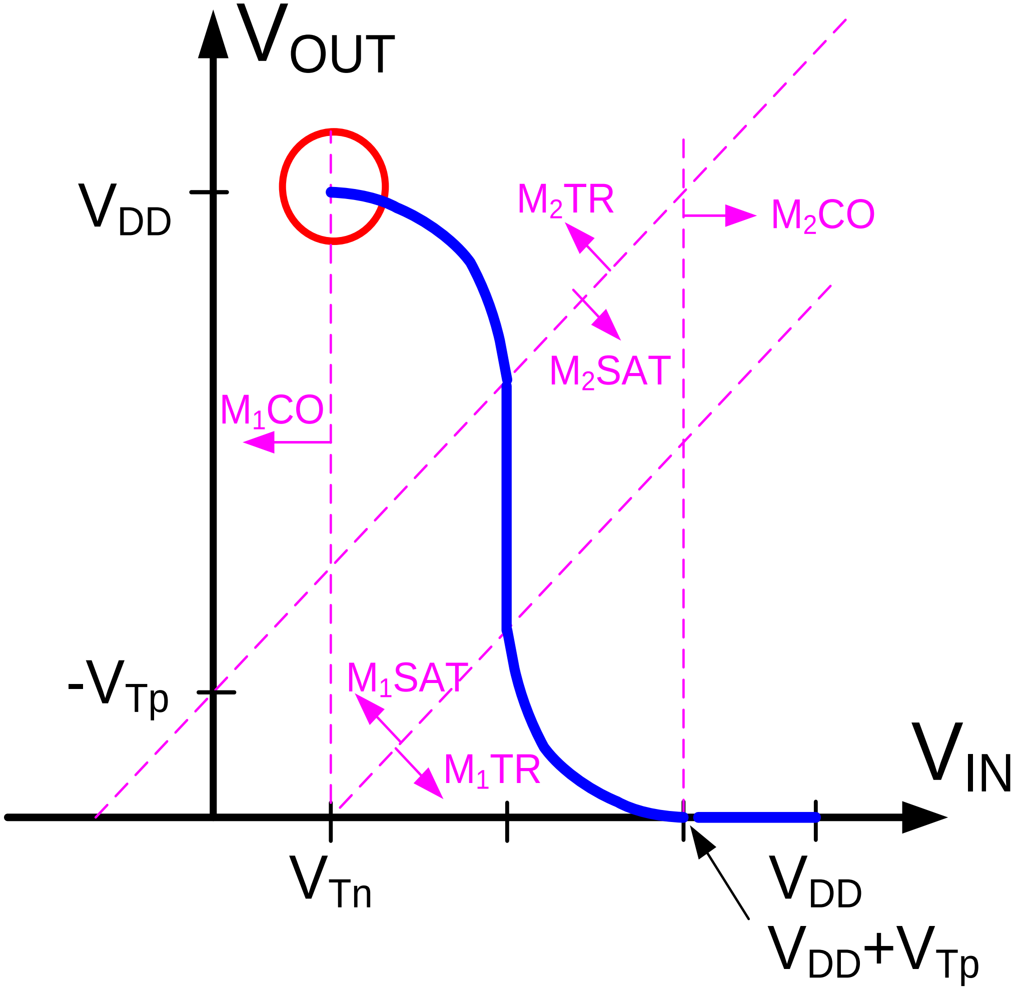
(Neglect λ effects)

Partial solution:



Transfer characteristics of the static CMOS inverter
(Neglect λ effects)

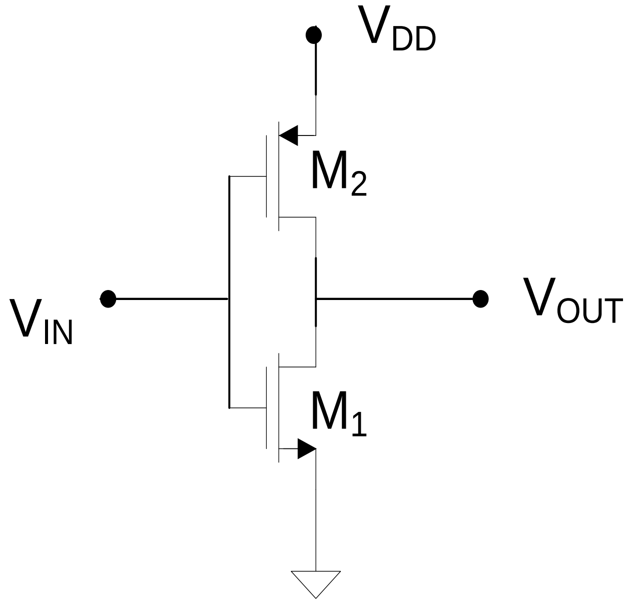
Case 4 M_1 cutoff, M_2 triode



Transfer characteristics of the static CMOS inverter

(Neglect λ effects)

Case 5 M_1 cutoff, M_2 triode



$$I_{D1} = 0$$

$$I_{D2} = -\mu_p C_{OXp} \frac{W_2}{L_2}\left(V_{IN} - V_{DD} - V_{Tp} - \frac{V_{OUT}\text{-}V_{DD}}{2}\right) \bullet \left(V_{OUT}\text{-}V_{DD}\right)$$

Equating I_{D1} and $-I_{D2}$ we obtain:

$$\mu_p C_{OXp} \frac{W_2}{L_2}\left(V_{IN} - V_{DD} - V_{Tp} - \frac{V_{OUT}\text{-}V_{DD}}{2}\right) \bullet \left(V_{OUT}\text{-}V_{DD}\right) = 0$$

valid for:

$$V_{GS1} < V_{Tn} \qquad V_{GS2} \le V_{Tp} \qquad V_{DS2} > V_{GS2}\text{-}V_{T2}$$

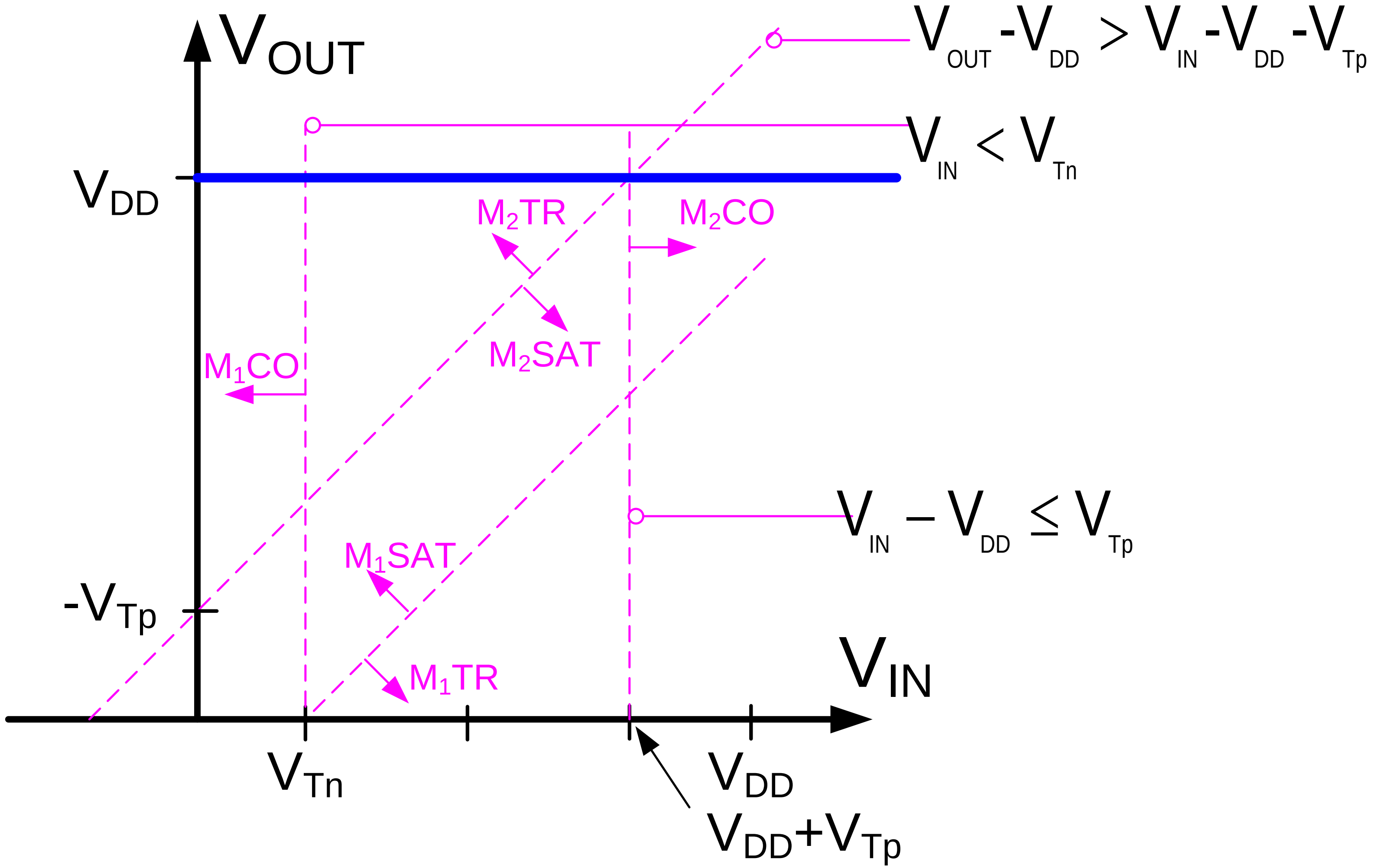
thus, valid for:

$$V_{IN} < V_{Tn} \qquad V_{IN} - V_{DD} \le V_{Tp} \qquad V_{OUT}\text{-}V_{DD} > V_{IN}\text{-}V_{DD}\text{-}V_{Tp}$$

Transfer characteristics of the static CMOS inverter

(Neglect λ effects)

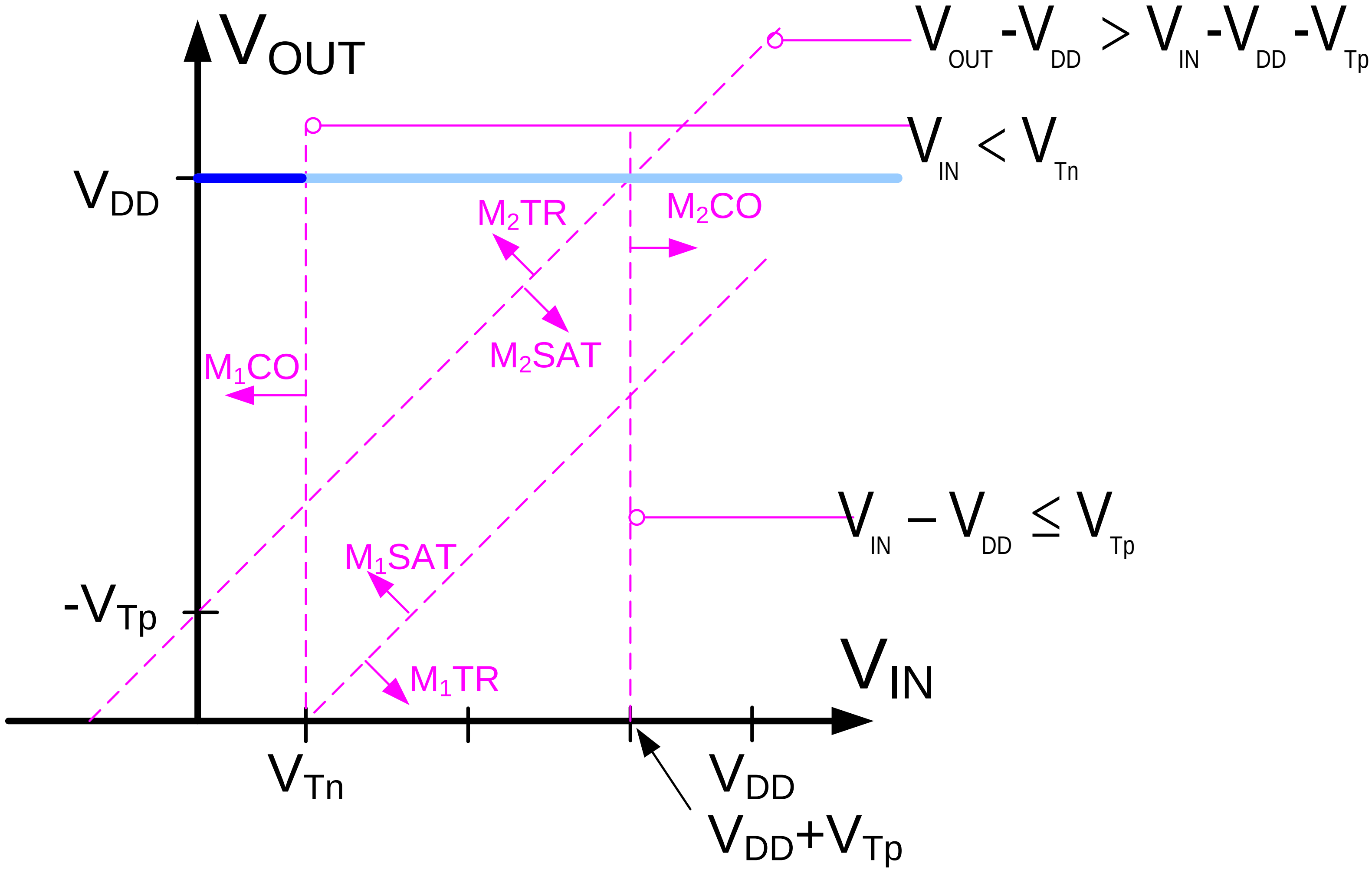
Case 5 M_1 cutoff, M_2 triode



Transfer characteristics of the static CMOS inverter

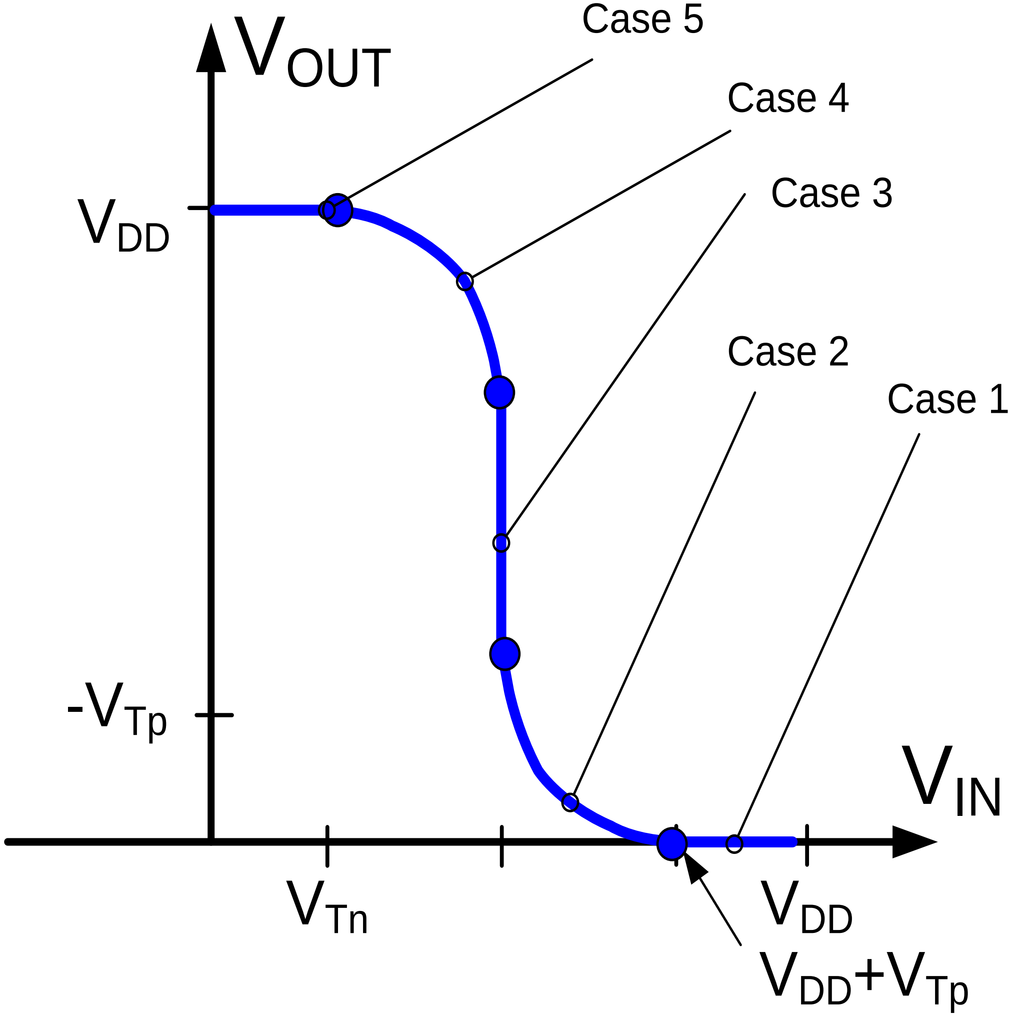
(Neglect λ effects)

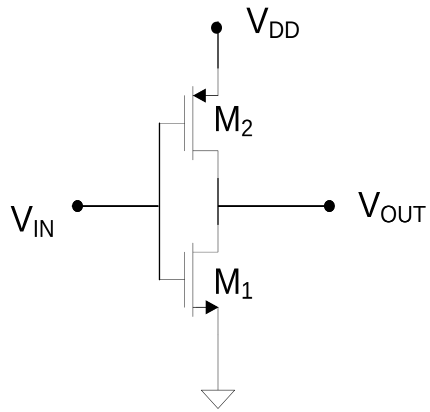
Case 5 M_1 cutoff, M_2 triode



Transfer characteristics of the static CMOS inverter

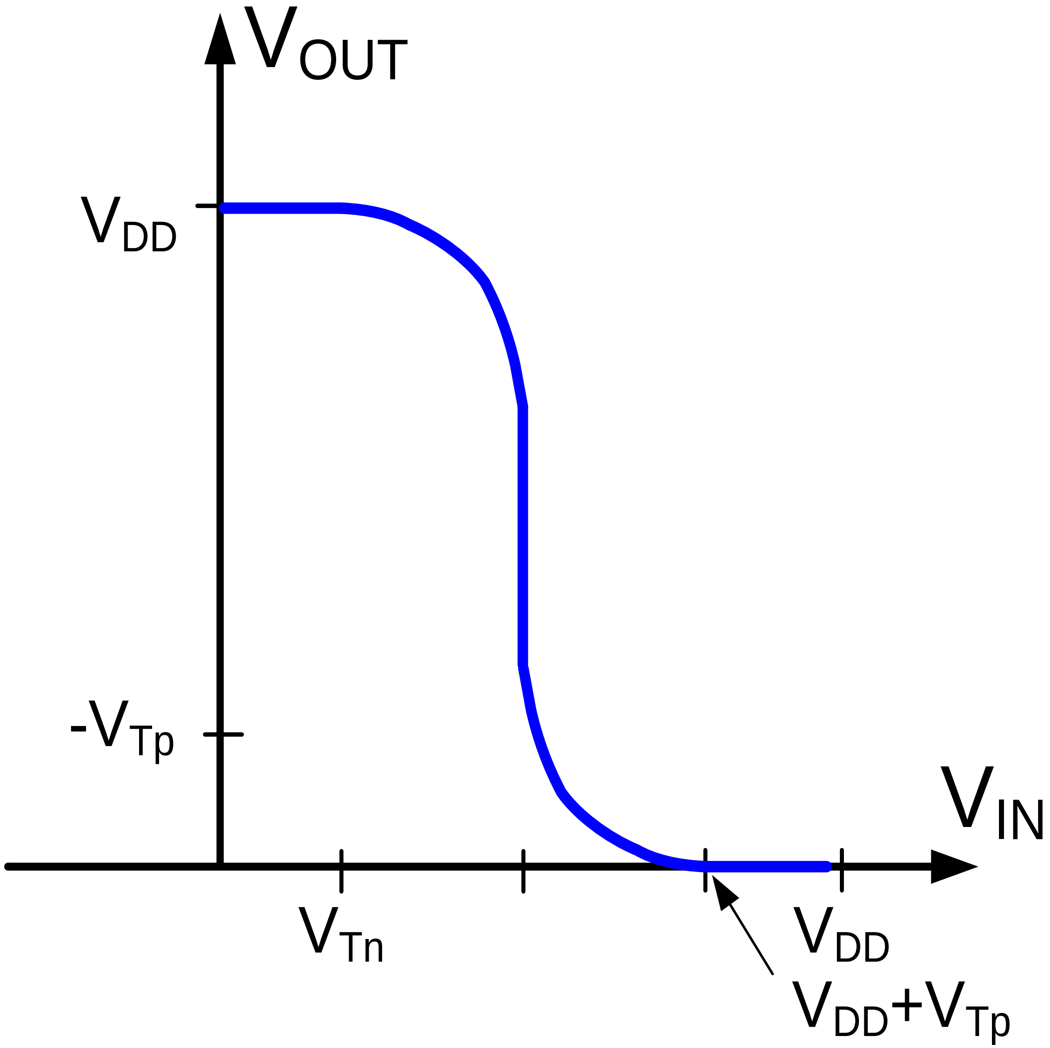
(Neglect λ effects)





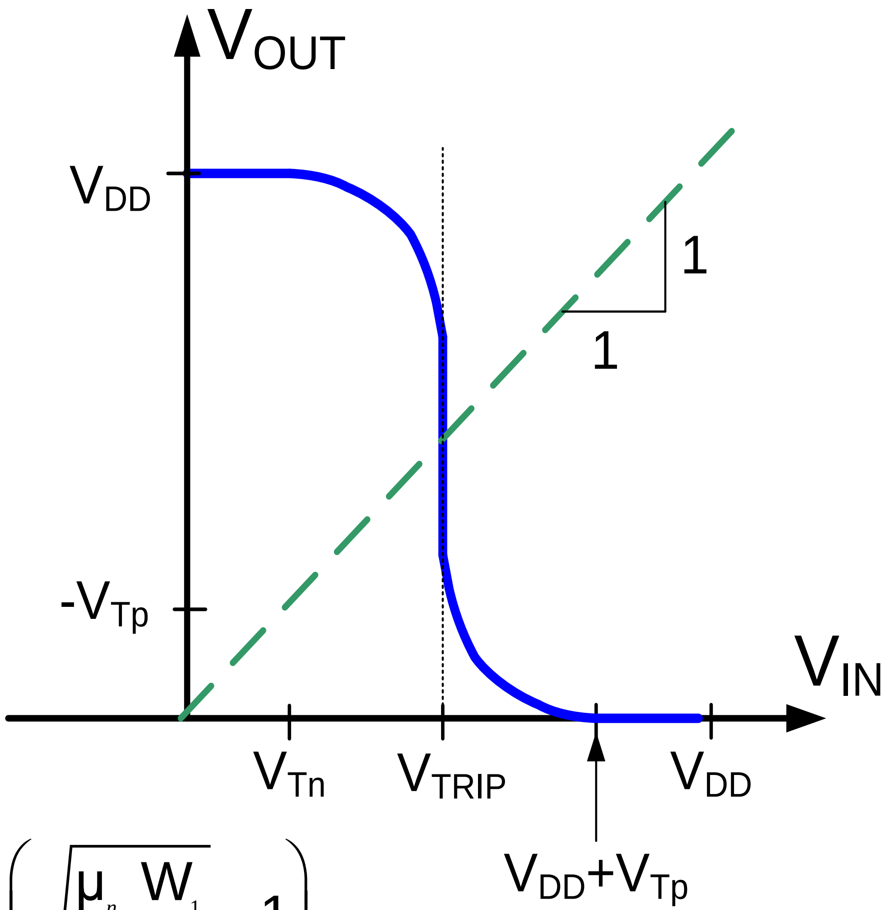
Transfer characteristics of the static CMOS inverter

(Neglect λ effects)



Transfer characteristics of the static CMOS inverter

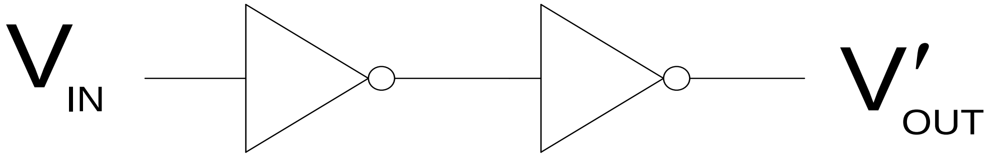
(Neglect λ effects)



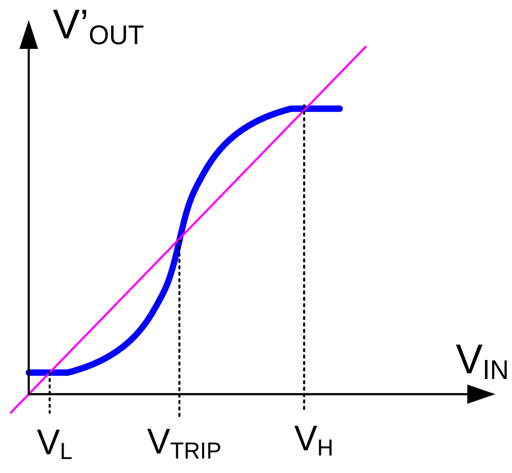
From Case 3 analysis:

$$V_{OUT}=V_{IN}=V_{TRIP}=\frac{V_{DD}}{1+\sqrt{\frac{\mu_n}{\mu_p}\frac{W_1}{W_2}}}+\frac{V_T\left(\sqrt{\frac{\mu_n}{\mu_p}\frac{W_1}{W_2}}-1\right)}{1+\sqrt{\frac{\mu_n}{\mu_p}\frac{W_1}{W_2}}}$$

Inverter Transfer Characteristics of Inverter Pair

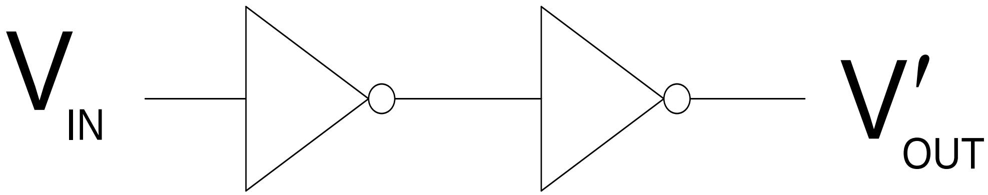


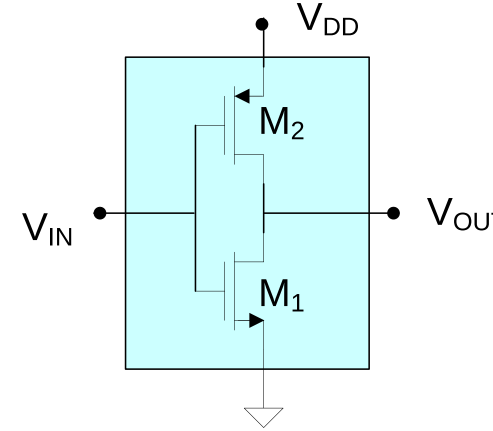
What are V_H and V_L?

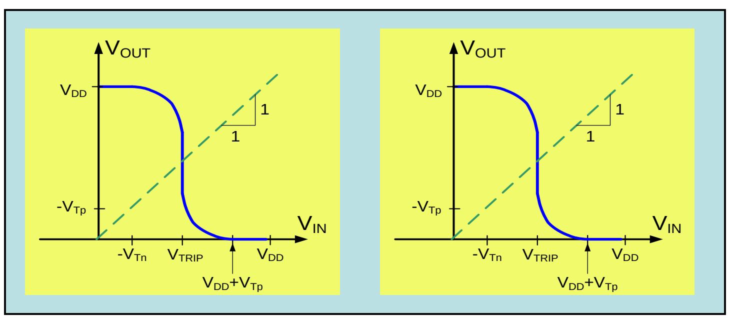


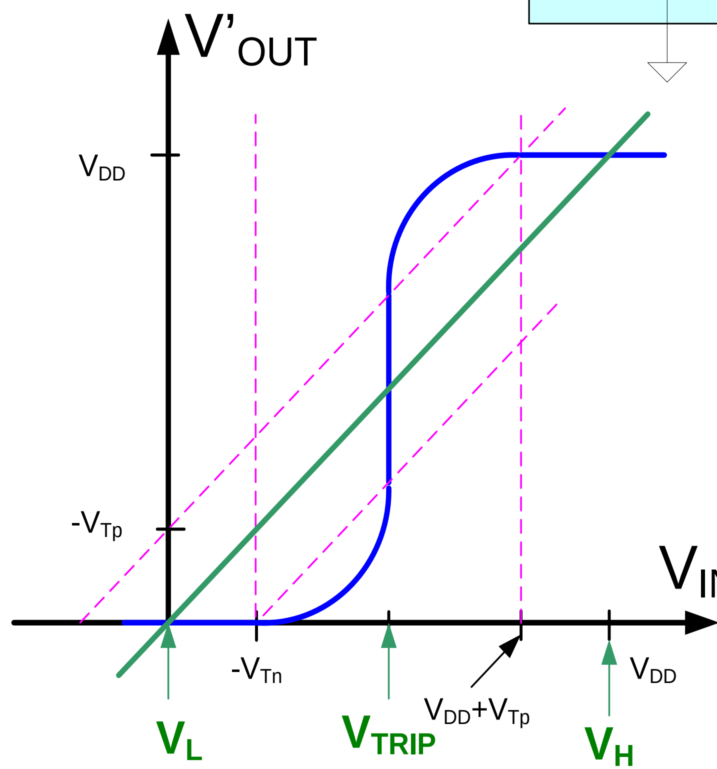
Find the points on the inverter pair transfer characteristics where $V_{OUT}' = V_{IN}$ and the slope is less than 1

Inverter Transfer Characteristics of Inverter Pair for THIS Logic Family





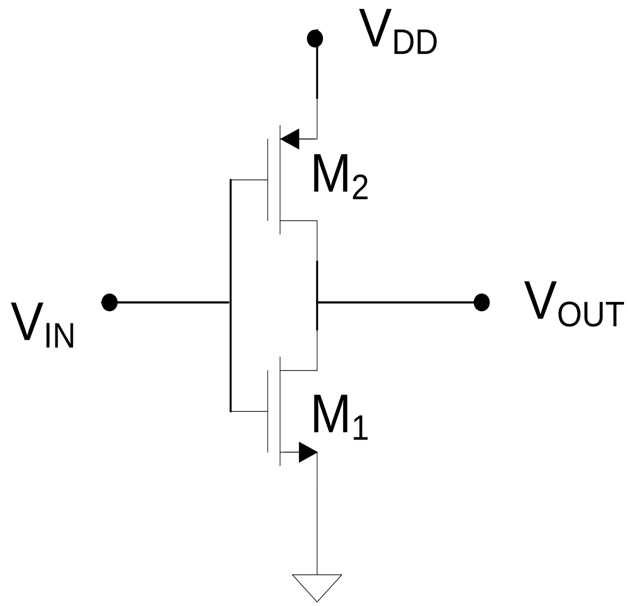




$V_H = V_{DD}$ and $V_L = 0$

Note this is independent of device sizing for THIS logic family !!

Sizing of the Basic CMOS Inverter

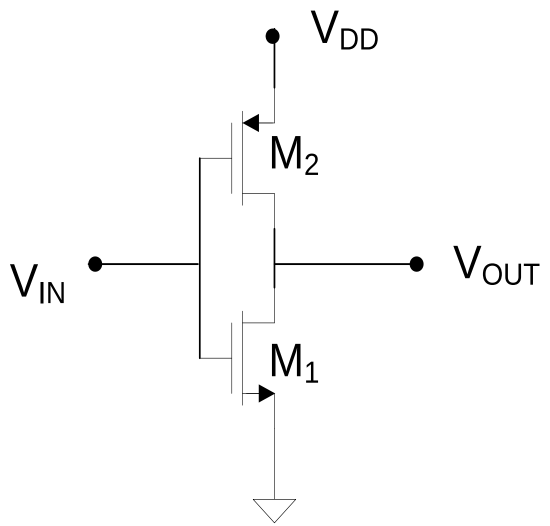


The characteristic that device sizes do not need to be used to establish V_H and V_L logic levels is a major advantage of this type of logic

How should M_1 and M_2 be sized?

How many degrees of freedom are there in the design of the inverter?

How should M_1 and M_2 be sized?



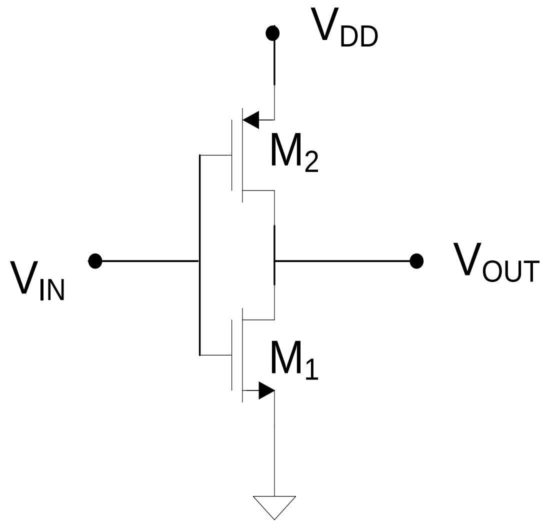
How many degrees of freedom are there in the design of the inverter?

$\{ W_1, W_2, L_1, L_2 \}$ 4 degrees of freedom

But in basic device model and in <u>most</u> performance metrics, W_1/L_1 and W_2/L_2 appear as ratios

$\{ W_1/L_1, W_2/L_2 \}$ effectively 2 degrees of freedom

How should M_1 and M_2 be sized?



$\{ W_1, W_2, L_1, L_2 \}$ 4 degrees of freedom Usually pick $L_1 = L_2 = L_{min}$

$\{ W_1, W_2 \}$ effectively 2 degrees of freedom

How are W_1 and W_2 chosen?

Depends upon what performance parameters are most important for a given application!

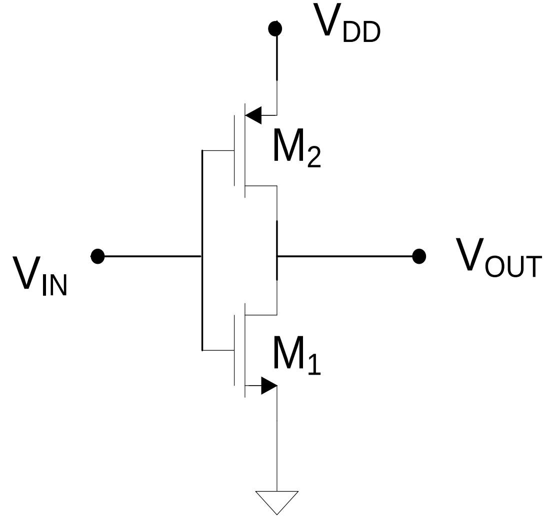
How should M_1 and M_2 be sized?

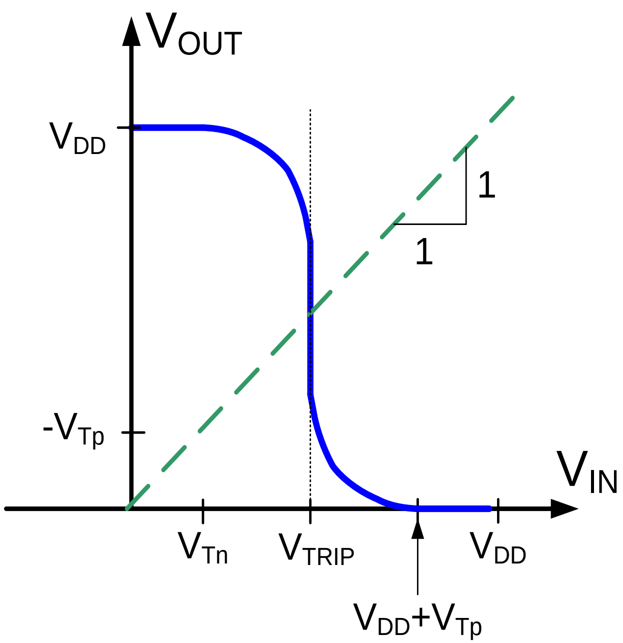
pick $L_1 = L_2 = L_{min}$

One popular sizing strategy:

1. Pick $W_1 = W_{MIN}$ to minimize area of M_1
2. Pick W_2 to set trip-point at $V_{DD}/2$

Observe Case 3 provides expression for V_{TRIP}



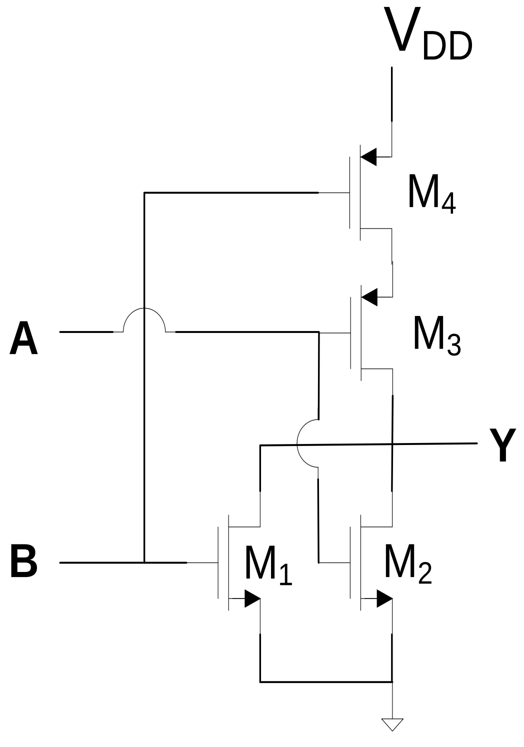


Thus, at the trip point,

$$V_{OUT} = V_{IN} = V_{TRIP} = \frac{V_{DD}}{1+\sqrt{\frac{\mu_n}{\mu_p}\frac{W_1}{W_2}}} + \frac{V_T\left(\sqrt{\frac{\mu_n}{\mu_p}\frac{W_1}{W_2}}-1\right)}{1+\sqrt{\frac{\mu_n}{\mu_p}\frac{W_1}{W_2}}}$$

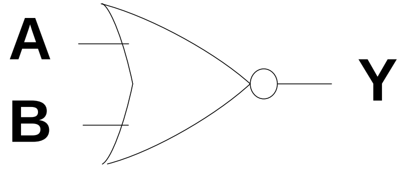
$$= \frac{V_{DD}}{2}, \quad \text{if } \frac{W_2}{W_1} = \frac{\mu_n}{\mu_p}$$

Extension of Basic CMOS Inverter to Multiple-Input Gates



A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

Truth Table

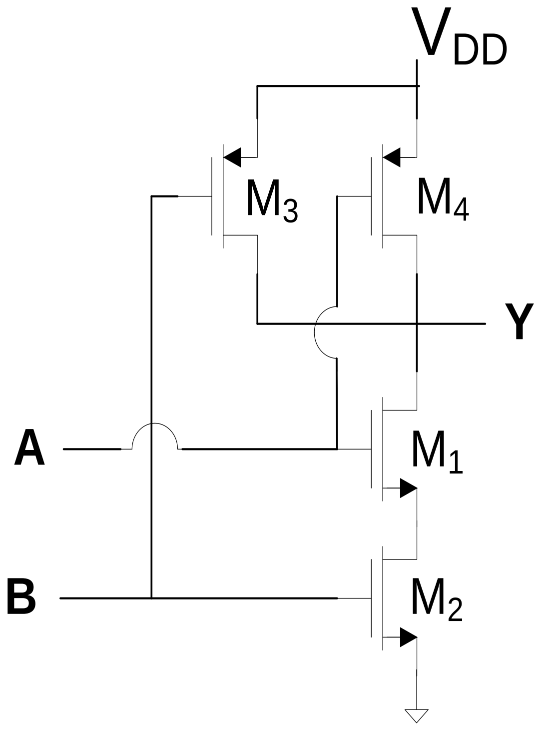


Performs as a 2-input NOR Gate

Can be easily extended to an n-input NOR Gate

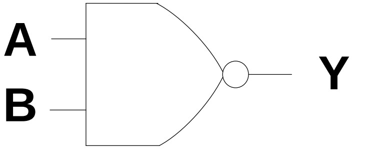
$V_H=V_{DD}$ and $V_L=0$ (inherited from inverter analysis)

Extension of Basic CMOS Inverter to Multiple-Input Gates



A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

Truth Table

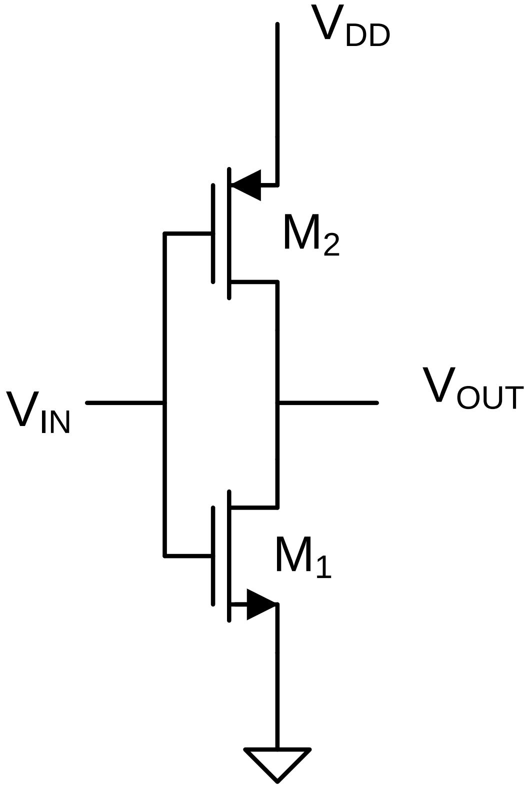


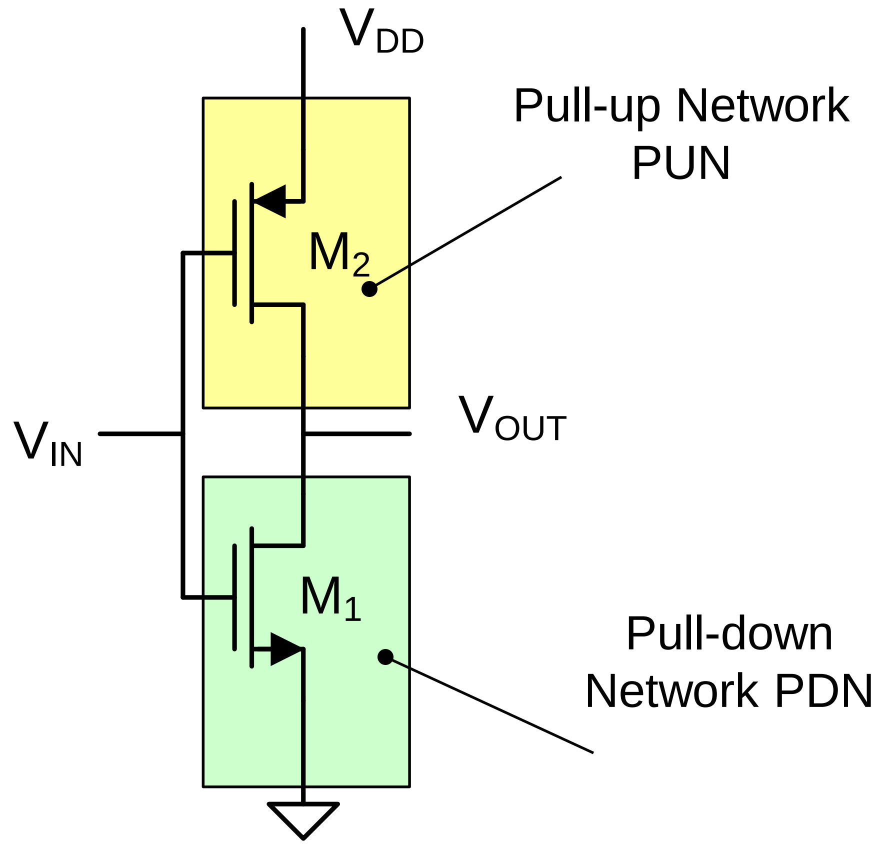
Performs as a 2-input NAND Gate

Can be easily extended to an n-input NAND Gate

V_H=V_{DD} and V_L=0 (inherited from inverter analysis)

Static CMOS Logic Family

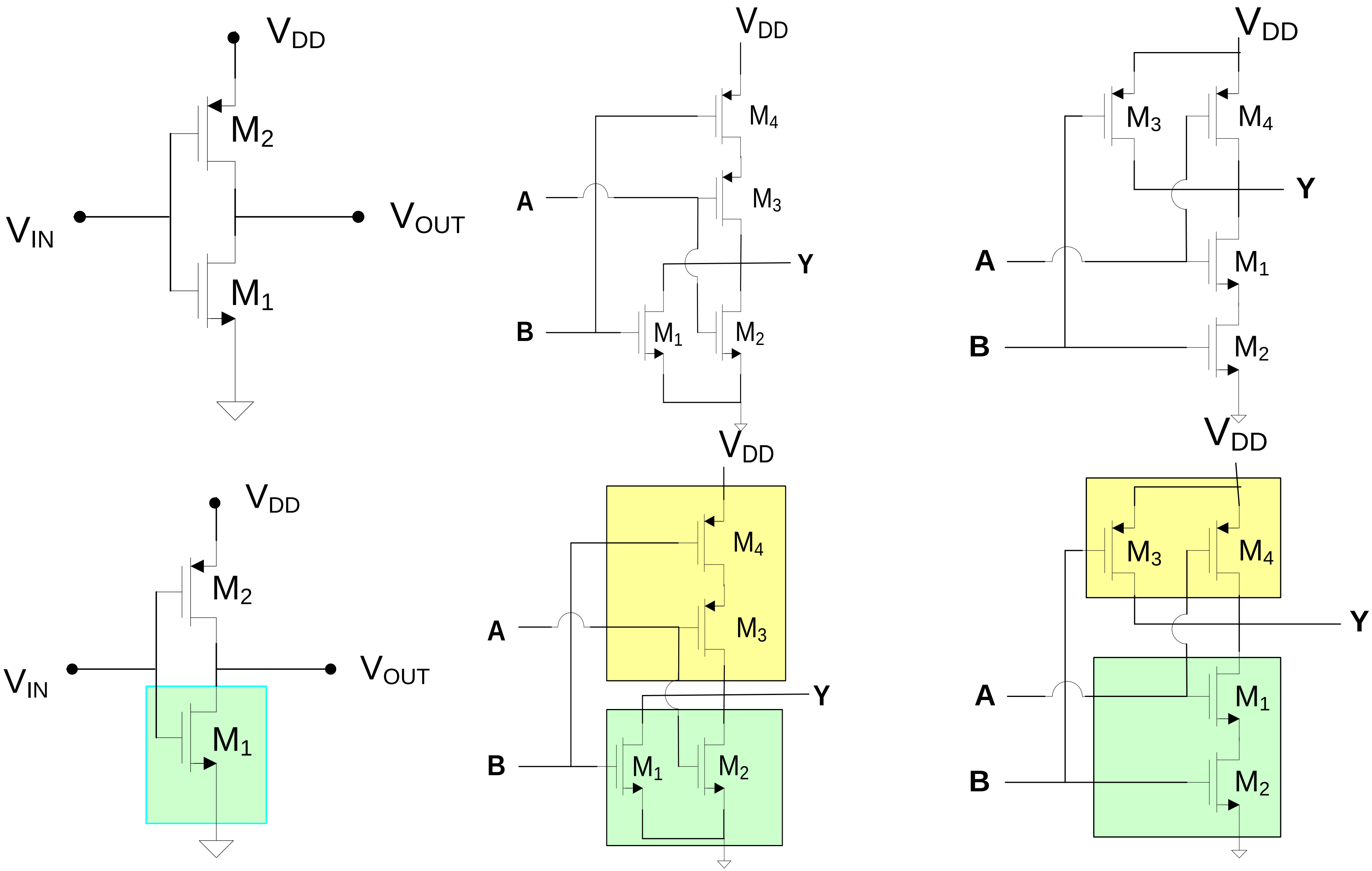




Observe PUN is p-channel, PDN is n-channel

V_H=V_{DD} and V_L=0 (inherited from inverter analysis)

Static CMOS Logic Family



n-channel PDN and p-channel PUN

$V_H = V_{DD}$, $V_L = 0V$ (same as for inverter!)

Digital Circuit Design

- Hierarchical Design
- Basic Logic Gates
- Properties of Logic Families
- Characterization of CMOS Inverter
- Static CMOS Logic Gates
  - Ratio Logic
- Propagation Delay
  - Simple analytical models
  - Elmore Delay
- Sizing of Gates
- Propagation Delay with Multiple Levels of Logic
- Optimal driving of Large Capacitive Loads
- Power Dissipation in Logic Circuits
- Other Logic Styles
- Array Logic
- Ring Oscillators

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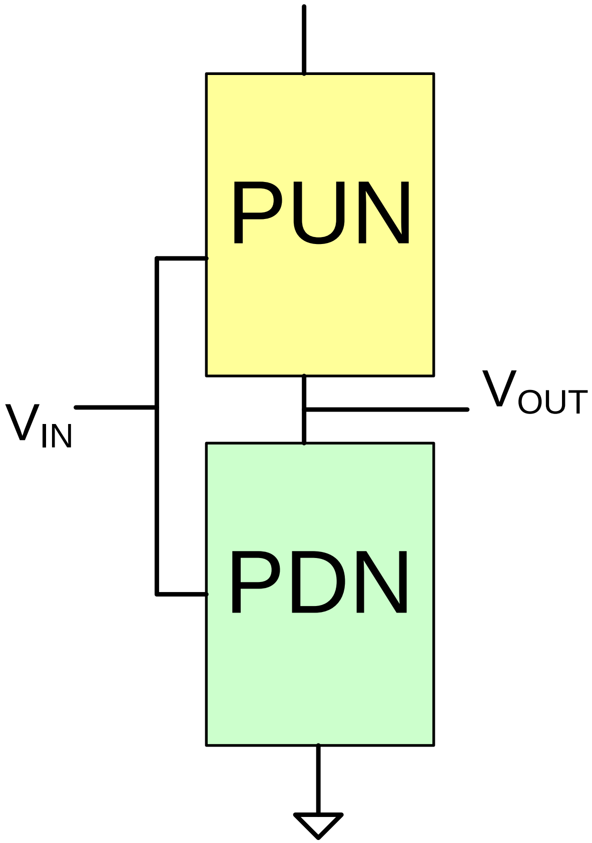
done

partial

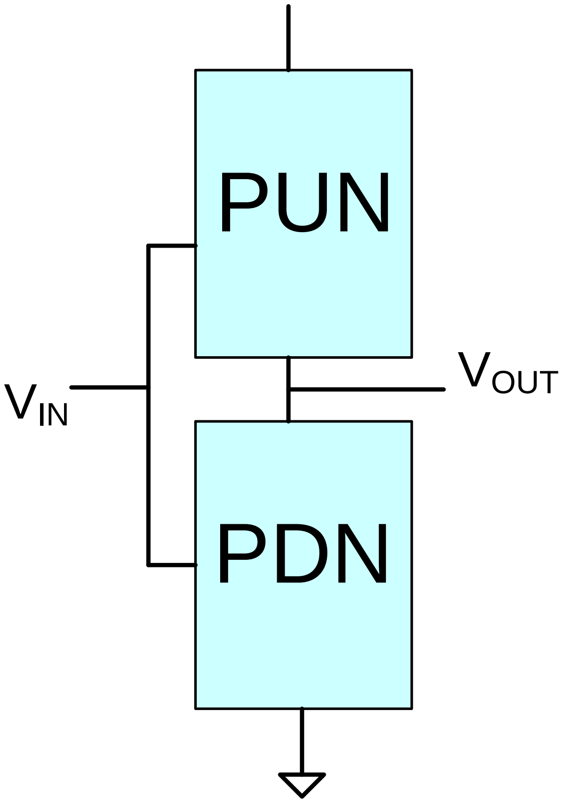
General Logic Family



Compound Gate in CMOS Process

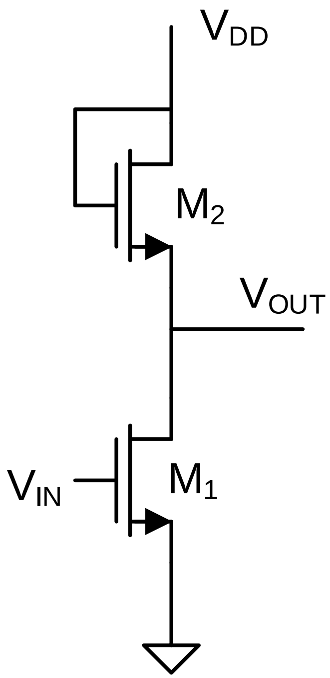
p-channel PUN
n-channel PDN

$V_H = V_{DD}$, $V_L = 0V$ (same as for inverter!)

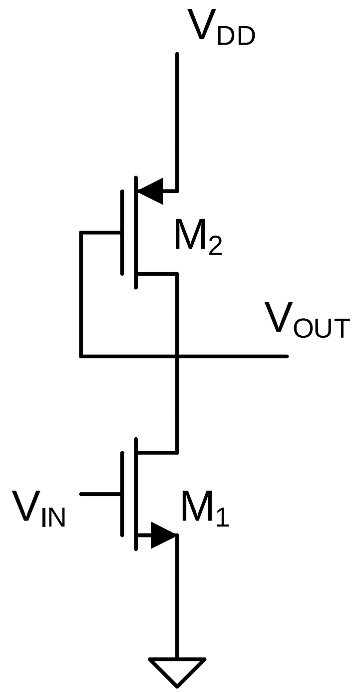


Arbitrary PUN and PDN

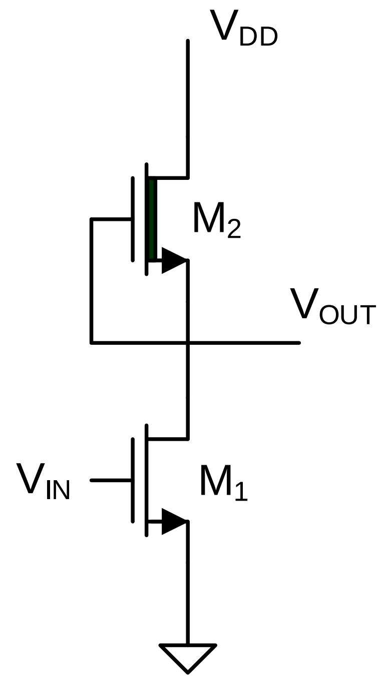
Other MOS Logic Families



Enhancement Load
NMOS

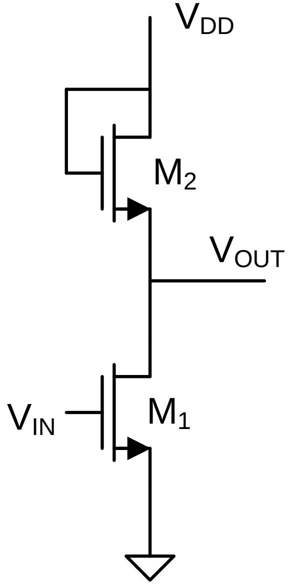


Enhancement Load
Pseudo-NMOS

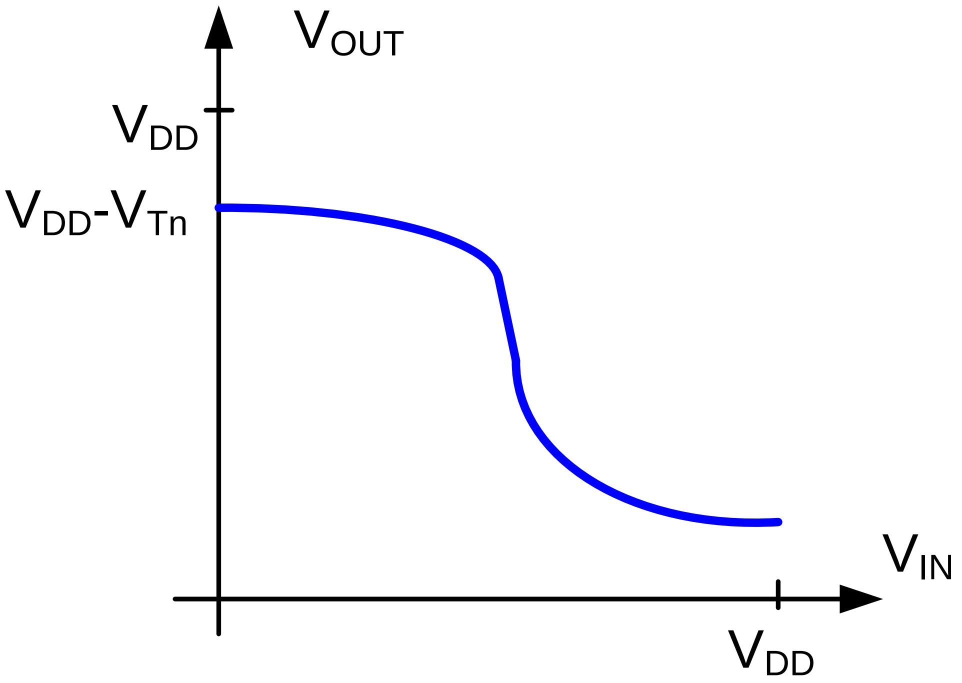


Depletion Load
NMOS

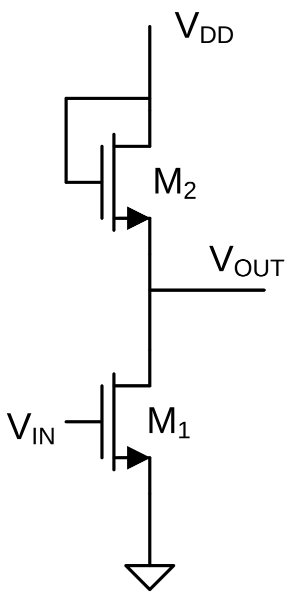
Other CMOS/MOS Logic Families



Enhancement
Load NMOS

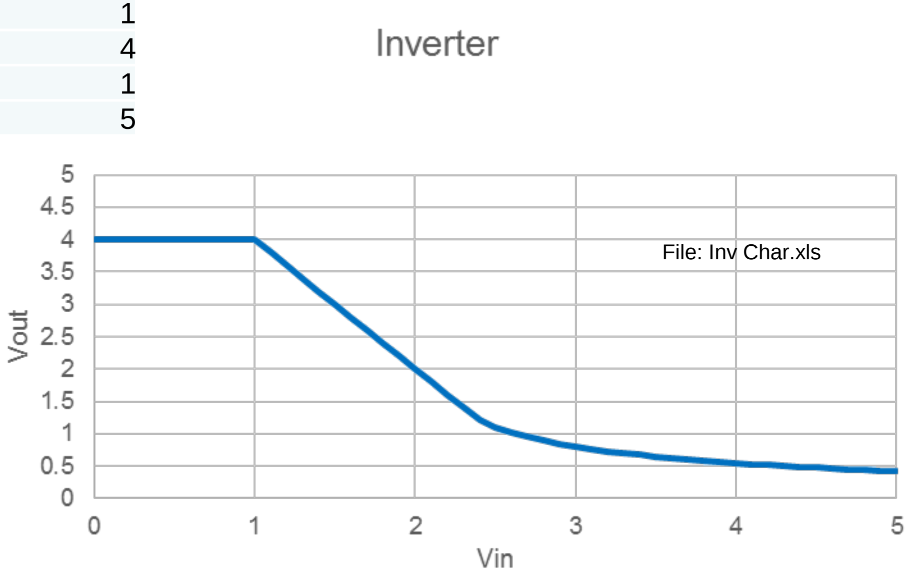


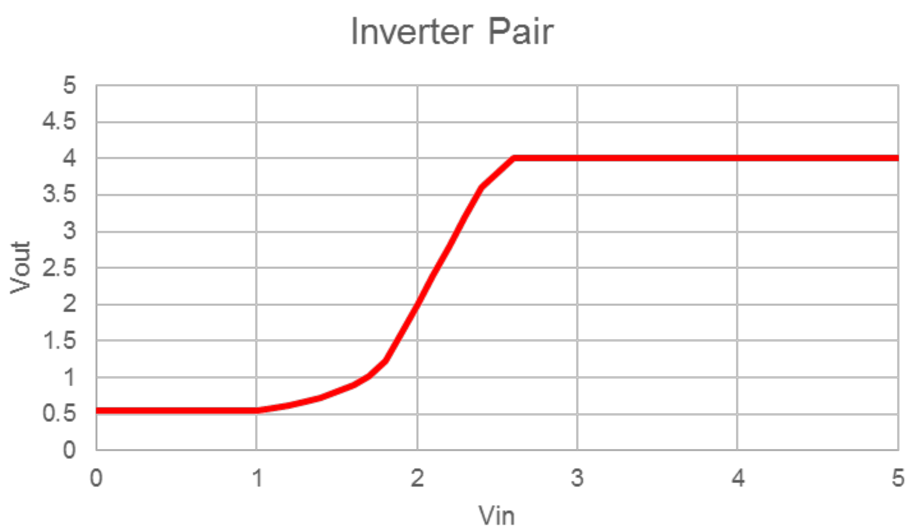
NMOS example



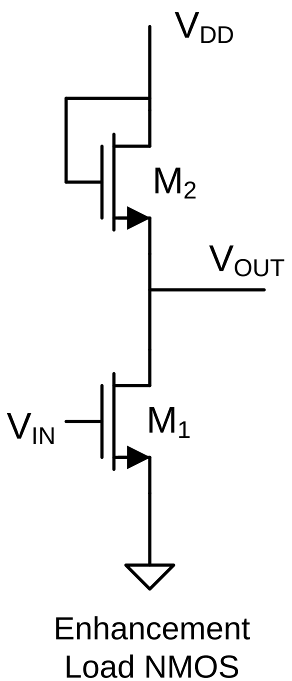
Enhancement
Load NMOS

VTH	1
W1/L1	4
W2/L2	1
VDD	5

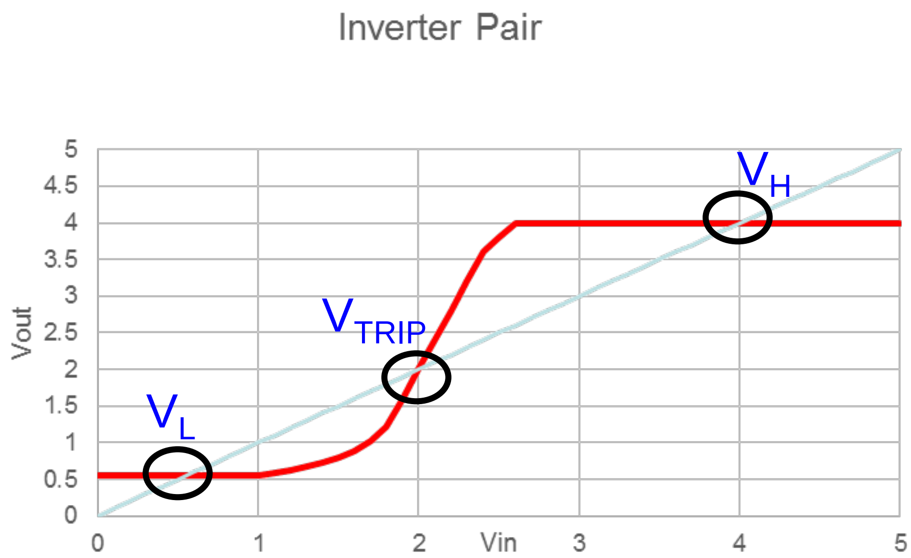




NMOS example

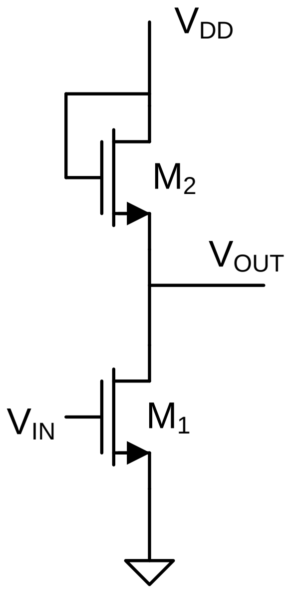


VTH	1
W1/L1	4
W2/L2	1
VDD	5

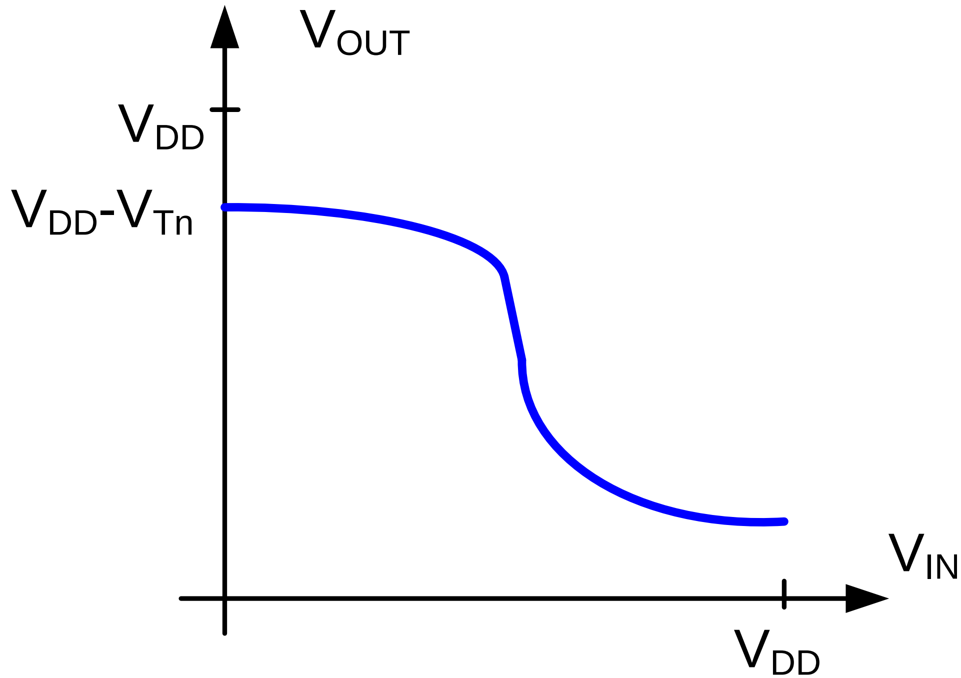


V_H=4V
V_L=0.55V
V_{TRIP}=2V

Other CMOS/MOS Logic Families



Enhancement
Load NMOS



- High and low swings are reduced
- Response time is slow on LH output transitions
- Static Power Dissipation Large when V_{OUT} is low (will show)
- Very economical process
- Termed “ratio logic” (because logic values dependent on device W/L ratios – USE UP DOF!)
- May not work for some device sizes
- Compact layout (no wells !)
- Available to use in standard CMOS process

End of Lecture 37