EE 330
Lecture 40

Digital Circuits

Propagation Delay – basic characterization
Device Sizing (Inverter and multiple-input gates)

Digital Circuit Design

- Hierarchical Design
- Basic Logic Gates
- Properties of Logic Families
- Characterization of CMOS Inverter
- Static CMOS Logic Gates
  - Ratio Logic
- Propagation Delay
  - Simple analytical models
  - Elmore Delay
- Sizing of Gates

- Propagation Delay with Multiple Levels of Logic
- Optimal driving of Large Capacitive Loads
- Power Dissipation in Logic Circuits
- Other Logic Styles
- Array Logic
- Ring Oscillators

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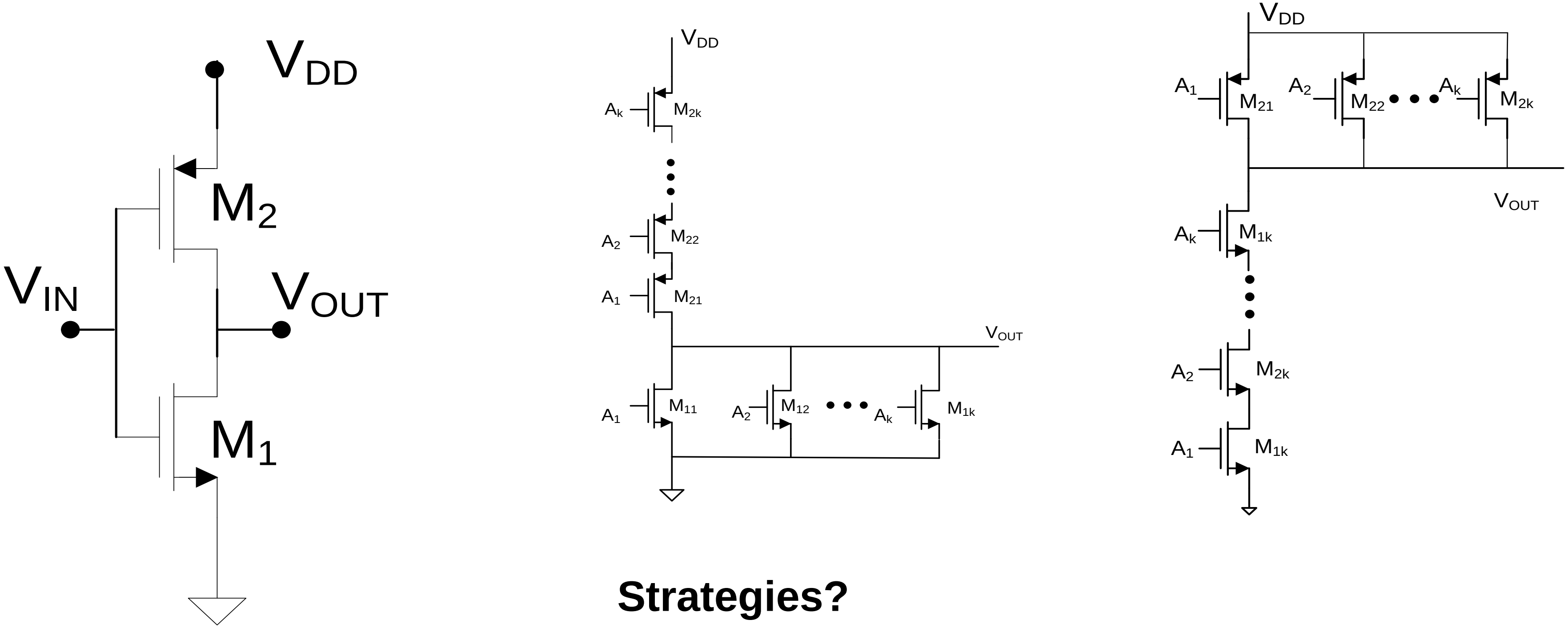
done

partial

Device Sizing

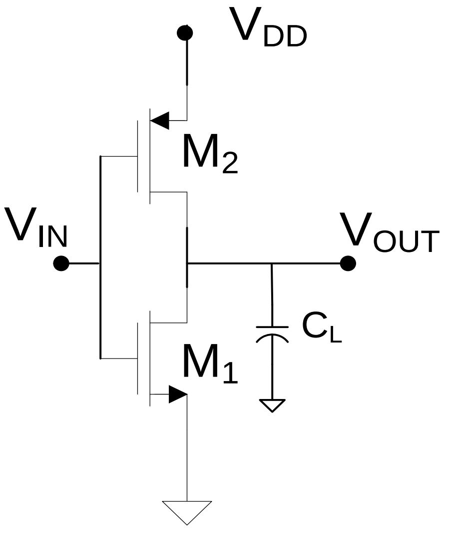


Strategies?

Degrees of Freedom?

Will consider the inverter first

Device Sizing

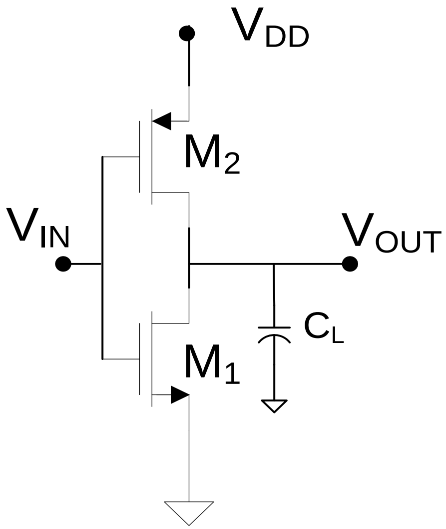


Degrees of Freedom?

Strategies?

Device Sizing

- Since not ratio logic, V_H and V_L are independent of device sizes for this inverter
- With $L_1=L_2=L_{min}$, there are 2 degrees of freedom (W_1 and W_2)

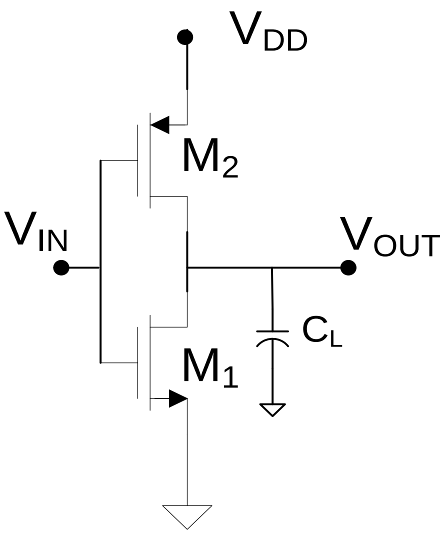


Sizing Strategies

- **Minimum Size**
- **Fixed V_{TRIP}**
- **Equal rise-fall times (equal worst-case rise and fall times)**
- **Minimum power dissipation**
- **Minimum time required to drive a given load**
- **Minimum input capacitance**

Device Sizing

Assume V_{Tn}=0.2V_{DD}, V_{Tp}=-0.2V_{DD}, μ_n/μ_p=3, L_1=L_2=L_{min}



Sizing Strategy: minimum sized

W_n=?, W_p=?, V_{trip}=?,t_{HL}=?,t_{LH}=?

$$R_{PD} = \frac{L_1}{\mu_n C_{OX} W_1 (V_{DD} - V_{Tn})}$$

$$R_{PU} = \frac{L_2}{\mu_p C_{OX} W_2 (V_{DD} + V_{Tp})}$$

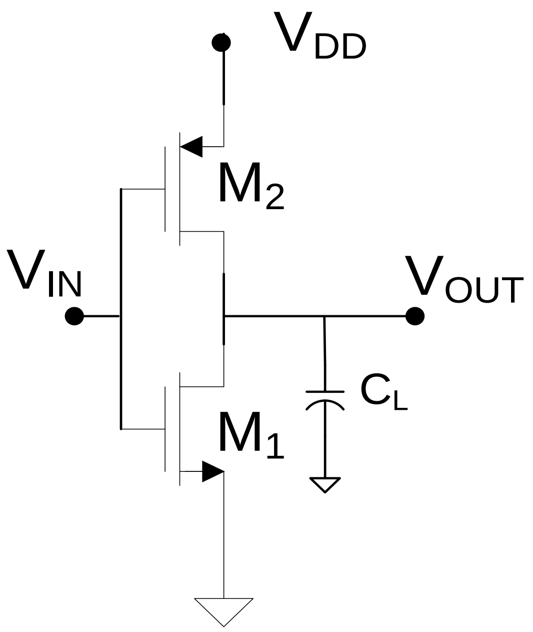
$$C_{IN} = C_{OX}(W_1 L_1 + W_2 L_2)$$

Device Sizing

Assume V_{Tn}=0.2V_{DD}, V_{Tp}=-0.2V_{DD}, μ_n/μ_p=3, $L_1=L_2=L_{min}$

Sizing Strategy: minimum sized

W_n=?, W_p=?, V_{trip}=?, t_{HL}=?, t_{LH}=?



$\boxed{W_1=W_2=W_{MIN}}$

also provides minimum input capacitance

$t_{HL}=R_{PD}C_L$

$t_{LH}=3\,R_{PD}C_L$

t_{LH} is longer than t_{HL}

$t_{PROP}=4R_{PD}C_L$

$$V_{TRIP}=\frac{(V_{Tn})+(V_{DD}+V_{Tp})\sqrt{\frac{\mu_p}{\mu_n}\frac{W_2}{W_1}\frac{L_1}{L_2}}}{1+\sqrt{\frac{\mu_p}{\mu_n}\frac{W_2}{W_1}\frac{L_1}{L_2}}}$$

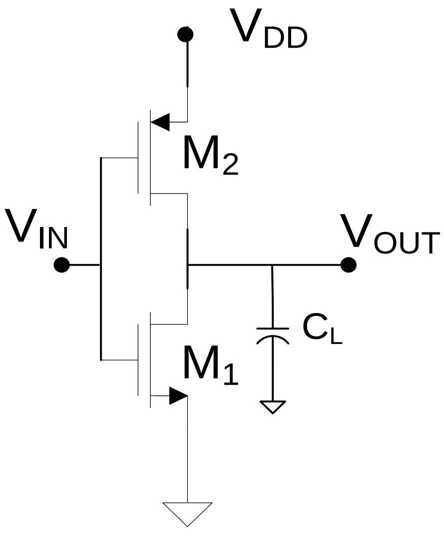
$$V_{TRIP}=\frac{(0.2V_{DD})+(V_{DD}\text{-}0.2V_{DD})\sqrt{\frac{1}{3}}}{1+\sqrt{\frac{1}{3}}}=.42V_{DD}$$

Device Sizing

Assume V_{Tn}=0.2V_{DD}, V_{Tp}=-0.2V_{DD}, μ_n/μ_p=3, $L_1=L_2=L_{min}$

Sizing strategy: Equal (worst case) rise and fall times

W_n=?, W_p=?, V_{trip}=?,t_{HL}=?,t_{LH}=?



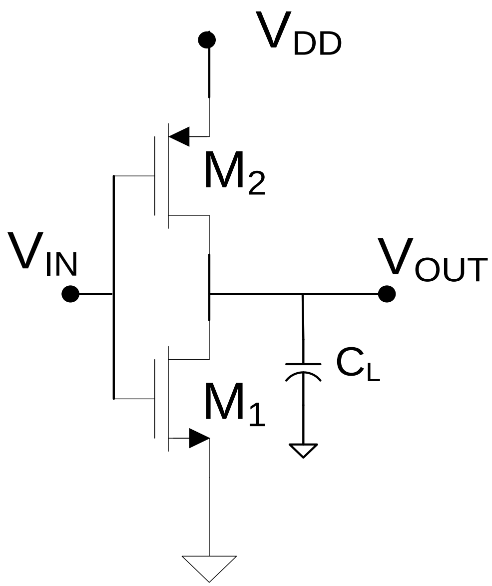
$$R_{PD} = \frac{L_{min}}{\mu_n C_{OX} W_1 (0.8V_{DD})}$$

$$R_{PU} = \frac{L_{min}}{3\mu_n C_{OX} W_2 (0.8V_{DD})}$$

Device Sizing

Assume V_{Tn}=0.2V_{DD}, V_{Tp}=-0.2V_{DD}, μ_n/μ_p=3, L_1=L_2=L_{min}

Sizing strategy: Equal (worst case) rise and fall times



$$\frac{t_{LH}}{t_{HL}}=\frac{R_{PU}C_{IN}}{R_{PD}C_{IN}} \Rightarrow R_{PU}=R_{PD}$$

Thus $$\frac{L_1}{u_n C_{OX} W_1 \left(V_{DD}-V_{Tn}\right)}=\frac{L_2}{u_p C_{OX} W_2 \left(V_{DD}+V_{Tp}\right)}$$

with L_1=L_2 and V_{Tp}=-V_{Tn} we must have

$$\boxed{\frac{W_2}{W_1}=\frac{\mu_n}{\mu_p}\cong 3}$$

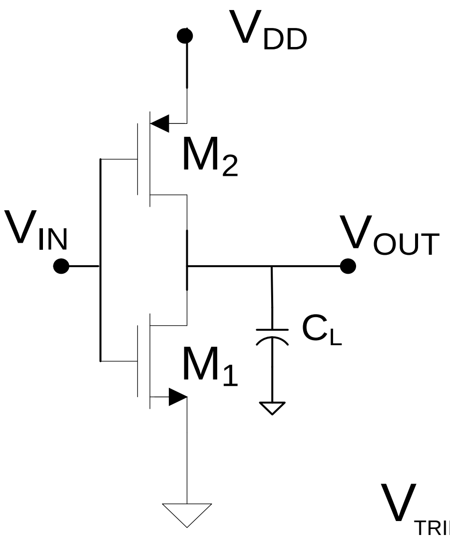
What about the second degree of freedom?

W_1=W_{MIN}

V_{TRIP}=?

Device Sizing

Assume V_{Tn}=0.2V_{DD}, V_{Tp}=-0.2V_{DD}, μ_n/μ_p=3, L_1=L_2=L_{min}



Sizing strategy: Equal (worst-case) rise and fall times

W_n=W_{MIN},W_p =3W_{MIN}, V_{trip}=?,t_{HL}=?,t_{LH}=?

$$V_{TRIP} = \frac{(V_{Tn}) + (V_{DD} + V_{Tp})\sqrt{\frac{\mu_p}{\mu_n}\frac{W_2}{W_1}\frac{L_1}{L_2}}}{1+\sqrt{\frac{\mu_p}{\mu_n}\frac{W_2}{W_1}\frac{L_1}{L_2}}} = \frac{0.2V_{DD}+0.8V_{DD}}{2} = \frac{V_{DD}}{2}$$

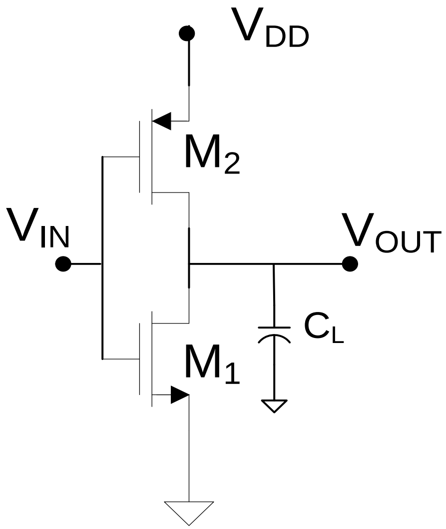
$$t_{HL} = t_{LH} = R_{pd}C_L = \frac{L_{min}}{\mu_n C_{OX} W_{min}(0.8V_{DD})}C_L$$

$$t_{PROP} = 2\,R_{pd}C_L$$

For a fixed C_L, how does t_{prop} compare for the minimum-sizing compared to equal rise/fall sizing?

Device Sizing

Assume V_{Tn}=0.2V_{DD}, V_{Tp}=-0.2V_{DD}, μ_n/μ_p=3, L_1=L_2=L_{min}



Sizing strategy: Fixed V_{TRIP}= V_{DD}/2

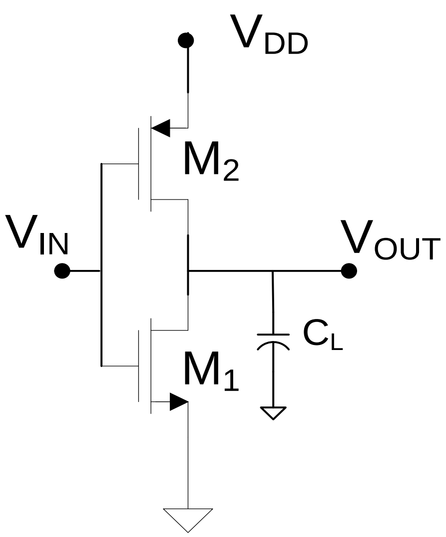
W_n=?, W_p=?, V_{trip}=?, t_{HL}=?, t_{LH}=?

Device Sizing

Assume V_{Tn}=0.2V_{DD}, V_{Tp}=-0.2V_{DD}, μ_n/μ_p=3, L_1=L_2=L_{min}

Sizing strategy: Fixed V_{TRIP}=V_{DD}/2

W_n=?, W_p=? , V_{trip}=?,t_{HL}=?,t_{LH}=?



Set

V_{TRIP}=V_{DD}/2

$$V_{TRIP} = \frac{(.2V_{DD}) + (V_{DD} - .2V_{DD})\sqrt{\frac{\mu_p}{\mu_n}\frac{W_2}{W_1}\frac{L_1}{L_2}}}{1+\sqrt{\frac{\mu_p}{\mu_n}\frac{W_2}{W_1}\frac{L_1}{L_2}}} = \frac{V_{DD}}{2}$$

Solving, obtain

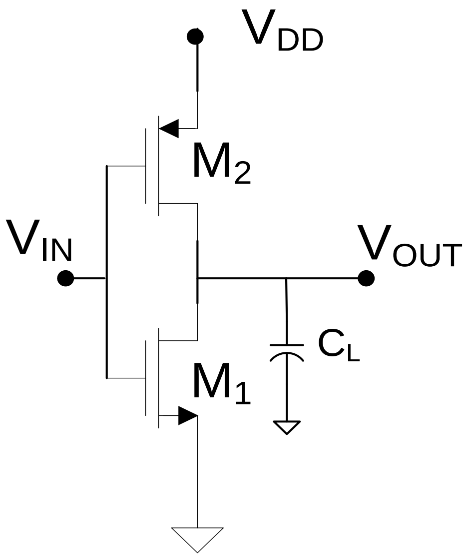
$$\boxed{\frac{W_2}{W_1} = \frac{\mu_n}{\mu_p}}$$

W_n=W_{MIN}, W_p =3W_{MIN}

- **This is the same sizing as was obtained for equal worst-case rise and fall times so t_{HL}=t_{LH}=$R_{pd}C_L$**
- **This is no coincidence !!! Why?**
- **These properties guide the definition of the process parameters provided by the foundry**

Device Sizing

Assume $V_{Tn}=0.2V_{DD}$, $V_{Tp}=-0.2V_{DD}$, $\mu_n/\mu_p=3$, $L_1=L_2=L_{min}$



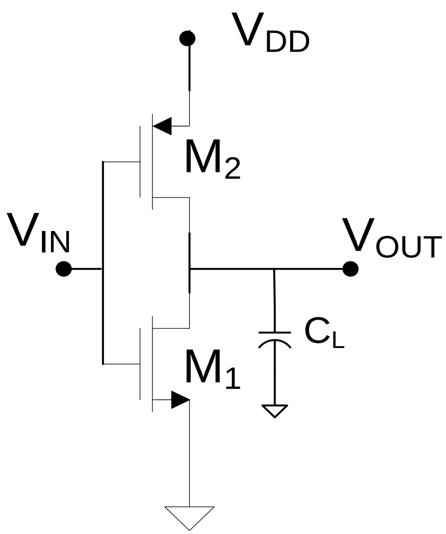
Sizing Strategies

- **Minimum Size**
- **Fixed V_{TRIP}**
- **Equal rise-fall times**
  (equal worst-case rise and fall times)
- **Minimum power dissipation**
- **Minimum time required to drive a given load**
- **Minimum input capacitance**

Device Sizing

Assume V_{Tn}=0.2V_{DD}, V_{Tp}=-0.2V_{DD}, μ_n/μ_p=3, $L_1=L_2=L_{min}$

Sizing Strategy Summary



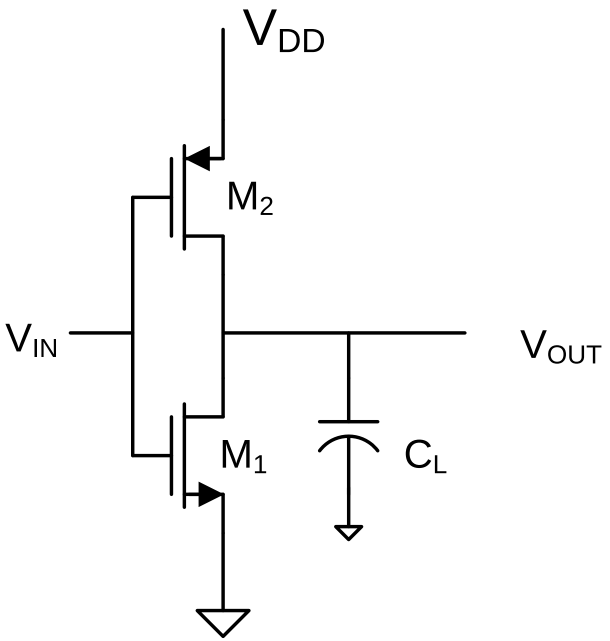
	Minimum Size	$V_{TRIP}=V_{DD}/2$	Equal Rise/Fall
Size	$W_n=W_p=W_{min}$ $L_p=L_n=L_{min}$	$W_n=W_{min}$ $W_{p=}3W_{min}$ $L_p=L_n=L_{min}$	$W_n=W_{min}$ $W_{p=}3W_{min}$ $L_p=L_n=L_{min}$
t_{HL}	$R_{pd}C_L$	$R_{pd}C_L$	$R_{pd}C_L$
t_{LH}	$3R_{pd}C_L$	$R_{pd}C_L$	$R_{pd}C_L$
t_{PROP}	$4R_{pd}C_L$	$2R_{pd}C_L$	$2R_{pd}C_L$
V_{trip}	$V_{TRIP}=0.42V_{DD}$	$V_{TRIP}=0.5V_{DD}$	$V_{TRIP}=0.5V_{DD}$

- **For a fixed load C_L, the minimum-sized structure has a higher t_{PROP} but if the load is another inverter, C_L will also change so the speed improvements become less apparent**
- **This will be investigated later**

Reference Inverter

The reference inverter

Assume $\mu_n/\mu_p=3$ **$W_n=W_{MIN}$, $W_p=3W_n$**
$L_n=L_p=L_{MIN}$



$$C_{REF} \underset{def}{=} C_{INREF} = 4C_{OX}W_{MIN}L_{MIN}$$

$$R_{PDREF} = \frac{L_{MIN}}{\mu_n C_{OX} W_{MIN}\left(V_{DD}-V_{Tn}\right)} \overset{V_{Tn}=.2V_{DD}}{=} \frac{L_{MIN}}{\mu_n C_{OX} W_{MIN}\left(0.8V_{DD}\right)}$$

$$R_{PUREF} = \frac{L_{MIN}}{\mu_p C_{OX} 3W_{MIN}\left(V_{DD}+V_{Tp}\right)} \overset{V_{Tp}=-.2V_{DD}}{=} R_{PDREF}$$

- **Have sized the reference inverter with $W_p/W_n=\mu_n/\mu_p$**
- **In standard processes, provides $V_{TRIP} \approx V_{DD}/2$ and $t_{HL} \approx t_{LH}$**
- **Any other sizing strategy could have been used for the reference inverter but this is most convenient**

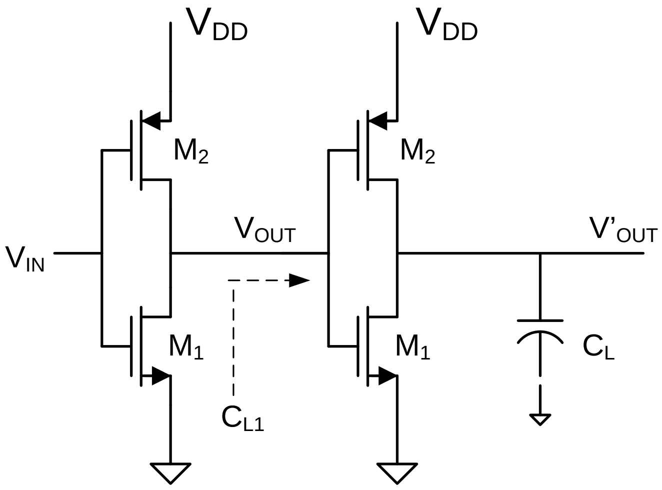
Reference Inverter

The reference inverter pair

Assume $\mu_n/\mu_p=3$

$L_n=L_p=L_{MIN}$

$W_n=W_{MIN}$, $W_p=3W_n$



$$C_{L1}= C_{REF}=4C_{OX}W_{MIN}L_{MIN}$$

$$t_{REF} \underset{def}{=} t_{PROPREF}= t_{HLREF}+t_{LHREF}=2R_{PDREF}C_{REF}$$

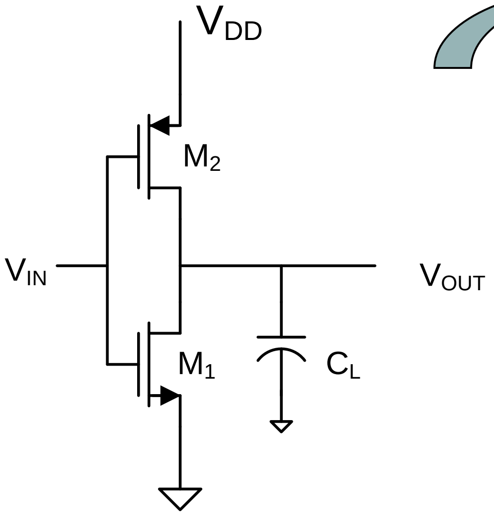
Reference Inverter

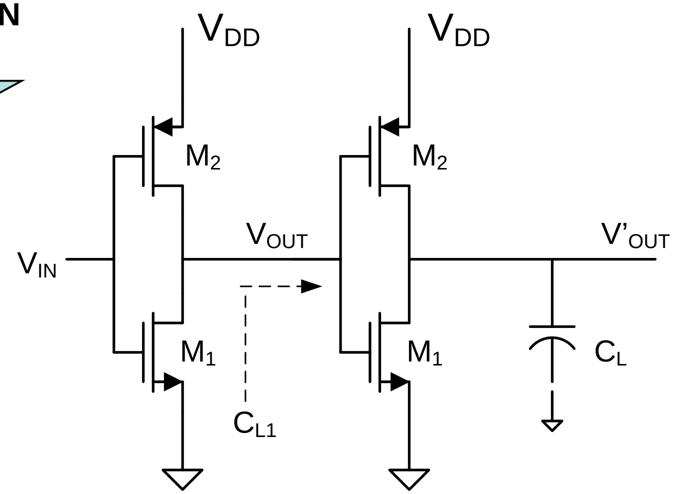
The reference inverter pair

Assume $\mu_n/\mu_p=3$

$L_n=L_p=L_{MIN}$

$W_n=W_{MIN}$, $W_p=3W_n$





Summary: parameters defined from reference inverter:

$$C_{REF}=4C_{OX}W_{MIN}L_{MIN}$$

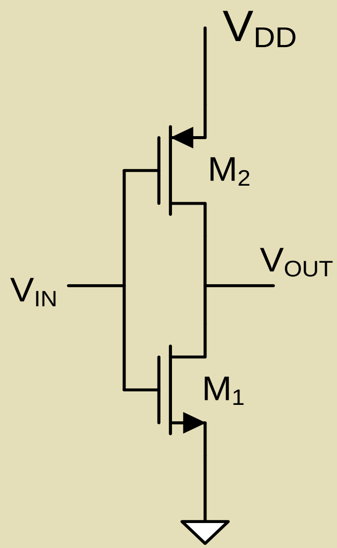
$$R_{PDREF}=\frac{L_{MIN}}{\mu_n C_{OX}W_{MIN}\left(V_{DD}-V_{Tn}\right)}$$

$$t_{REF}=2R_{PDREF}C_{REF}$$

$$C_{REF}=4C_{OX}W_{MIN}L_{MIN}$$

The Reference Inverter

Reference Inverter



Assume $\mu_n/\mu_p=3$

$W_n=W_{MIN}$, $W_p=3W_{MIN}$

$L_n=L_p=L_{MIN}$

In 0.5u proc t_{REF}=20ps, C_{REF}=4fF, $R_{PDREF}=R_{PUREF}$=2.5K

$$R_{PDREF}=R_{PUREF}$$

$$\mathbf{C_{REF}=C_{IN}=4C_{OX}W_{MIN}L_{MIN}}$$

$$R_{PDREF}=\frac{L_{MIN}}{\mu_n C_{OX} W_{MIN}\left(V_{DD}-V_{Tn}\right)}\overset{V_{Tn}=.2V_{DD}}{=}\frac{L_{MIN}}{\mu_n C_{OX} W_{MIN}\left(0.8V_{DD}\right)}$$

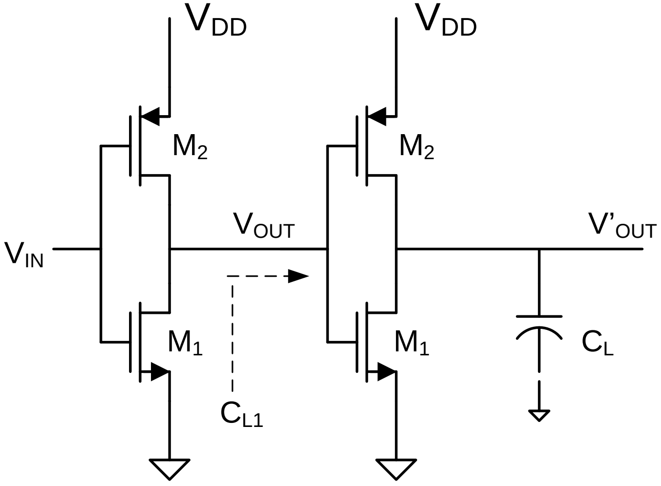
$$\mathbf{t_{HLREF}=t_{LHREF}=R_{PDREF}C_{REF}}$$

$$\mathbf{t_{REF}=t_{HLREF}+t_{LHREF}=2R_{PDREF}C_{REF}}$$

(Note: This C_{OX} is somewhat larger than that in the 0.5u ON process)

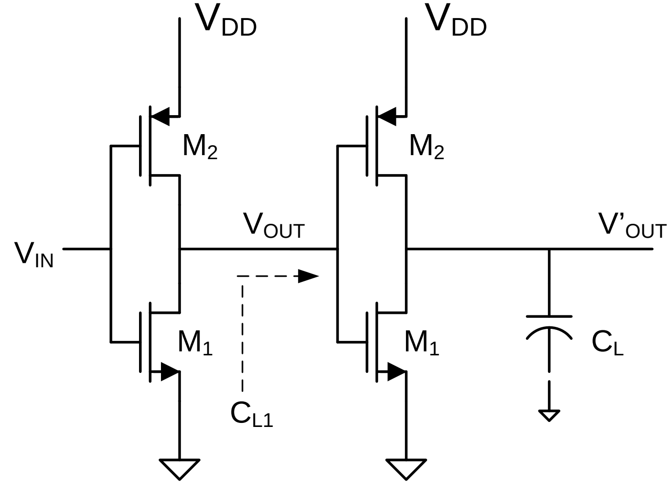
Propagation Delay

How does the propagation delay compare for a minimum-sized strategy to that of an equal rise/fall sizing strategy?



Minimum Sized

$$\mathbf{W_2=W_1=W_{MIN}}$$



Reference Inverter

$$\mathbf{W_2=(\mu_n/\mu_p)W_1,\ \ W_1=W_{MIN}}$$

$$t_{PROP} = t_{REF}$$

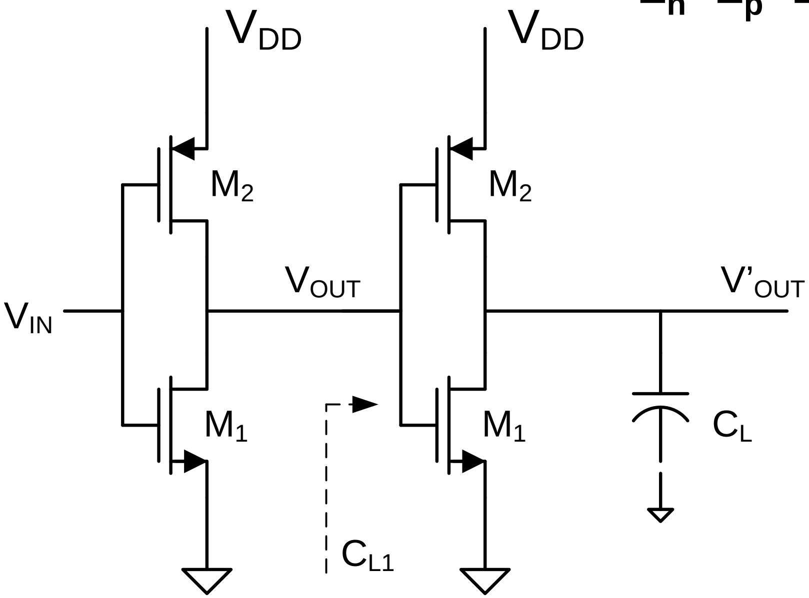
Device Sizing

The minimum-sized inverter pair

Assume $\mu_n/\mu_p=3$

$L_n=L_p=L_{MIN}$

$W_n=W_{MIN}$, $W_p=W_n$



$$C_{REF} = 4C_{OX}W_{MIN}L_{MIN}$$

$$C_{L1} = 0.5C_{REF} = 2C_{OX}W_{MIN}L_{MIN}$$

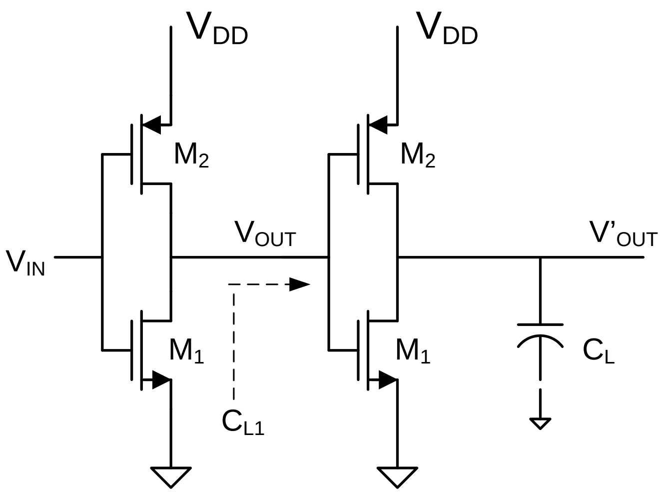
$$R_{PDREF} = \frac{L_{MIN}}{\mu_n C_{OX} W_{MIN}\left(V_{DD}-V_{Tn}\right)} \overset{V_{Tn}=.2V_{DD}}{=} \frac{L_{MIN}}{\mu_n C_{OX} W_{MIN}\left(0.8V_{DD}\right)}$$

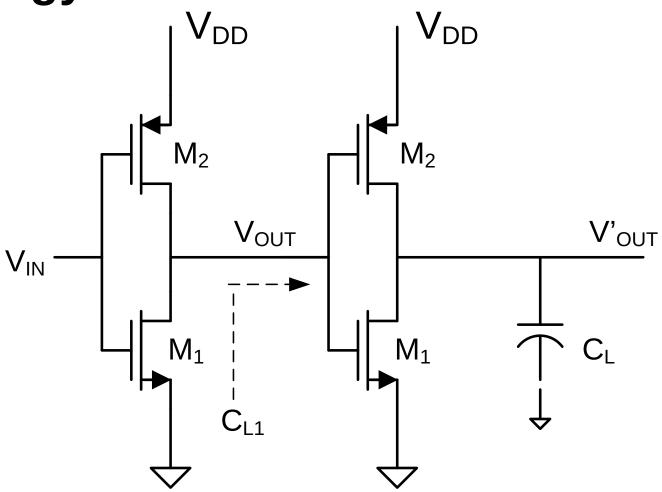
$$t_{PROP} = t_{HLREF} + t_{LHREF} = R_{PDREF}\left(0.5C_{REF}\right) + 3R_{PDREF}\left(0.5C_{REF}\right) = 2R_{PDREF}C_{REF}$$

$$t_{PROP} = t_{REFF}$$

Propagation Delay

How does the propagation delay compare for a minimum-sized strategy to that of an equal rise/fall sizing strategy?





Minimum Sized

$\mathbf{W_2=W_1=W_{MIN}}$

$t_{PROP} = t_{REF}$

Reference Inverter

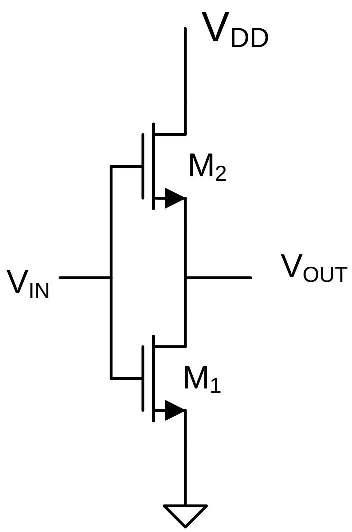
$\mathbf{W_2=(\mu_n/\mu_p)W_1, \;\; W_1=W_{MIN}}$

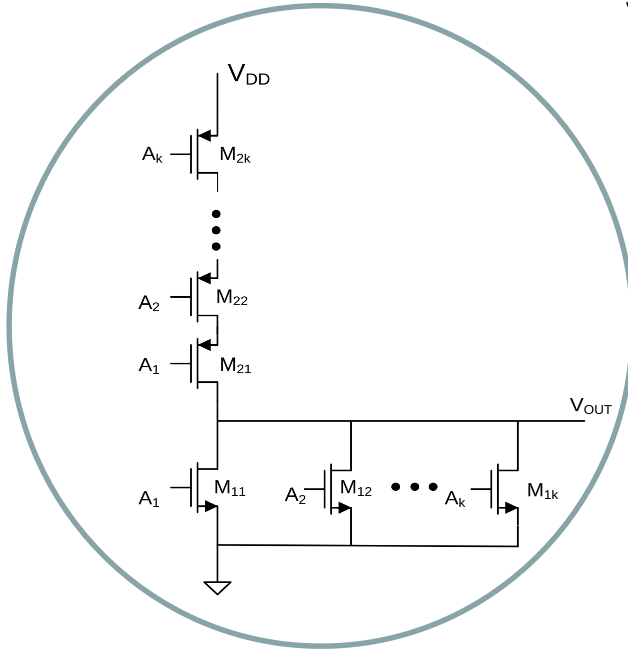
$t_{PROP} = t_{REF}$

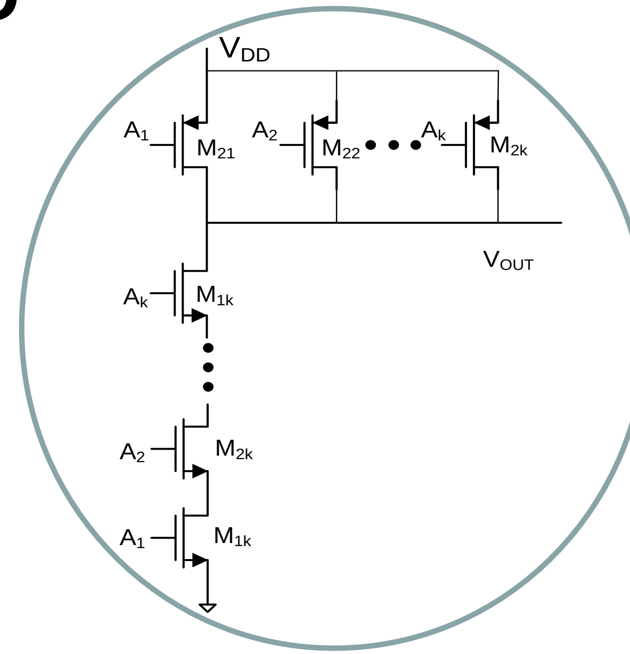
They are the same!

Even though the t_{LH} rise time has been reduced with the equal rise/fall sizing strategy, this was done at the expense of an increase in the total load capacitance that resulted in no net change in propagation delay!

Device Sizing







Will consider now the multiple-input gates

Will consider both minimum sizing and equal <u>worst-case</u> rise/fall

Will assume C_L (not shown)=C_{REF}

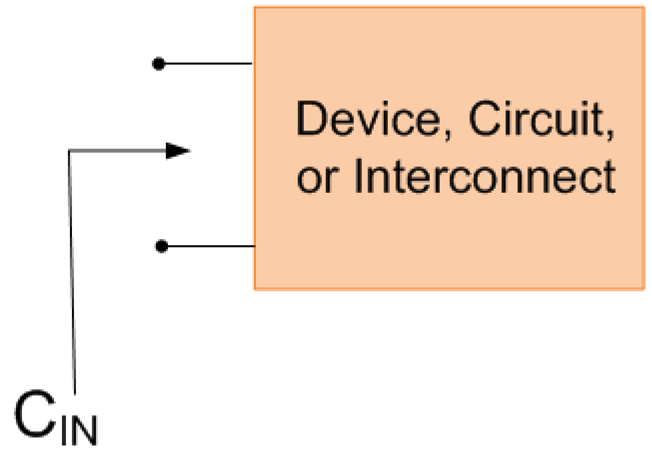
Will initially size so gate drive capability is same as that of ref inverter

Note: worst-case has been added since fall time in NOR gates or rise time in NAND gates depends upon how many transistors are conducting

Fan In

- **The Fan In (FI) to an input of a gate device, circuit or interconnect that is capacitive is the input capacitance**

- **Often this is normalized to some capacitance (typically C_{REF} of ref inverter).**

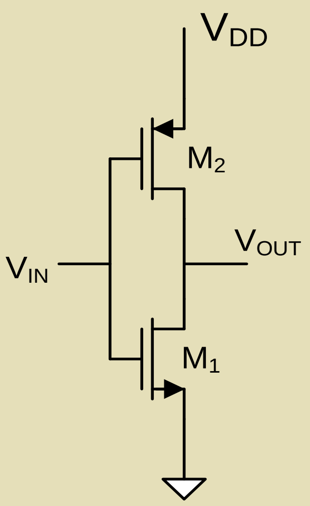


$$FI = C_{IN} \qquad \text{alternately} \qquad FI = \frac{C_{IN}}{C_{REF}}$$

Sizing of Multiple-Input Gates

Analysis strategy : Express delays in terms of those of reference inverter

Reference Inverter



Assume $\mu_n/\mu_p=3$

$W_n=W_{MIN}$, $W_p=3W_{MIN}$

$L_n=L_p=L_{MIN}$

In 0.5u proc t_{REF}=20ps, C_{REF}=4fF, R_{PDREF}=2.5K

$$C_{IN}=C_{REF}=4C_{OX}W_{MIN}L_{MIN}$$

$FI_{REF}=C_{REF}$ **alternately** $FI_{REF}=\dfrac{C_{IN}}{C_{REF}}=1$

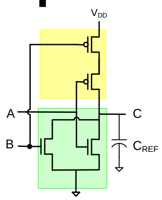
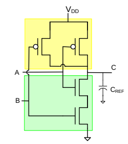
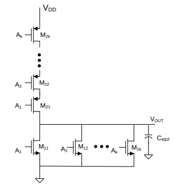
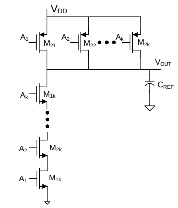
$$R_{PDREF}=R_{PUREF}=\frac{L_{MIN}}{\mu_n C_{OX} W_{MIN}\left(0.8V_{DD}\right)}$$

$$t_{HLREF}=t_{LHREF}=R_{PDREF}C_{REF}$$

$$t_{REF}=t_{HLREF}+t_{LHREF}=2R_{PDREF}C_{REF}$$

Device Sizing

Multiple Input Gates:

2-input NOR	2-input NAND	k-input NOR	k-input NAND
			

Equal Worst Case Rise/Fall **(and equal to that of ref inverter when driving C_{REF})**

W_n=?

W_p=?

Fastest response (t_{HL} or t_{LH}) = ?

Worst case response (t_{PROP}, usually of most interest)?

Input capacitance (FI) = ?

Minimum Sized **(assume driving a load of C_{REF})**

$W_n=W_{min}$

$W_p=W_{min}$

Fastest response (t_{HL} or t_{LH}) = ?

Slowest response (t_{HL} or t_{LH}) = ?

Worst case response (t_{PROP}, usually of most interest)?

Input capacitance (FI) = ?

Device Sizing

Equal Worst Case Rise/Fall **(and equal to that of ref inverter when driving C_{REF})**

Multiple Input Gates: **2-input NOR**

(n-channel devices sized same, p-channel devices sized the same)

Assume L_n=L_p=Lmin and driving a load of C_{REF}

W_n=?

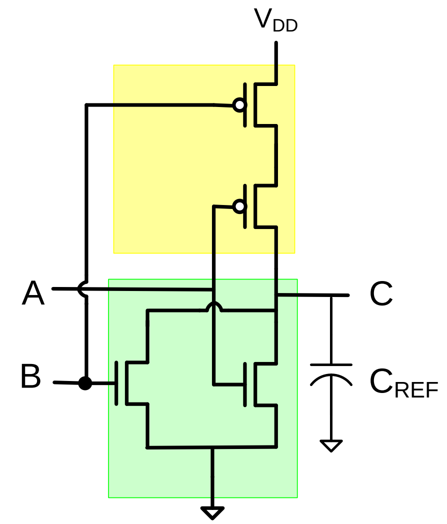
DERIVATIONS

W_p=?

Input capacitance = ?

FI=?

t_{PROP}=? (worst case)



$W_n = W_{MIN}$

$W_p = 6W_{MIN}$

$$C_{INA} = C_{INB} = C_{OX}W_{MIN}L_{MIN} + 6C_{OX}W_{MIN}L_{MIN} = 7C_{OX}W_{MIN}L_{MIN} = \left(\frac{7}{4}\right)4C_{OX}W_{MIN}L_{MIN} = \left(\frac{7}{4}\right)C_{REF}$$

$$FI = \left(\frac{7}{4}\right)C_{REF} \quad \textit{or} \quad FI = \frac{7}{4}$$

$t_{PROP} = t_{REF}$ (worst case)

Device Sizing

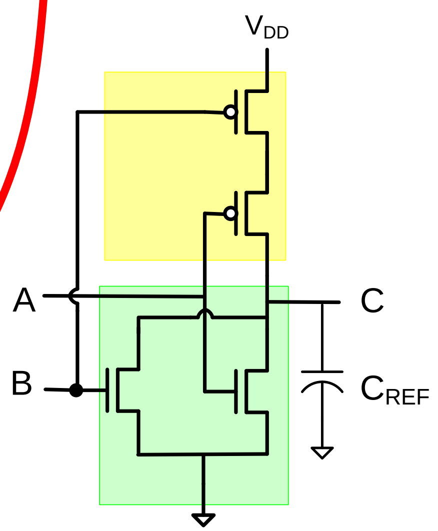
Equal Worst Case Rise/Fall

(and equal to that of ref inverter when driving C_{REF})

Multiple Input Gates: 2-input NOR

(n-channel devices sized same, p-channel devices sized the same)

Assume L_n=L_p=Lmin and driving a load of C_{REF}



W_n=?

DERIVATIONS

W_p=?

Input capacitance = ?

FI=?

t_{PROP}=? (worst case)

One degree of freedom was used to satisfy the constraint indicated

$\boxed{W_n = W_{MIN}}$

Other degree of freedom was used to achieve equal rise and fall times

$\boxed{W_p = 6W_{MIN}}$

$$C_{INA} = C_{INB} = C_{OX}W_{MIN}L_{MIN} + 6C_{OX}W_{MIN}L_{MIN} = 7C_{OX}W_{MIN}L_{MIN} = \left(\frac{7}{4}\right)4C_{OX}W_{MIN}L_{MIN} = \left(\frac{7}{4}\right)C_{REF}$$

$$FI = \left(\frac{7}{4}\right)C_{REF} \qquad or \qquad FI = \frac{7}{4}$$

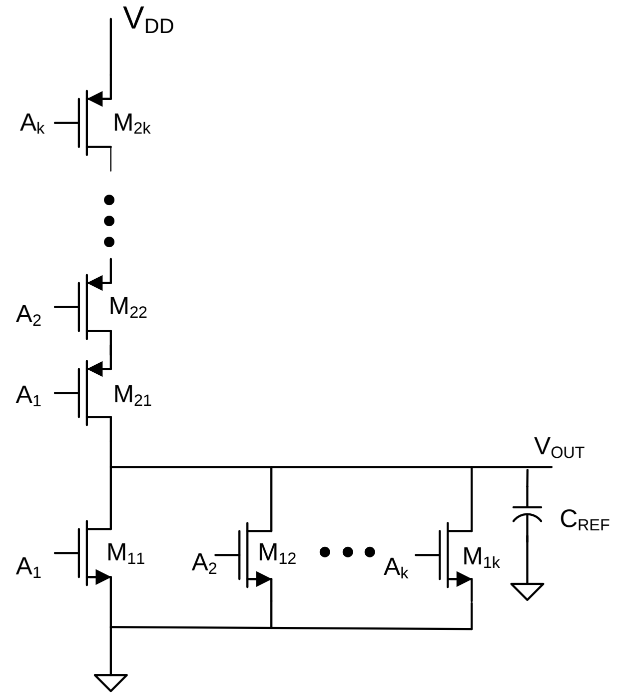
$t_{PROP} = t_{REF}$ (worst case)

Device Sizing

Equal Worst Case Rise/Fall **(and equal to that of ref inverter when driving C_{REF})**

Multiple Input Gates: **k-input NOR**

DERIVATIONS



Wn=?

Wp=?

Input capacitance = ?

FI=?

t_{PROP}=?

$$W_n = W_{MIN}$$

$$W_p = 3kW_{MIN}$$

$$C_{INx} = C_{OX}W_{MIN}L_{MIN} + 3kC_{OX}W_{MIN}L_{MIN} = (3k+1)C_{OX}W_{MIN}L_{MIN} = \left(\frac{3k+1}{4}\right)4C_{OX}W_{MIN}L_{MIN} = \left(\frac{3k+1}{4}\right)C_{REF}$$

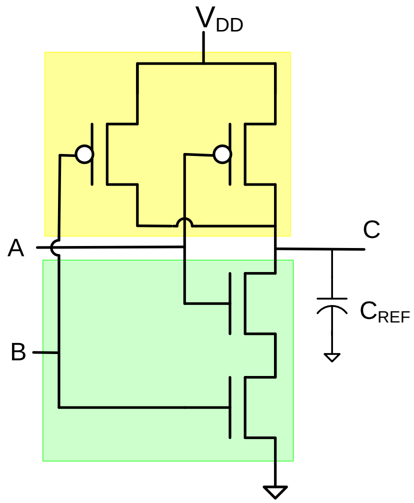
$$FI = \left(\frac{3k+1}{4}\right)C_{REF} \quad \textit{or} \quad FI = \frac{3k+1}{4}$$

$$t_{PROP} = t_{REF}$$

Device Sizing

Equal Worst Case Rise/Fall (and equal to that of ref inverter when driving C_{REF})

Multiple Input Gates: 2-input NAND



Wn=?

DERIVATIONS

Wp=?

Input capacitance = ?

FI=?

t_{PROP}=?

$$W_n=2W_{MIN}$$

$$W_p=3W_{MIN}$$

$$C_{INA}=C_{INB}=2C_{OX}W_{MIN}L_{MIN}+3C_{OX}W_{MIN}L_{MIN}=(5)C_{OX}W_{MIN}L_{MIN}=\left(\frac{5}{4}\right)4C_{OX}W_{MIN}L_{MIN}=\left(\frac{5}{4}\right)C_{REF}$$

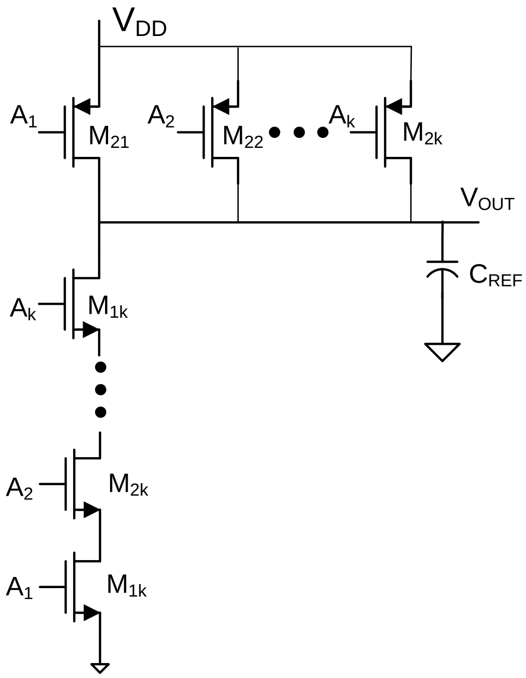
$$FI=\left(\frac{5}{4}\right)C_{REF} \qquad or \qquad FI=\frac{5}{4}$$

$$t_{PROP}=t_{REF}$$

Device Sizing

Equal Worst Case Rise/Fall **(and equal to that of ref inverter when driving C_{REF})**

Multiple Input Gates: **k-input NAND**



DERIVATIONS

Wn=?

Wp=?

Input capacitance = ?

FI=?

t_{PROP}=?

$$W_n = kW_{MIN}$$

$$W_p = 3W_{MIN}$$

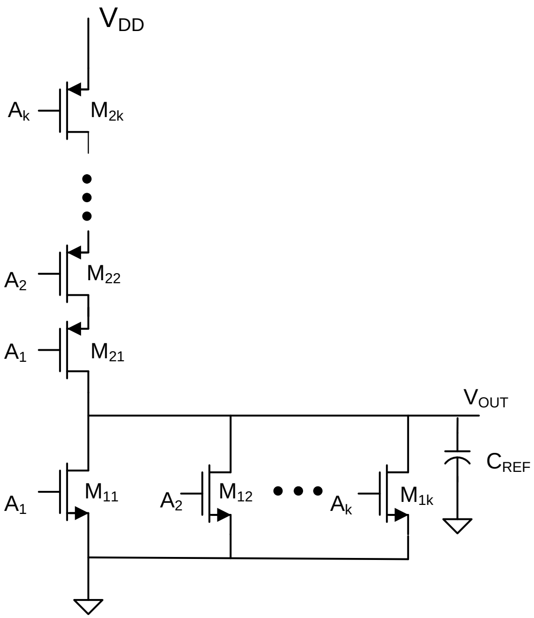
$$C_{INx} = kC_{OX}W_{MIN}L_{MIN} + 3C_{OX}W_{MIN}L_{MIN} = (3+k)C_{OX}W_{MIN}L_{MIN} = \left(\frac{3+k}{4}\right)4C_{OX}W_{MIN}L_{MIN} = \left(\frac{3+k}{4}\right)C_{REF}$$

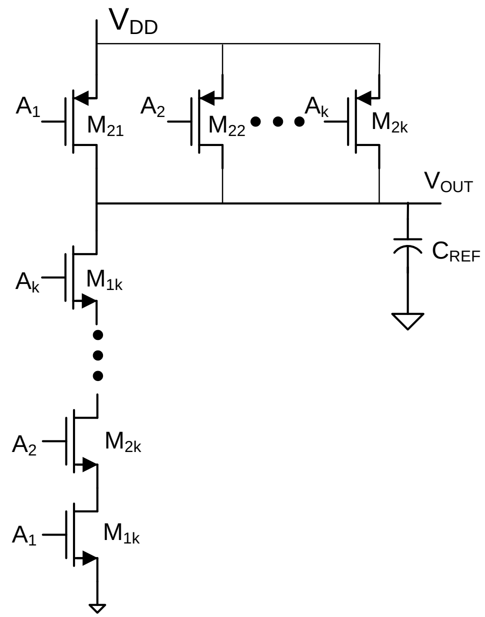
$$FI = \left(\frac{3+k}{4}\right)C_{REF} \quad \textit{or} \quad FI = \frac{3+k}{4}$$

$$t_{PROP} = t_{REF}$$

Device Sizing

Comparison of NAND and NOR Gates





$W_n = W_{MIN}$

$W_p = 3kW_{MIN}$

$C_{INx} = \left(\frac{3k+1}{4}\right) C_{REF}$

$FI = \left(\frac{3k+1}{4}\right) C_{REF}$ *or* $FI = \frac{3k+1}{4}$

$t_{PROP} = t_{REF}$

$W_n = kW_{MIN}$

$W_p = 3W_{MIN}$

$C_{INx} = \left(\frac{3+k}{4}\right) C_{REF}$

$FI = \left(\frac{3+k}{4}\right) C_{REF}$ *or* $FI = \frac{3+k}{4}$

$t_{PROP} = t_{REF}$

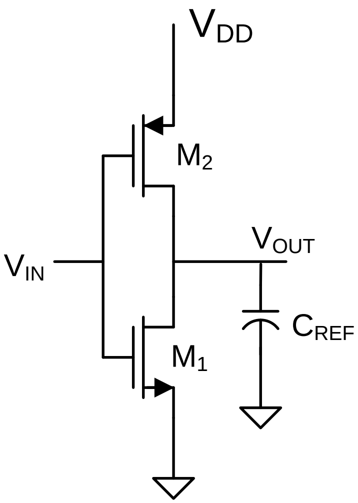
Device Sizing

Equal Worse-Case Rise/Fall Device Sizing Strategy

-- (same as $V_{TRIP}=V_{DD}/2$ for worst case delay in typical process considered in example)

Assume $\mu_n/\mu_p=3$

$L_n=L_p=L_{MIN}$

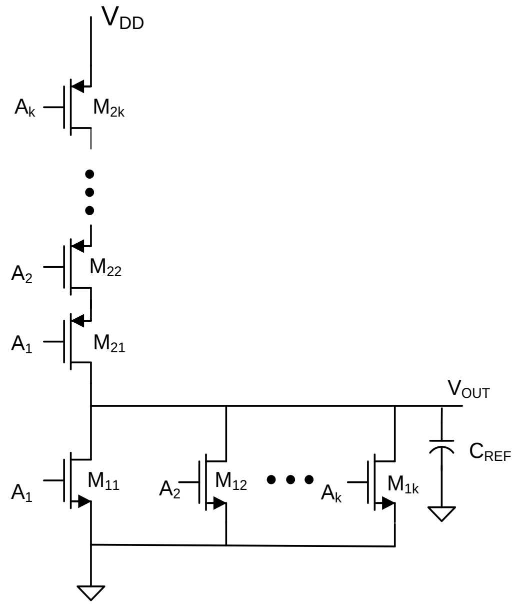


INV

$$W_n=W_{MIN},\ \ W_p=3W_{MIN}$$

$$C_{IN}=C_{REF}$$

FI=1

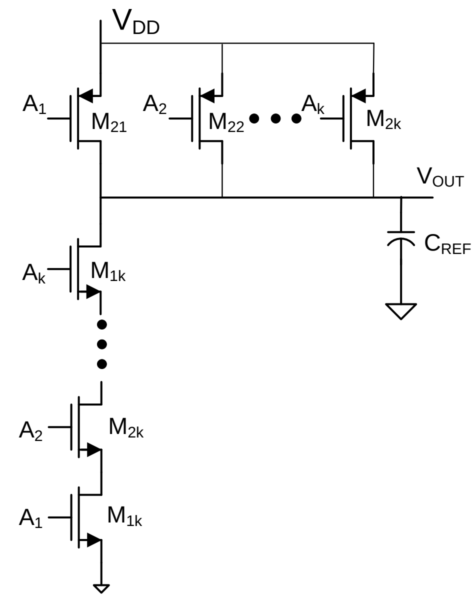


k-input NOR

$$W_n=W_{MIN},\ \ W_p=3kW_{MIN}$$

$$C_{IN}=\left(\frac{3k+1}{4}\right)C_{REF}$$

$$FI=\left(\frac{3k+1}{4}\right)$$



k-input NAND

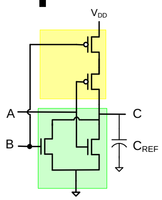
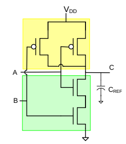
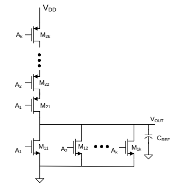
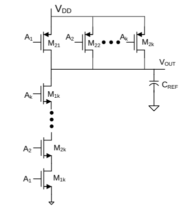
$$W_n=kW_{MIN},\ \ W_p=3W_{MIN}$$

$$C_{IN}=\left(\frac{3+k}{4}\right)C_{REF}$$

$$FI=\left(\frac{3+k}{4}\right)$$

Device Sizing

Multiple Input Gates:

2-input NOR	2-input NAND	k-input NOR	k-input NAND
			

Equal Worst Case Rise/Fall **(and equal to that of ref inverter when driving C_{REF})**

Wn=?
Wp=?

Fastest response (t_{HL} or t_{LH}) = ?

Worst case response (t_{PROP}, usually of most interest)?

Input capacitance (FI) = ?

Minimum Sized **(assume driving a load of C_{REF})**

Wn=Wmin
Wp=Wmin

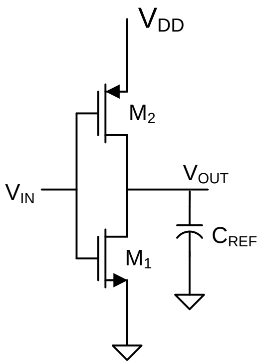
Fastest response (t_{HL} or t_{LH}) = ?

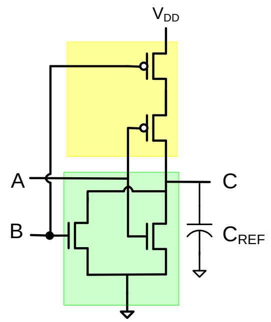
Slowest response (t_{HL} or t_{LH}) = ?

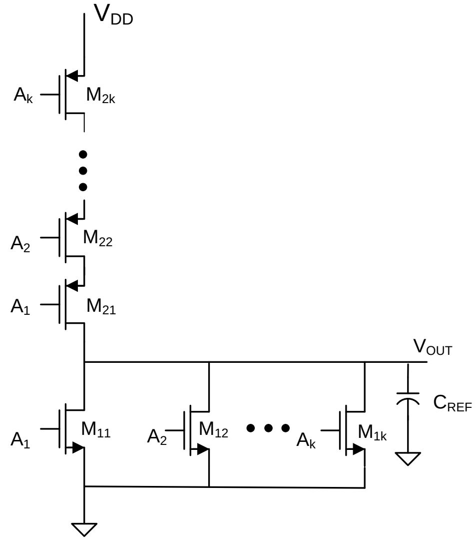
Worst case response (t_{PROP}, usually of most interest)?

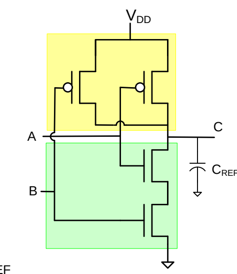
Input capacitance (FI) = ?

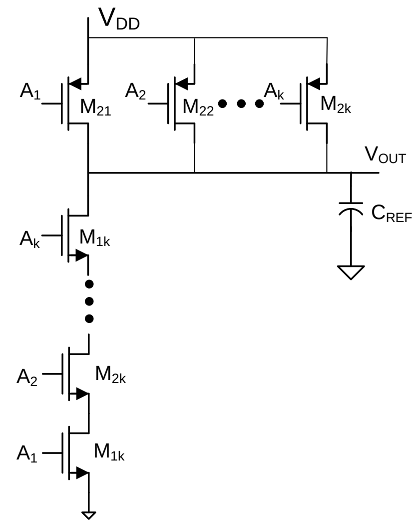
Device Sizing











Minimum Sized **(assume driving a load of C_{REF})** **$W_n = W_{min}$** **$W_p = W_{min}$**

Input capacitance (FI) = ?

$$C_{IN} = C_{OX}W_nL_n + C_{OX}W_pL_p = C_{OX}W_{min}L_{min} + C_{OX}W_{min}L_{min} = 2C_{ox}W_{min}L_{min} = \frac{C_{REF}}{2}$$

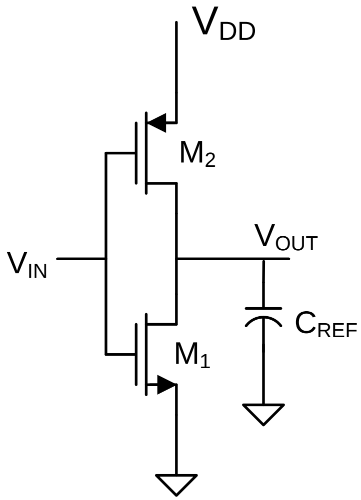
$$FI = \frac{1}{2}$$

Fastest response (t_{HL} or t_{HL}) = ?

Slowest response (t_{HL} or t_{HL}) = ?

Worst case response (t_{PROP}, usually of most interest)?

Device Sizing – minimum size driving C_{REF}



INV

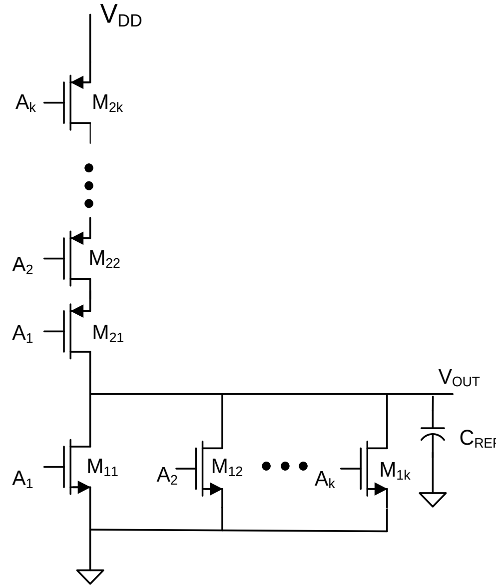
$$t_{PROP} = ?$$

$$t_{PROP} = 0.5t_{REF} + \frac{3}{2}t_{REF}$$

$$t_{PROP} = 2t_{REF}$$

$$FI = \frac{C_{REF}}{2}$$

$$\mathbf{R_{PU}} = \mathbf{R_{PD}} = \mathbf{R_{PDREF}}$$



k-input NOR

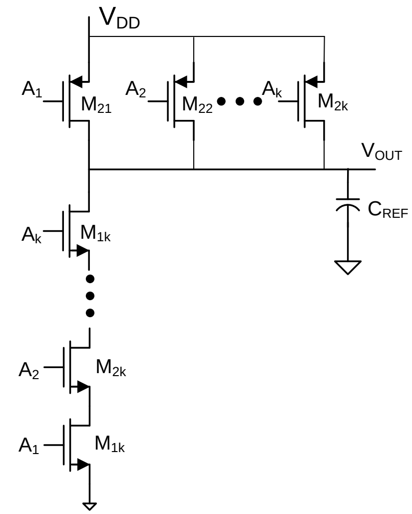
$$t_{PROP} = ?$$

$$t_{PROP} = 0.5t_{REF} + \frac{3k}{2}t_{REF}$$

$$t_{PROP} = \left(\frac{3k+1}{2}\right)t_{REF}$$

$$FI = \frac{C_{REF}}{2}$$

$$\mathbf{R_{PD}} = \mathbf{R_{PDREF}} \quad \mathbf{R_{PU}} = 3k\mathbf{R_{PDREF}}$$



k-input NAND

$$t_{PROP} = ?$$

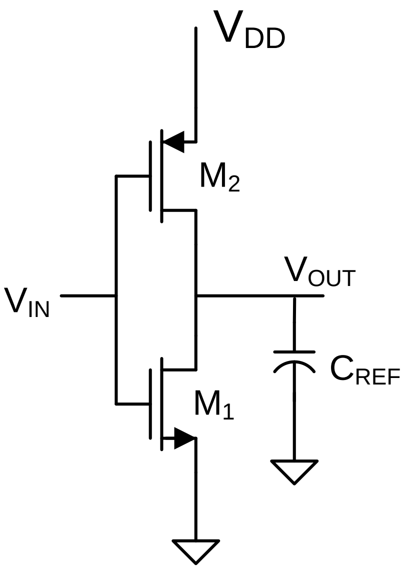
$$t_{PROP} = \frac{3}{2}t_{REF} + \frac{k}{2}t_{REF}$$

$$t_{PROP} = \frac{3+k}{2}t_{REF}$$

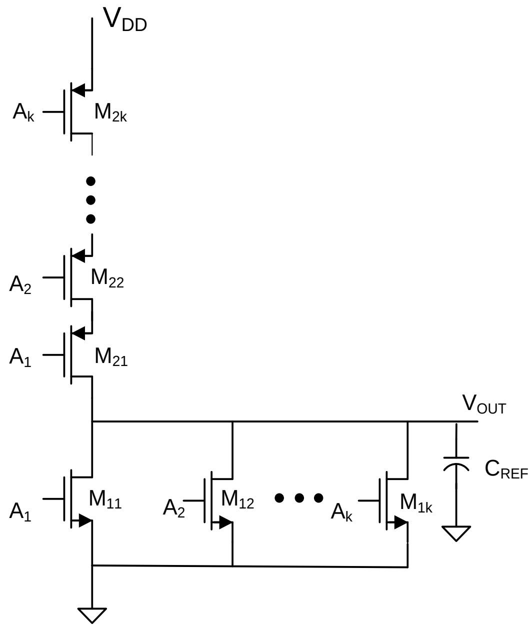
$$FI = \frac{C_{REF}}{2}$$

$$\mathbf{R_{PD}} = 3\mathbf{R_{PDREF}} \quad \mathbf{R_{PU}} = 3\mathbf{R_{PDREF}}$$

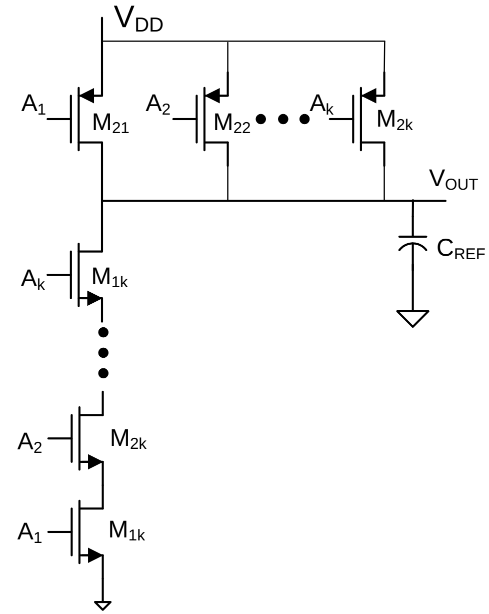
Device Sizing Summary



INV



k-input NOR



k-input NAND

C_{IN} for N_{AND} gates is considerably smaller than for NOR gates for equal worst-case rise and fall times

C_{IN} for minimuim-sized structures is independent of number of inputs and much smaller than C_{IN} for the equal rise/fall time case

R_{PU} gets very large for minimum-sized NOR gate

End of Lecture 40