EE 330
Lecture 6

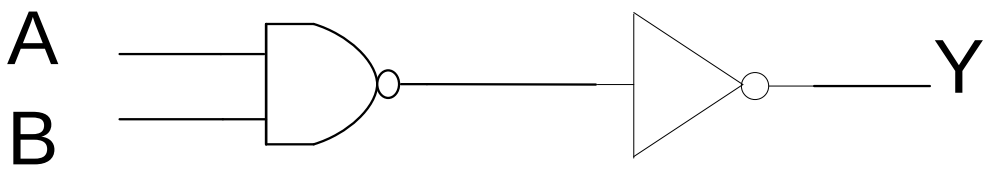
- Pass Transistor Logic
- Improved Switch-Level Model
- Propagation Delay

Pass Transistor Logic

- Improved Switch-Level Model
- Propagation Delay
- Stick Diagrams
- Technology Files

Consider $Y = A \bullet B$

Standard CMOS Implementation

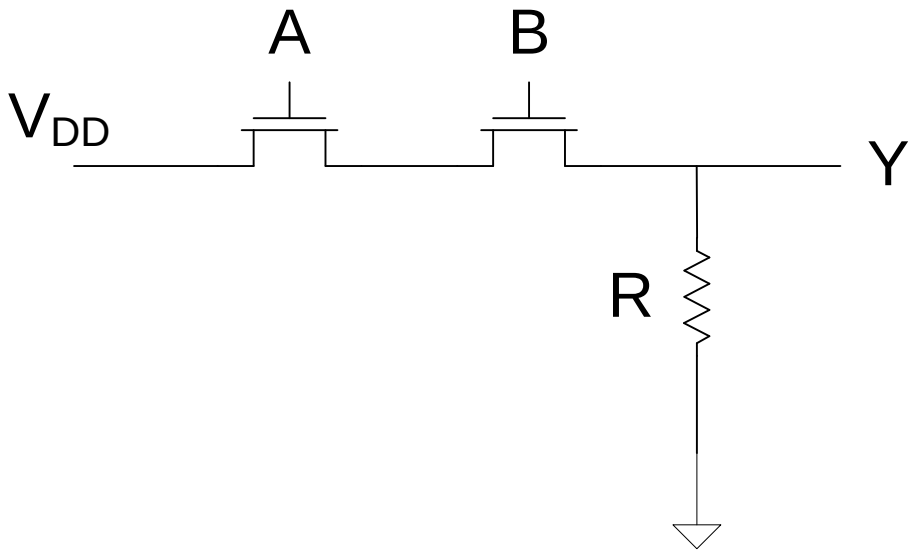


2 levels of Logic

6 Transistors if Basic CMOS Gates are Used

Basic noninverting functions generally require more complexity if basic CMOS gates are used for implementation

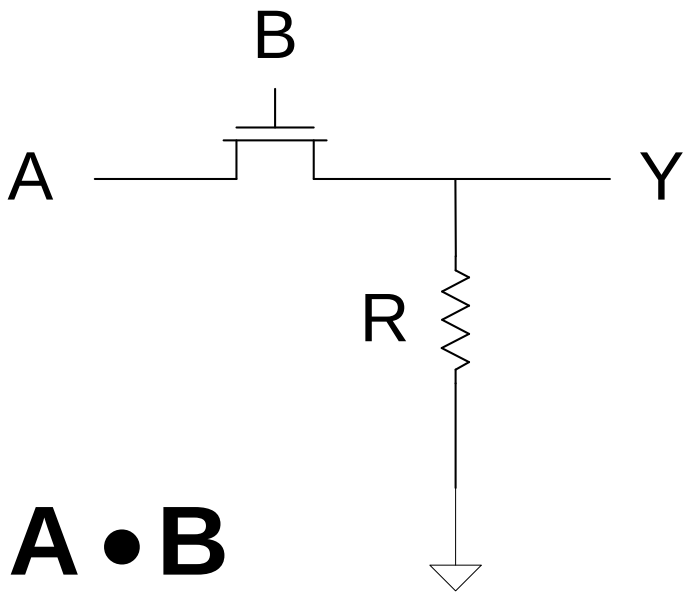
Pass Transistor Logic



$$Y = A \bullet B$$

Requires only 2 transistors rather than 6 for a standard CMOS gate (and a resistor).

Pass Transistor Logic



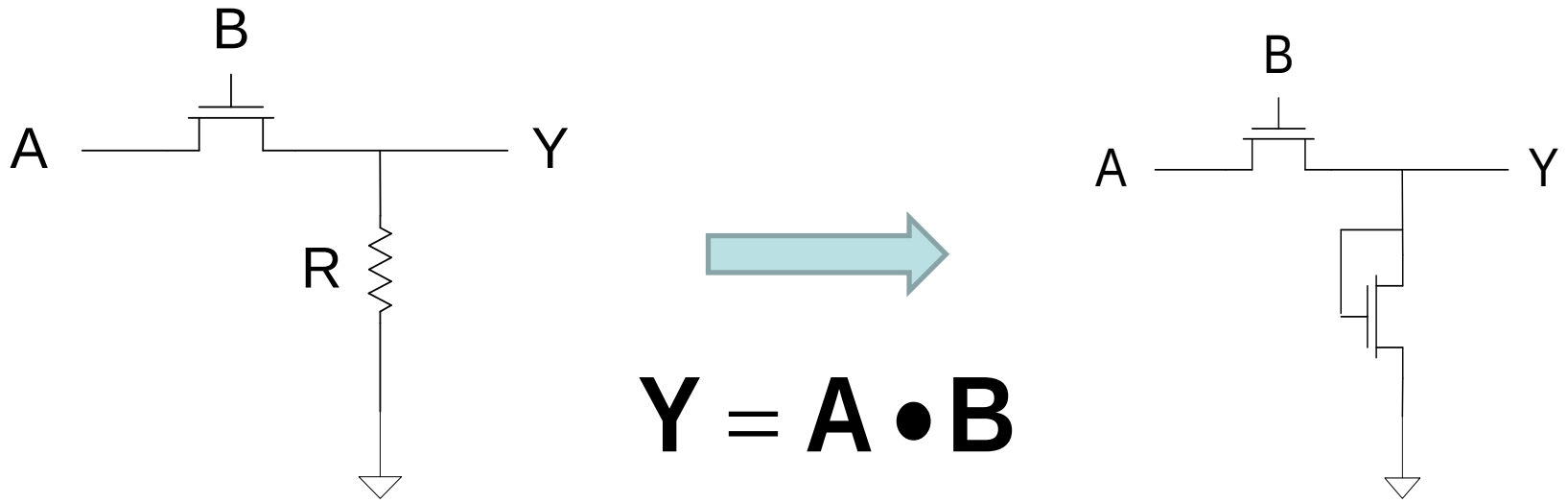
$$Y = A \bullet B$$

Even simpler pass transistor logic implementations are possible

Requires only 1 transistor (and a resistor).

Will see later that the area of a single practical resistor for this circuit may be comparable to that needed for hundreds or even thousands of transistors

Pass Transistor Logic

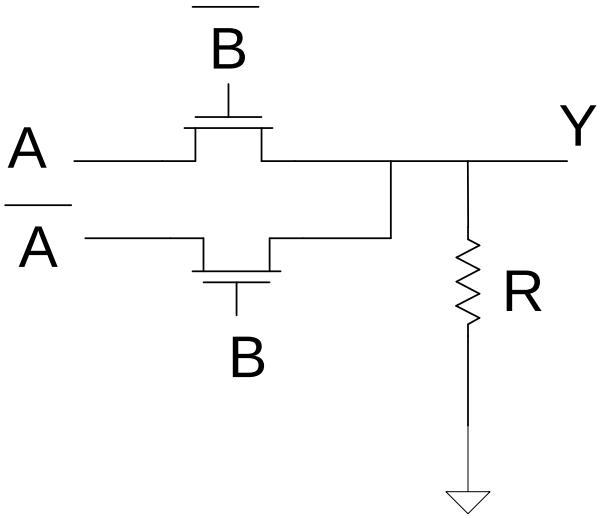


$$Y = A \bullet B$$

- **May be able to replace resistor with transistor (one of several ways shown)**
- **But high logic level can not be determined with existing device model (or even low logic level for circuit on right)**
- **Power dissipation can not be determined with existing device model for circuit on right**

Better device model is needed (Power? Signal Swing? Speed?)

Pass Transistor Logic

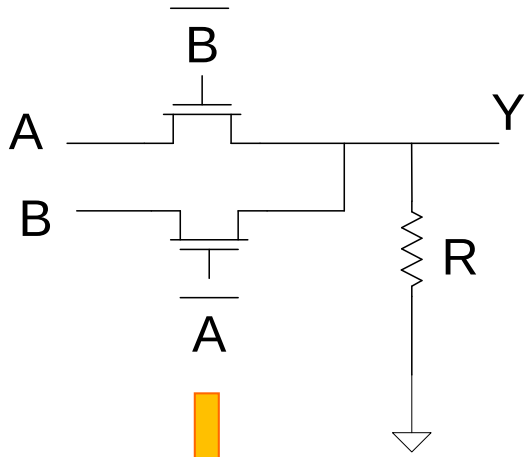


$$Y = A \oplus B$$

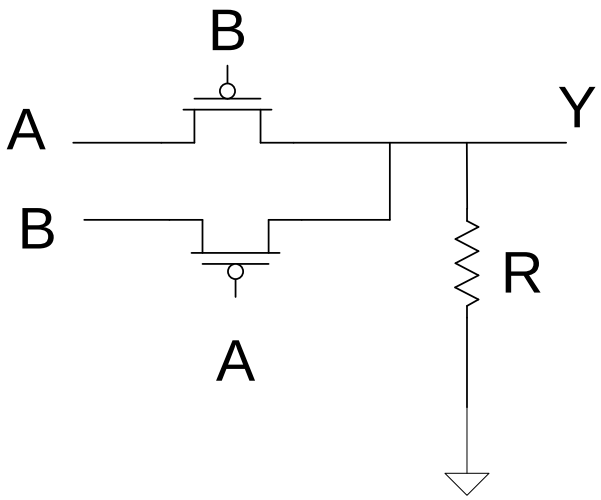
6 transistors, 1 resistor, two levels of logic

(the 4 transistors in the two inverters are not shown)

Pass Transistor Logic



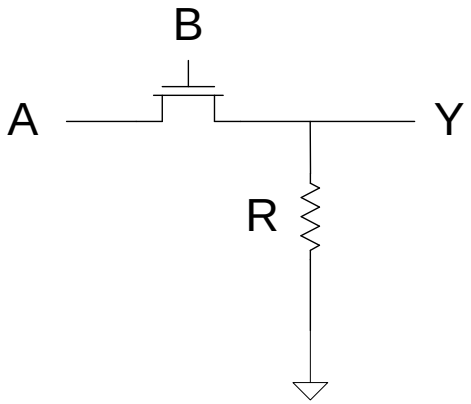
$$Y = A \oplus B$$



$$Y = A \oplus B$$

2 transistors, 1 resistor, one level of logic

Pass Transistor Logic



$$Y = A \bullet B$$

Requires only 1 transistor (and a resistor)

- **Pass transistor logic can offer significant reductions in complexity for some functions (particularly noninverting)**
- **Resistor may require more area than several hundred or even several thousand transistors**
- **Signal levels may not go to V_{DD} or to 0V**
- **Static power dissipation may not be zero**
- **Signals may degrade unacceptably if multiple gates are cascaded**
- **"resistor" often implemented with a transistor to reduce area but signal swing and power dissipation problems still persist**
- **Pass transistor logic is widely used**

Logic Design Styles

- Several different logic design styles are often used throughout a given design (3 considered thus far)
  - Static CMOS
  - Complex Logic Gates
  - Pass Transistor Logic
- The designer has complete control over what is placed on silicon and governed only by cost and performance
- New logic design strategies have been proposed recently and others will likely emerge in the future
- The digital designer needs to be familiar with the benefits and limitations of varying logic styles to come up with a good solution for given system requirements

- Pass Transistor Logic
- Improved Switch-Level Model
- Propagation Delay
- Stick Diagrams
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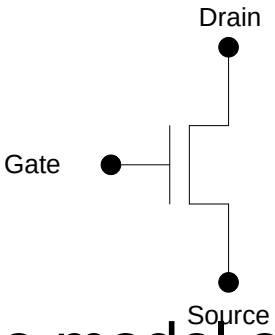
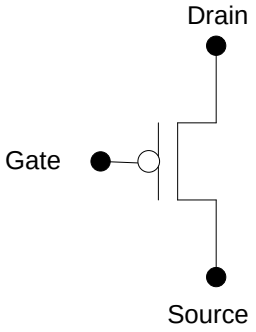
MOSFET Modeling

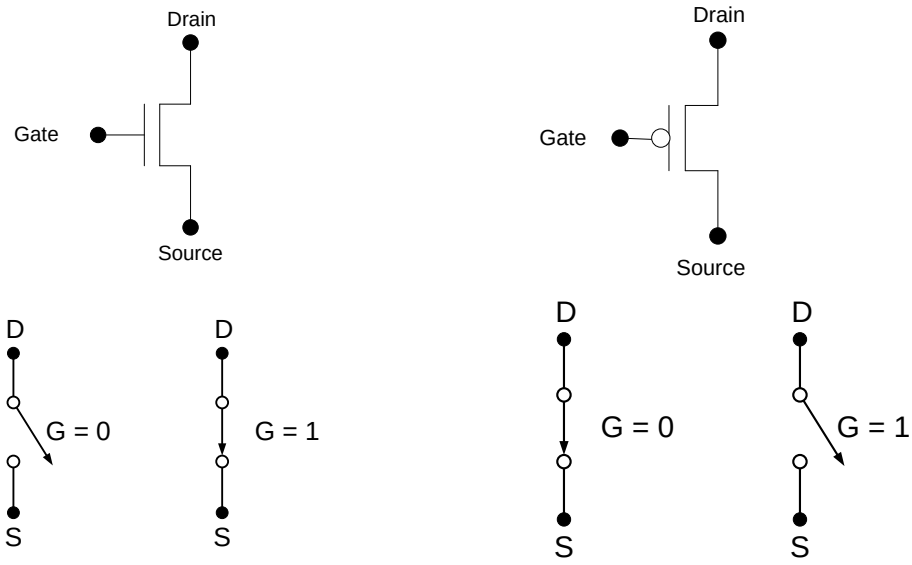




- Simple model of MOSFET was developed (termed switch-level model)
- Simple gates designed in CMOS Process were introduced
  - Some have zero power dissipation
  - Some have or appeared to have rail to rail logic voltage swings
  - All appeared to be Infinitely fast
  - Logic levels of some can not be predicted with simple model
  - Simple model is not sufficiently accurate to provide insight relating to some of these properties
- MOSFET modeling strategy
  - hierarchical model structure will be developed
  - generally use simplest model that can be justified

MOS Transistor Models

1, Switch-Level model



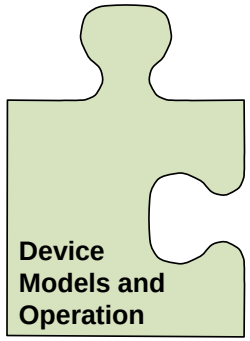
Advantages:

Simple, does not require understanding of semiconductor properties, does not depend upon process, adequate for understanding basic operation of many digital circuits

Limitations:

Does not provide timing information (surfaced when looking at static CMOS circuits, and several others that have not yet become apparent from the applications that have been considered) and can not support design of "resistor" used in Pass Transistor Logic

Improved Device Models



With the simple switch-level model, it was observed that basic static CMOS logic gates have the following three properties:

- **Rail to rail logic swings**
- **Zero static power dissipation in both Y=1 and Y=0 states**
- **Arbitrarily fast (too good to be true? will consider again with better model)**

It can be shown that the first two properties are nearly satisfied in actual fabricated circuits with p-channel/n-channel PU/PD logic but though the circuits are fast, they are observably not arbitrarily fast

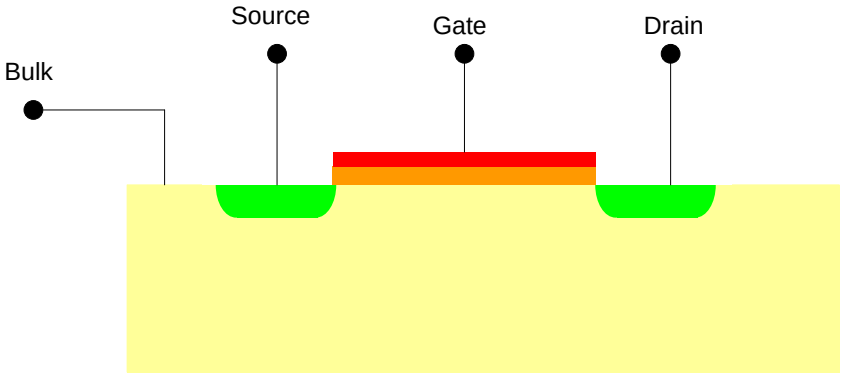
None of these properties are observed for some logic styles such as Pass Transistor Logic

Will now extend switch-level model to predict speed of basic gates in static CMOS and logic levels and power dissipation in PTL

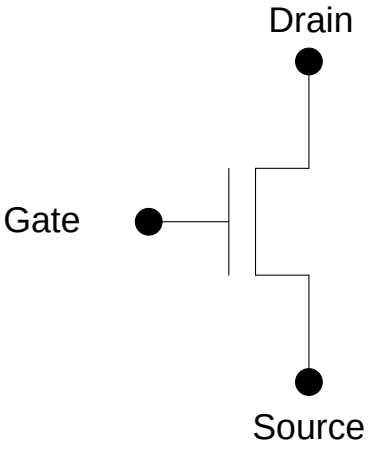
Recall

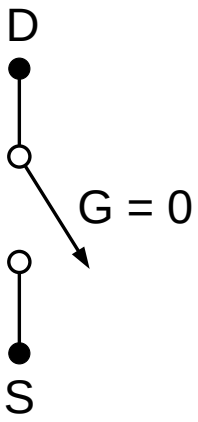
MOS Transistor

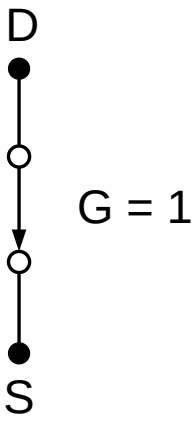
Qualitative Discussion of n-channel Operation



n-channel MOSFET



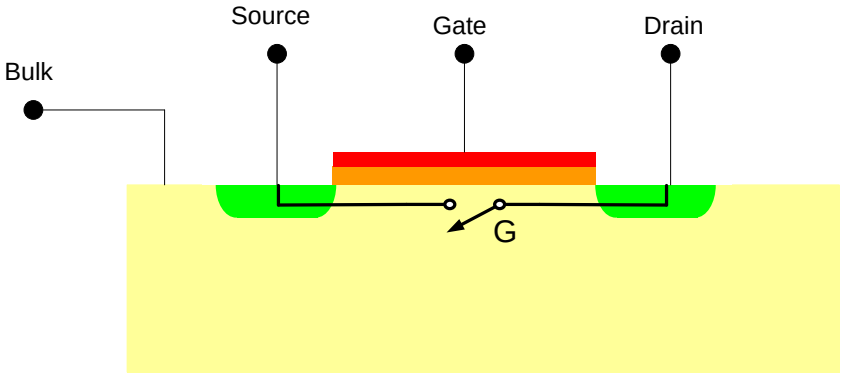




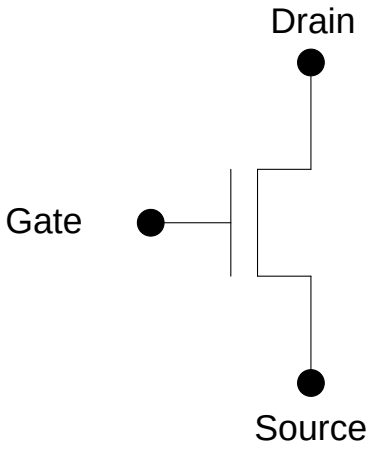
This was the first model introduced and was termed the basic switch-level mode

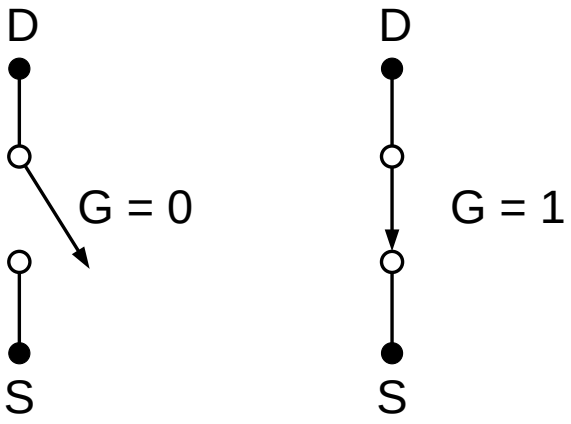
MOS Transistor

Qualitative Discussion of n-channel Operation



n-channel MOSFET

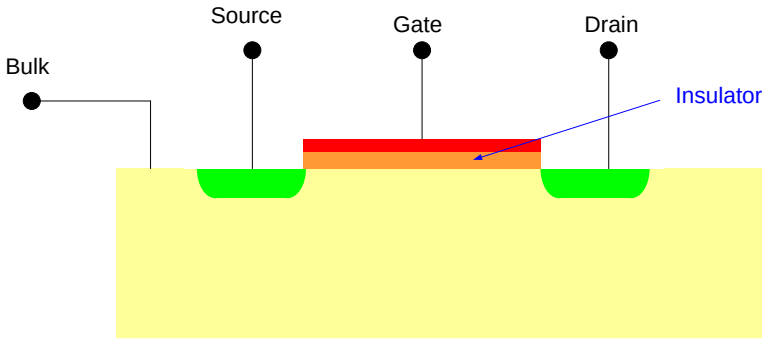




Conceptual view of basic switch-level model

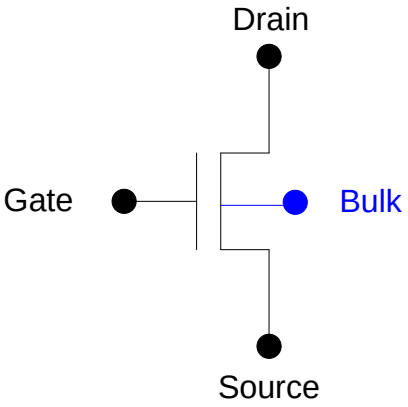
MOS Transistor

Qualitative Discussion of n-channel Operation

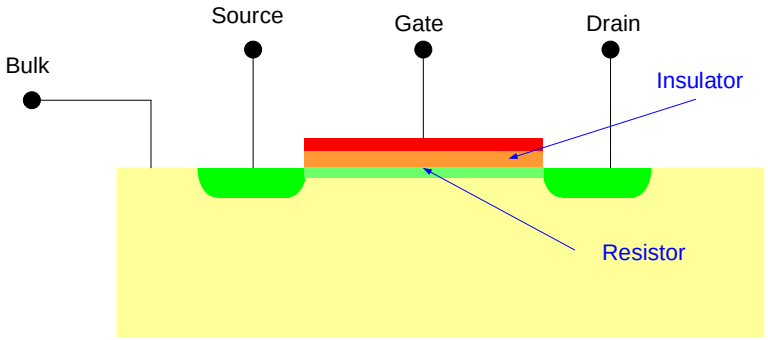


n-channel MOSFET

For V_{GS} small



MOSFET actually 4-terminal device



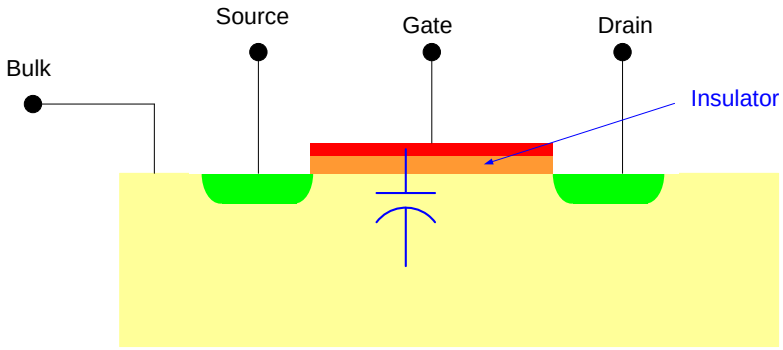
n-channel MOSFET

For V_{GS} large

- Region under gate termed the “channel”
- When “resistor” is electrically created, it is termed an “inversion region”

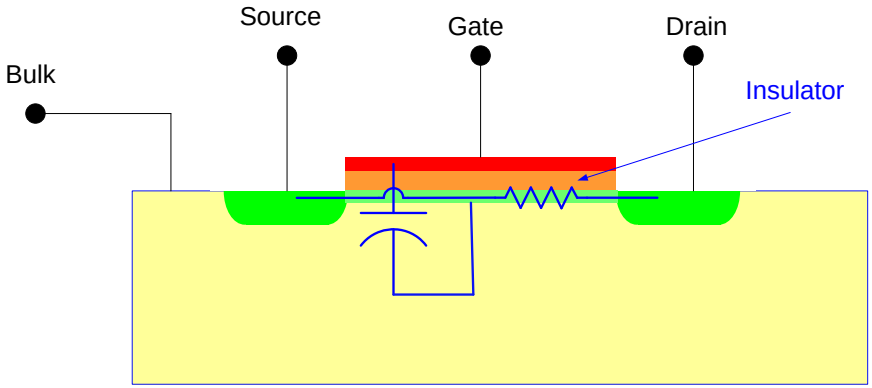
MOS Transistor

Qualitative Discussion of n-channel Operation



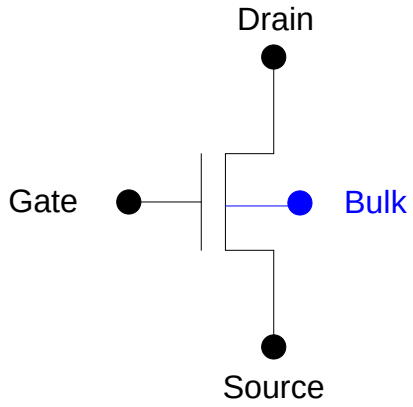
n-channel MOSFET

For V_{GS} small



n-channel MOSFET

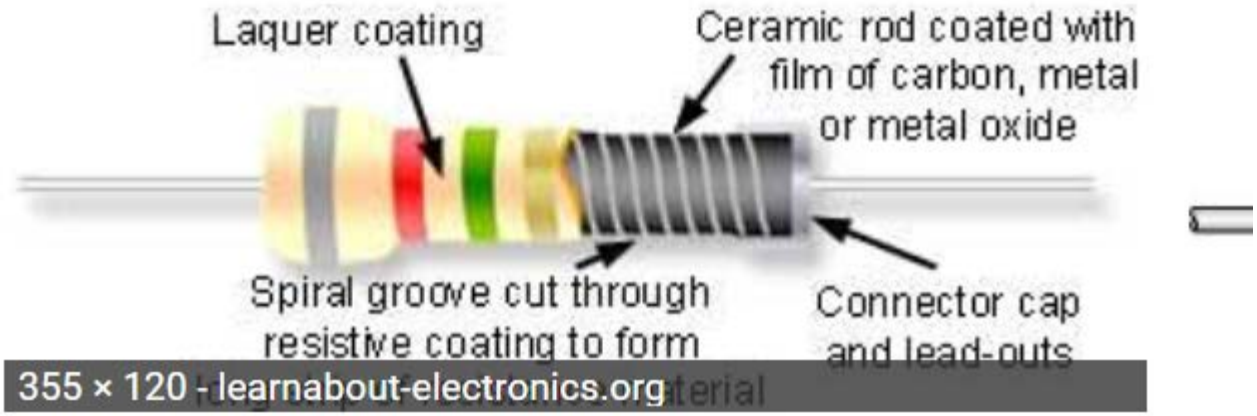
For V_{GS} large



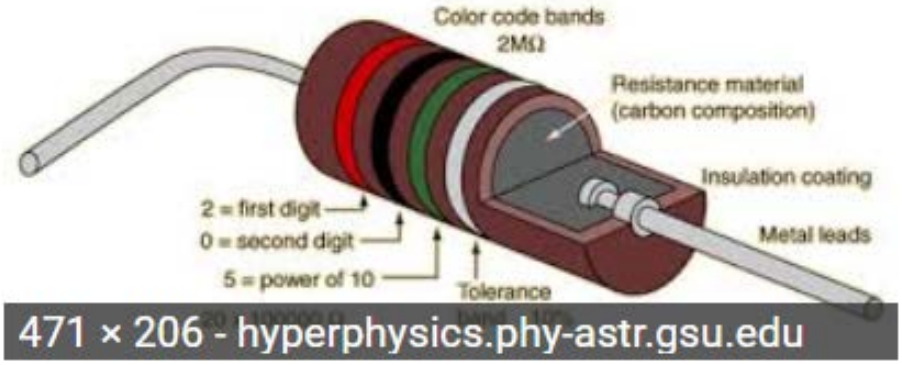
- Electrically created inversion layer forms a “thin “film” resistor
- Capacitance from gate to channel region is distributed
- Lumped capacitance much easier to work with

Discrete Resistors often use thin films too though not electrically created

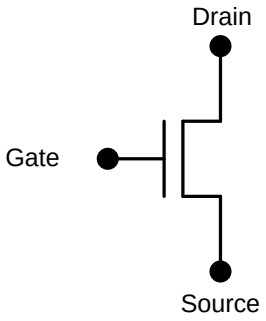
- **Thin-film spiral wound**

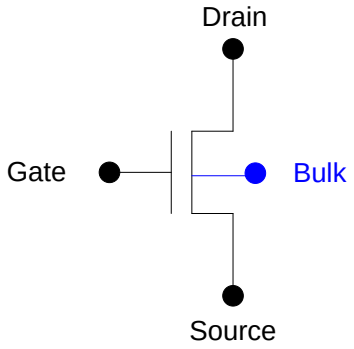


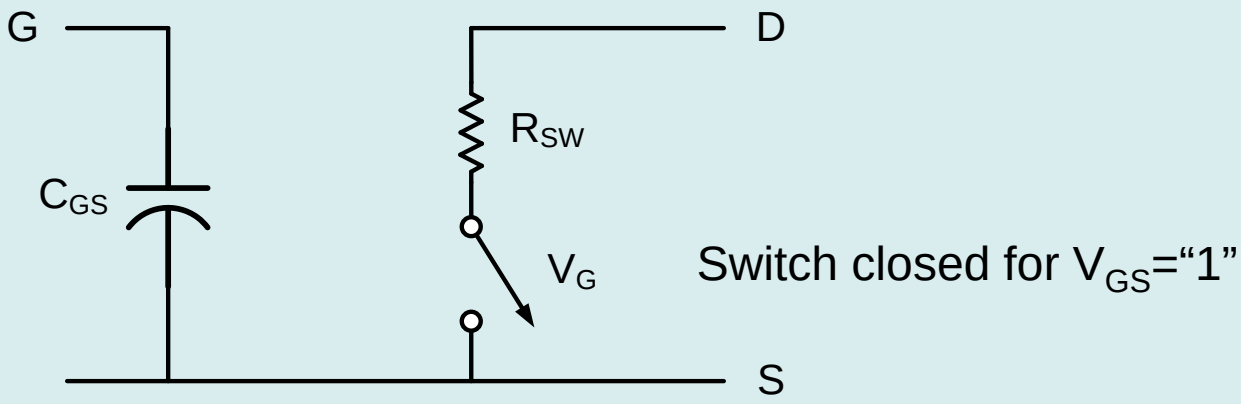
- **Carbon composition**



Improved Switch-Level Model



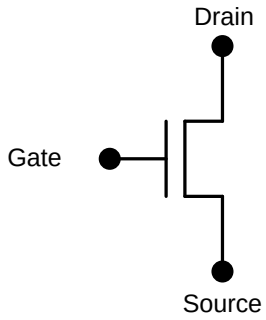




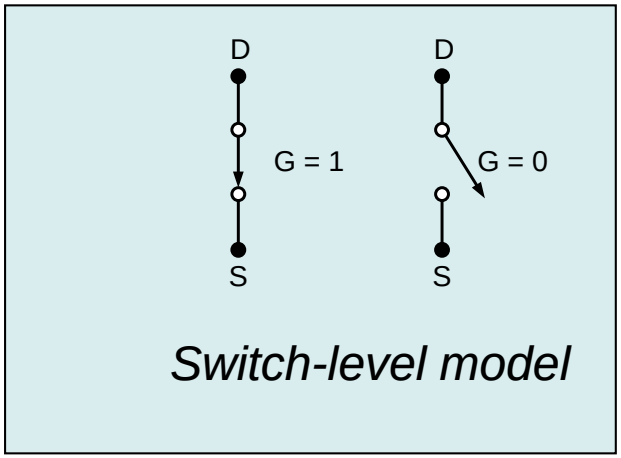
Switch-level model including gate capacitance and channel resistance

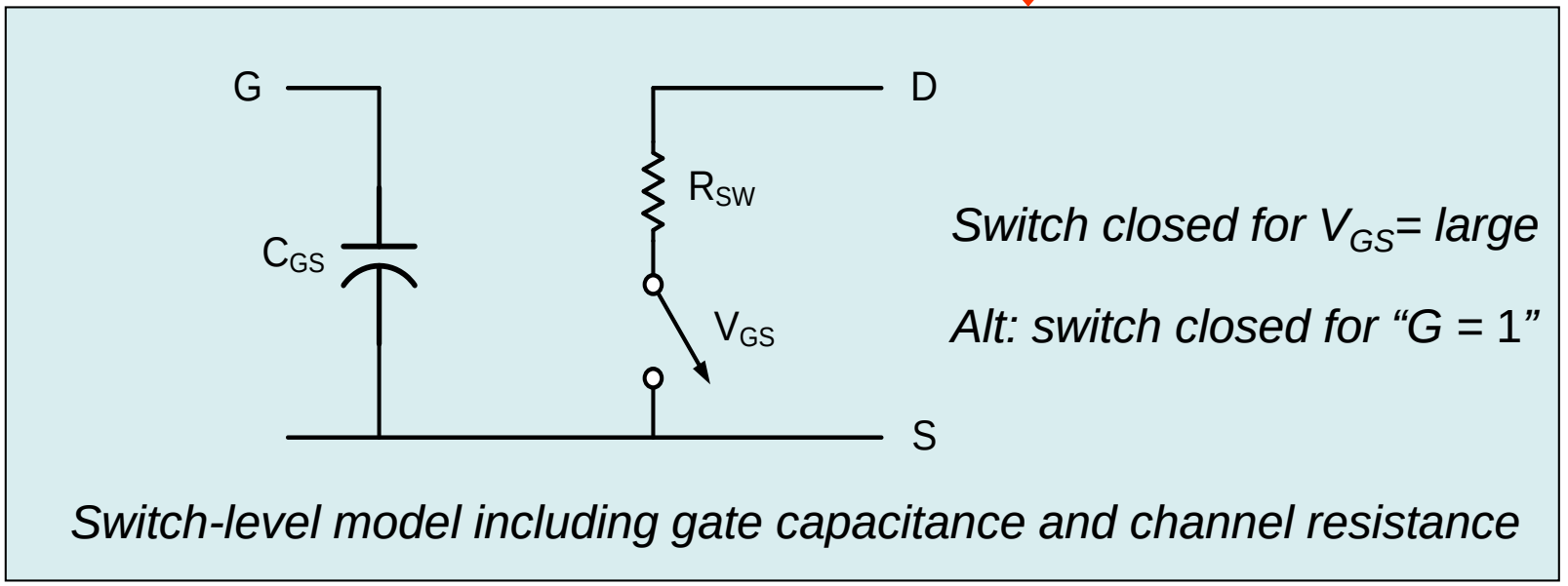
- Connect the gate capacitance to the source to create lumped model
- Still neglect bulk connection

Improved Switch-Level Model

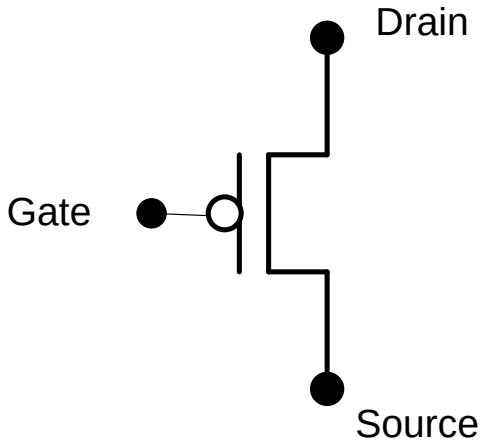


n-channel

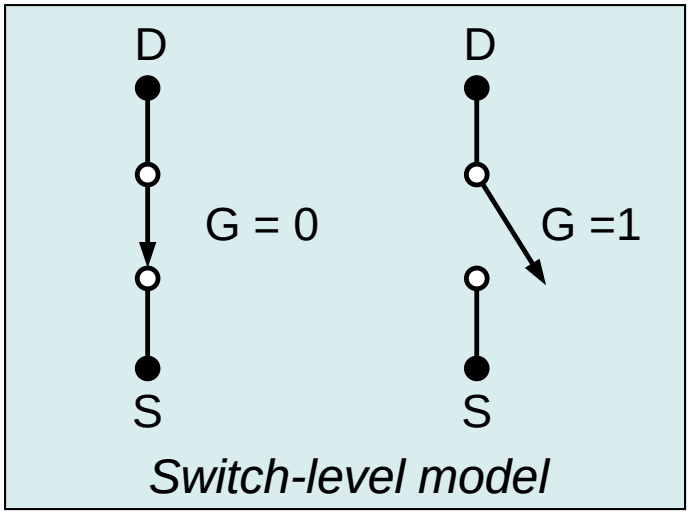




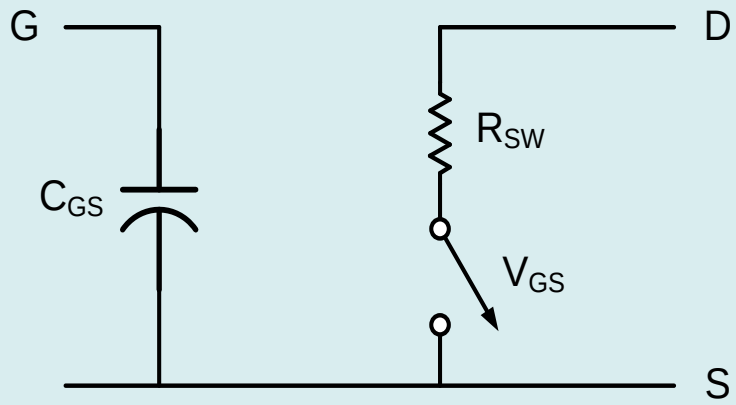
Improved Switch-Level Model



p-channel



Switch-level model

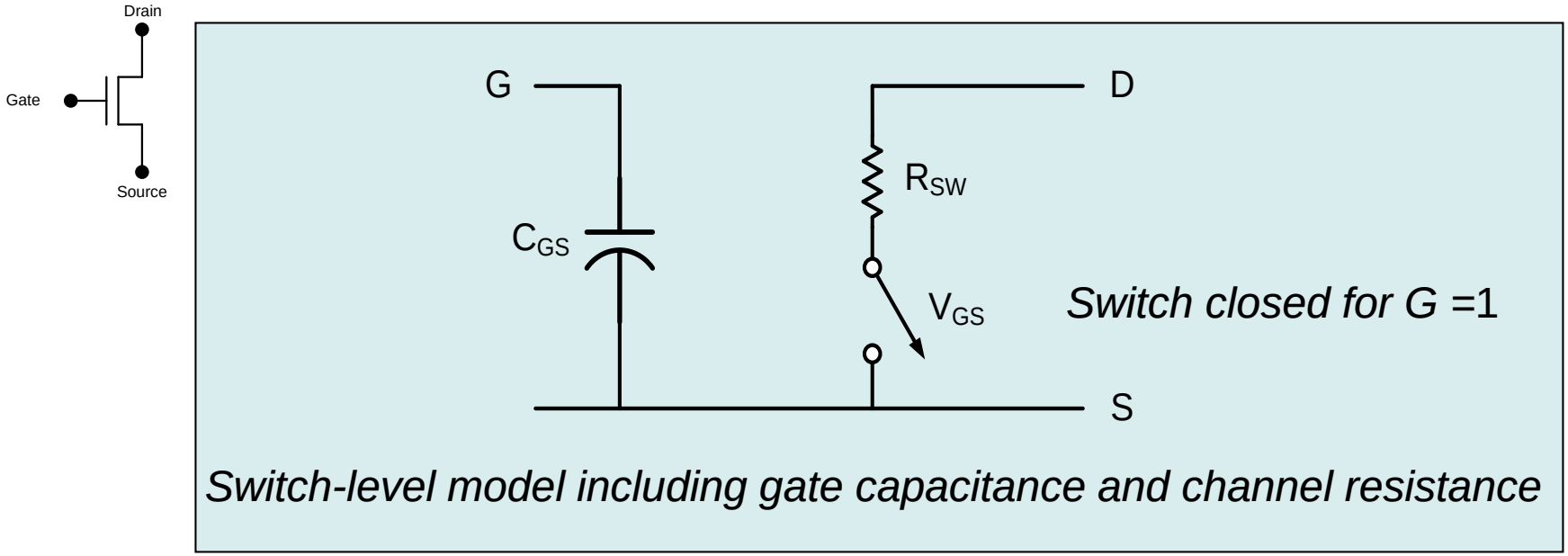


Switch closed for V_{GS} large and neg

Alt: If S near V_{DD}, closed for G=0

Switch-level model including gate capacitance and channel resistance

Improved Switch-Level Model



Switch-level model including gate capacitance and channel resistance

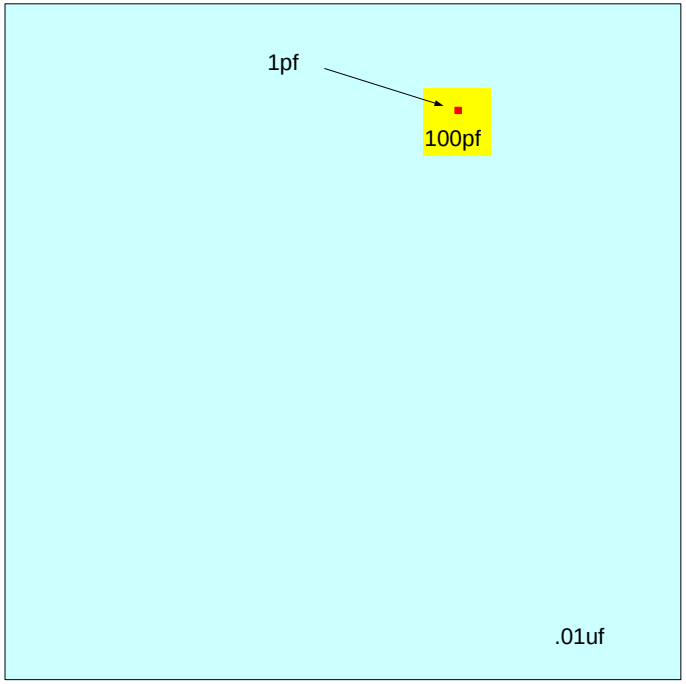
C_{GS} and R_{SW} dependent upon device sizes and process

For minimum-sized devices in a 0.5u process

$$\mathbf{C_{GS} \cong 1.5fF} \qquad \mathbf{R_{sw}} \cong \begin{cases} \mathbf{2K\Omega \;\; n-channel} \\ \mathbf{6K\Omega \;\; p-channel} \end{cases}$$

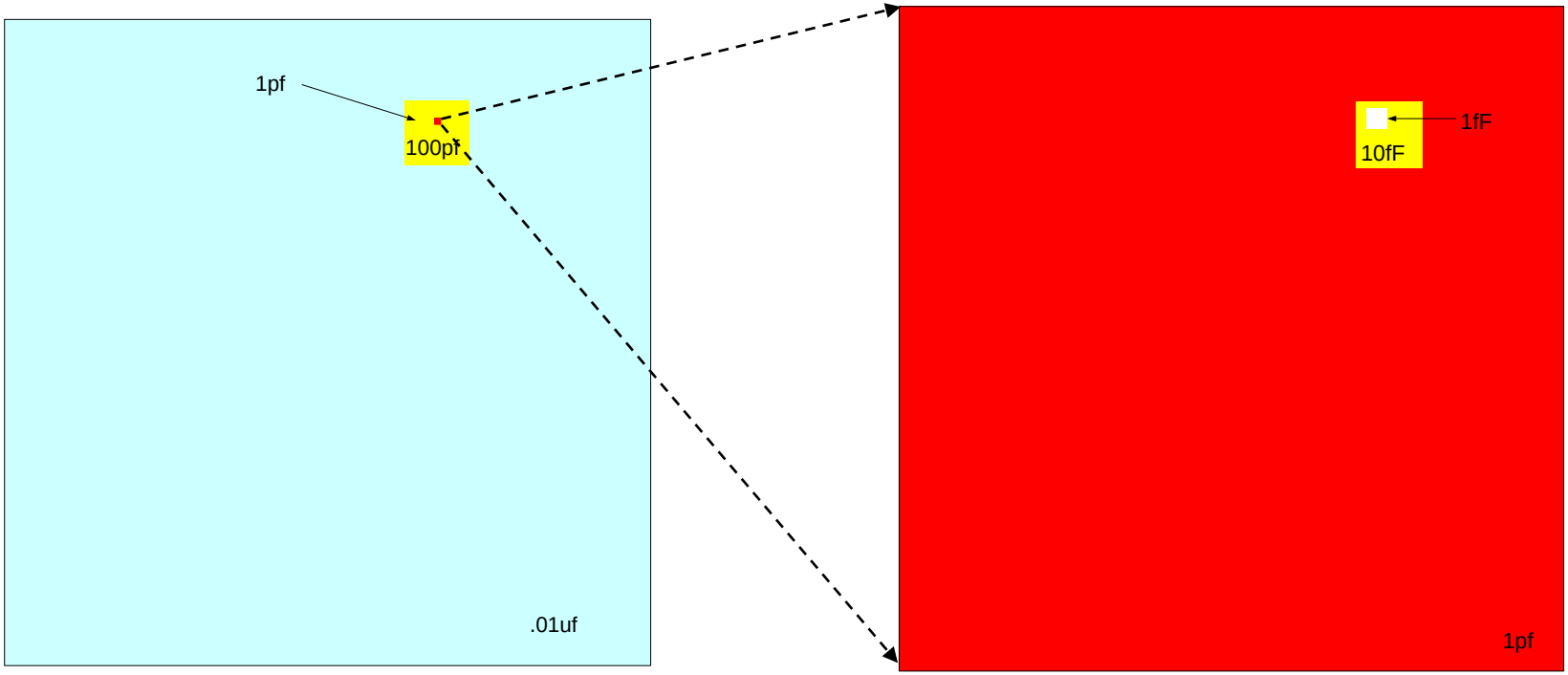
Considerable emphasis will be placed upon device sizing to manage C_{GS} and R_{SW}

Is a capacitor of 1.5fF small enough to be neglected?



Area allocations shown to relative scale:

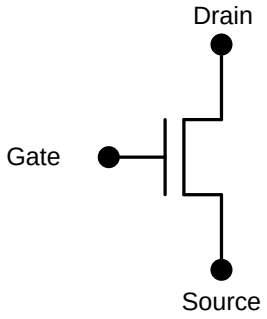
Is a capacitor of 1.5fF small enough to be neglected?



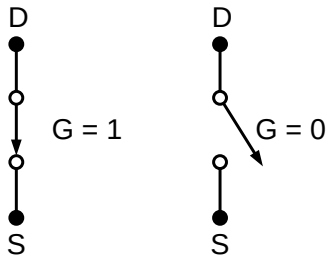
Area allocations shown to relative scale:

- **Not enough information at this point to determine whether this very small capacitance can be neglected**
- **Will answer this important question later**

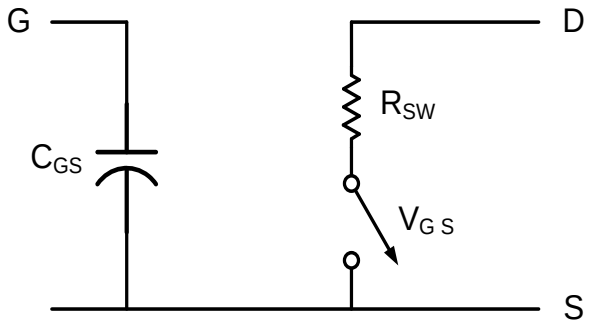
Model Summary (for n-channel)



1, Switch-Level model



2, Improved switch-level model



Switch closed for V_{GS}= large

Switch open for V_{GS}= small

Other models will be developed later

- Pass Transistor Logic
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- Propagation Delay
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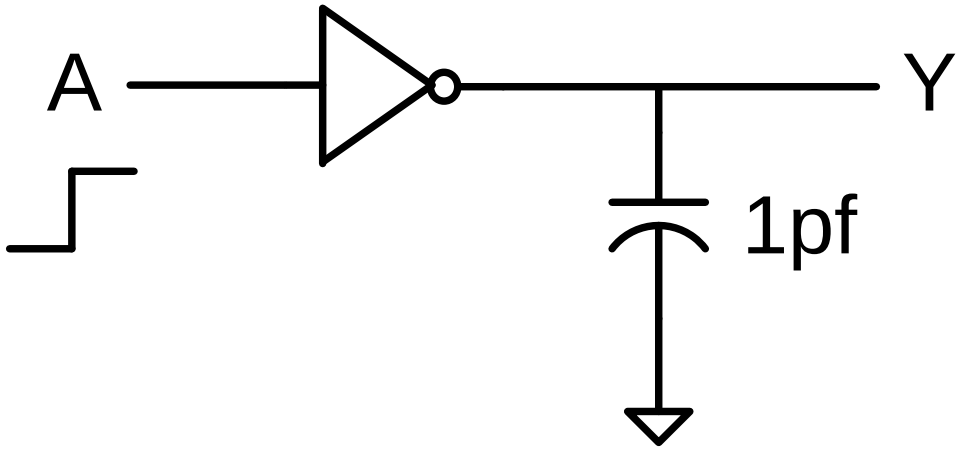
Example

What are t_{HL} and t_{LH}?

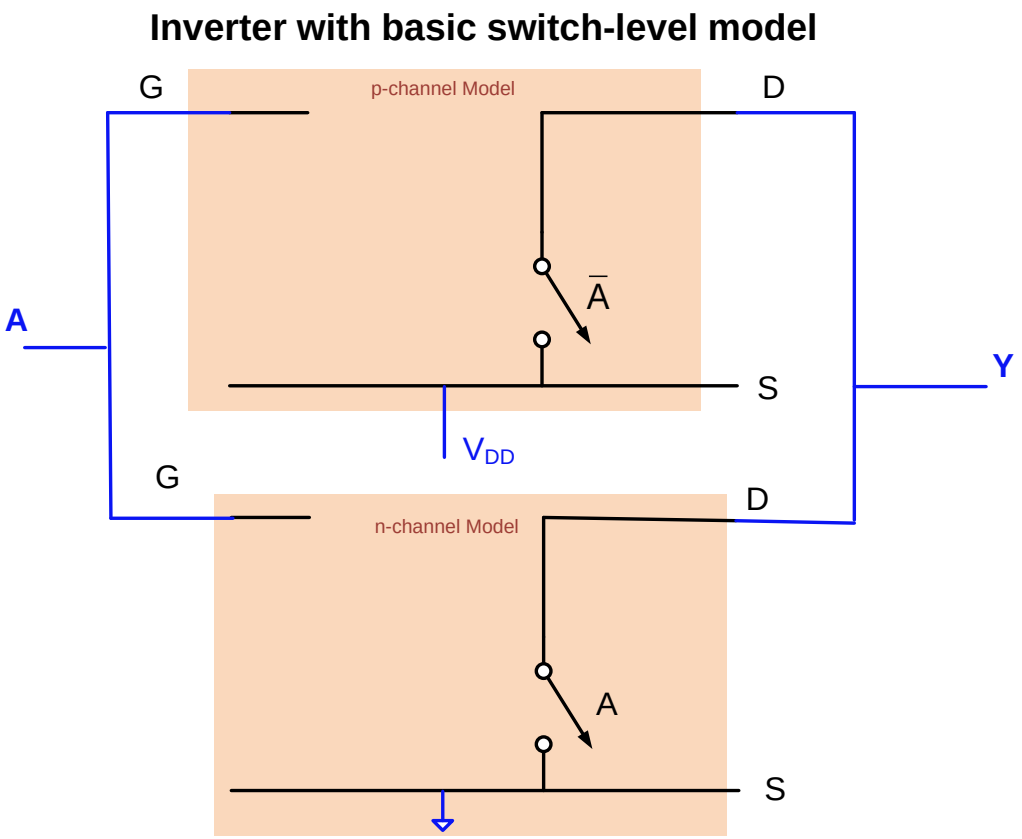
Assume V_{DD}=5V



With basic switch level model ?

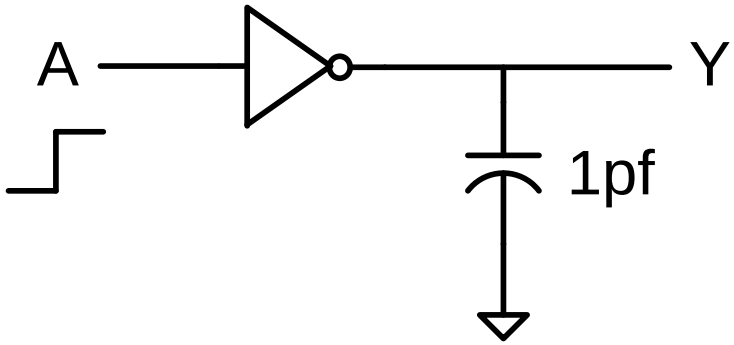
With improved switch level model ?

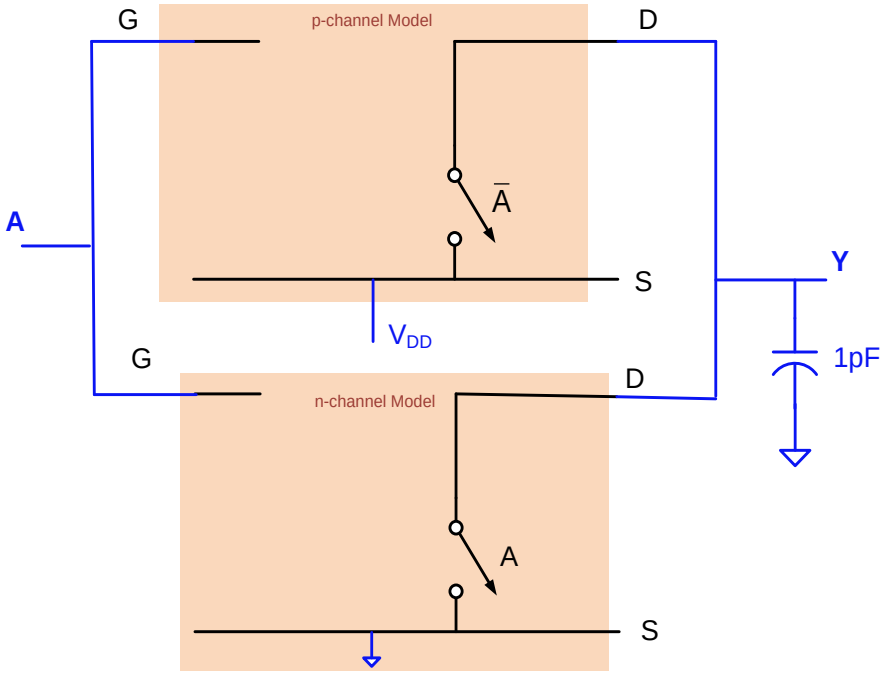
Example


Inverter with basic switch-level model
G
p-channel Model
D
$\overline{A}$
A
S
Y
V_{DD}
G
D
n-channel Model
A
S

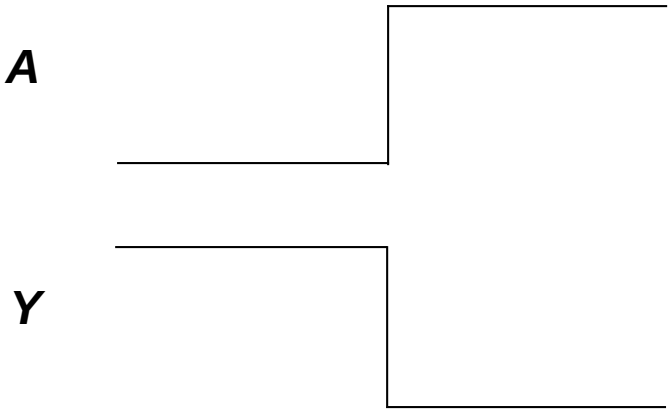
Example

What are t_{HL} and t_{LH}?





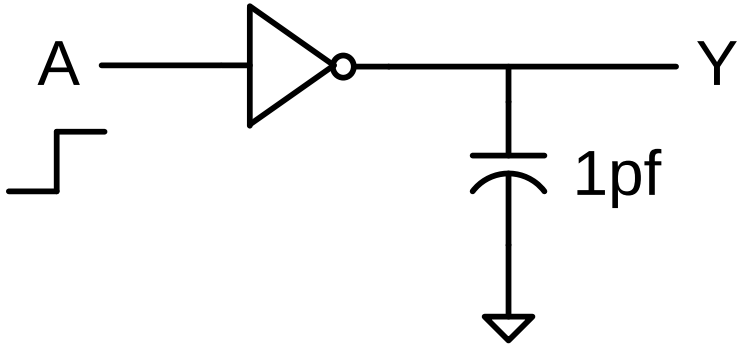
With basic switch level model



$t_{HL}=t_{LH}=0$

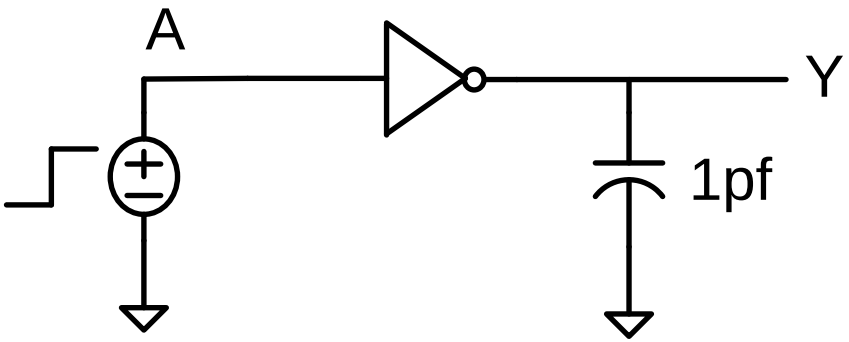
Example (cont)

With simple switch-level model $t_{HL}=t_{LH}=0$



Inverter

With improved model ?

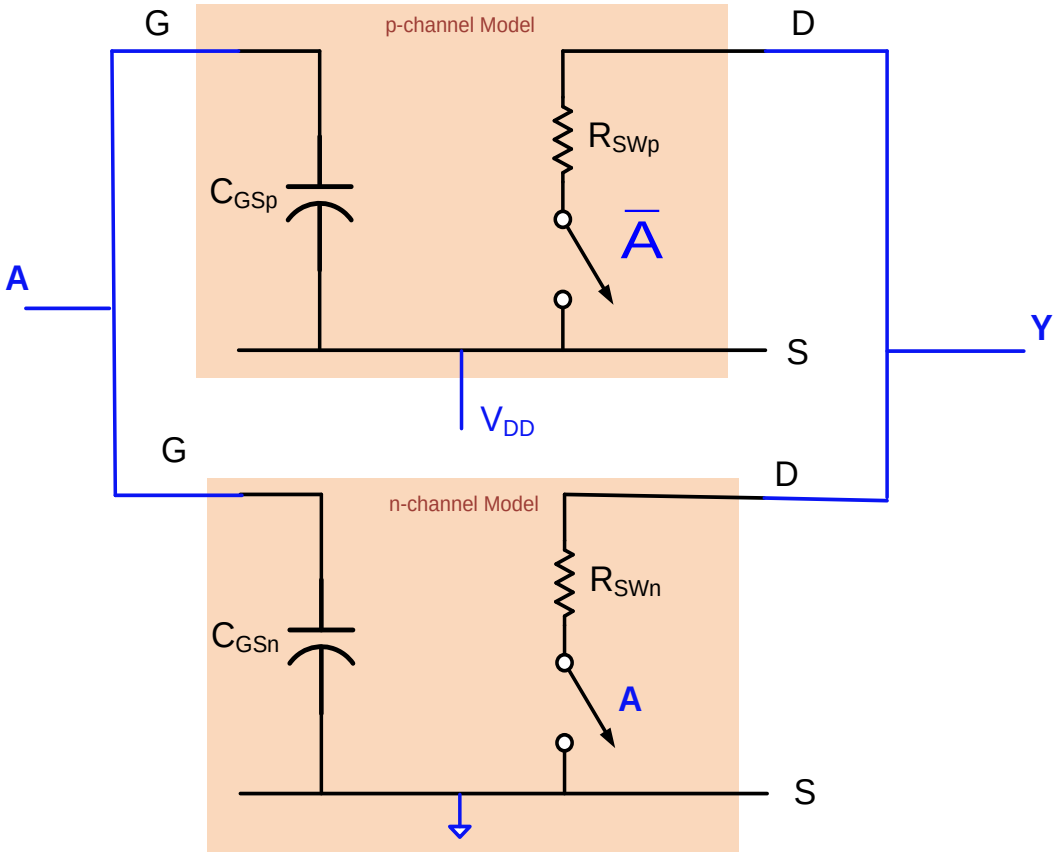


Example (cont)

Inverter with improved model

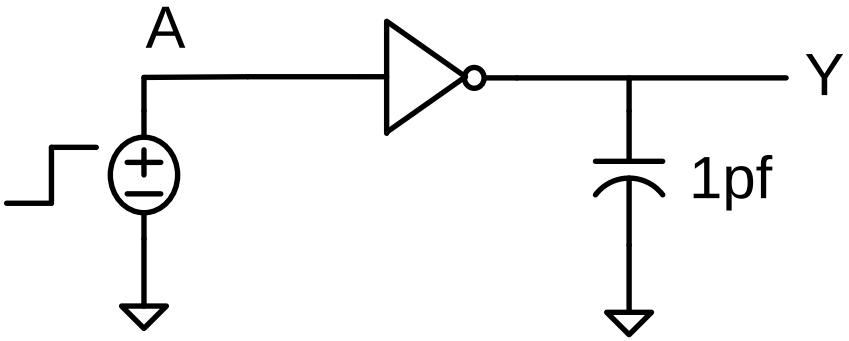
Inverter

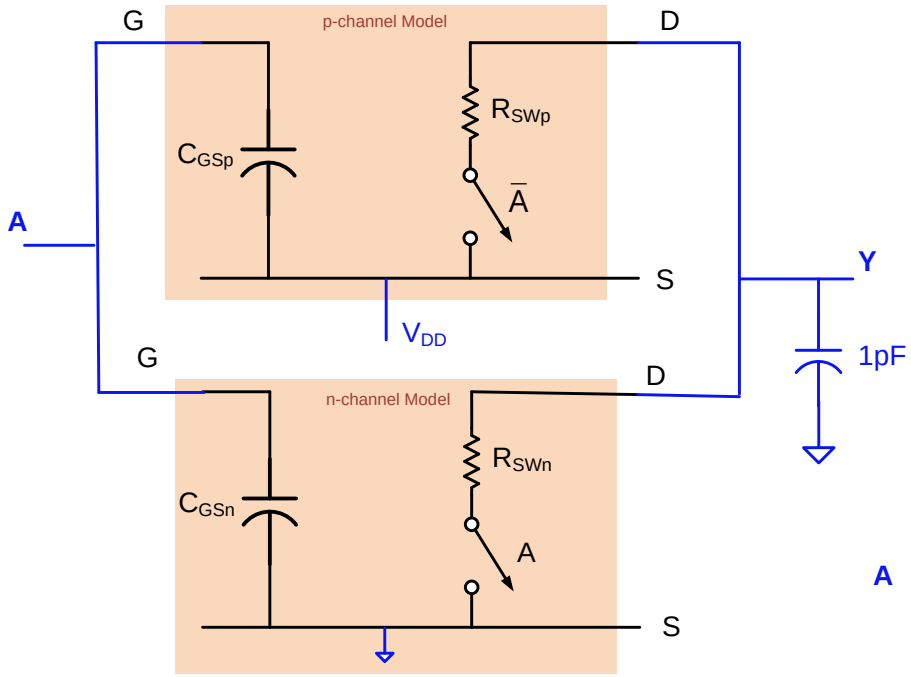
Inverter with Improved Model



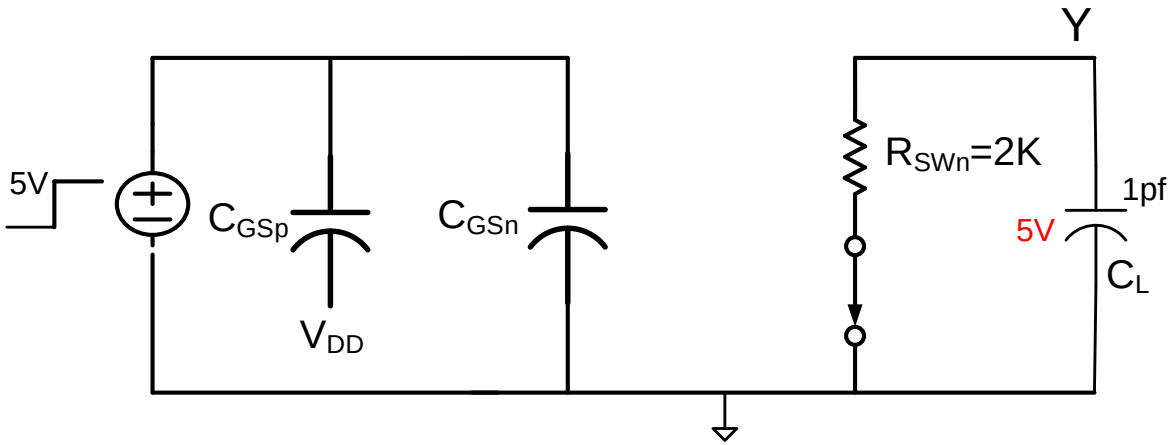
Example (cont)

With improved model $t_{HL}=?$





To initiate a HL output transisition, assume Y has been in the high state for a long time and lower switch closes at time t=0

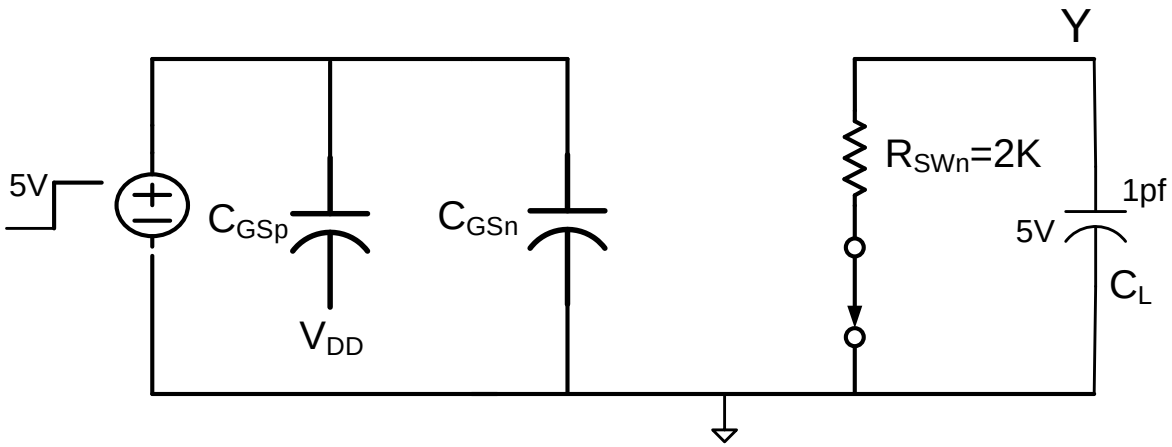


5V is the initial condition on C_L

Example (cont)

With improved model

t_{HL}=?



Recognize as a first-order RC network

Recall: Step response of any first-order network with LHP pole can be written as

$$y(t) = F + (I - F)e^{-\frac{t}{\tau}}$$

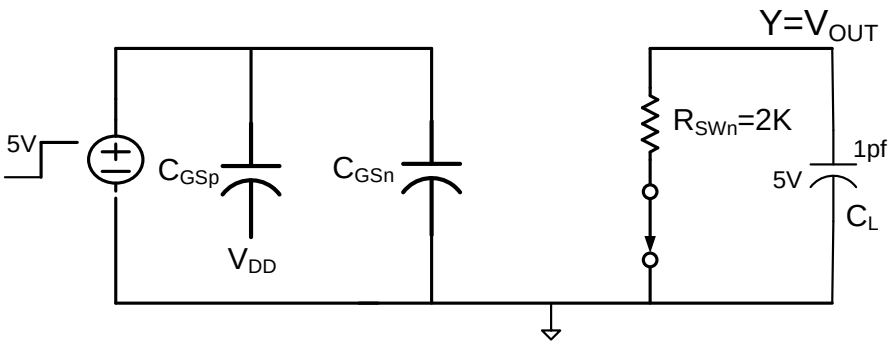
where F is the final value, I is the initial value and τ is the time constant of the circuit

(from Chapter 7 of Nilsson and Riedel)

For the circuit above, F=0, I=5 and $\tau = R_{SWn}C_L$

Example (cont)

With improved model

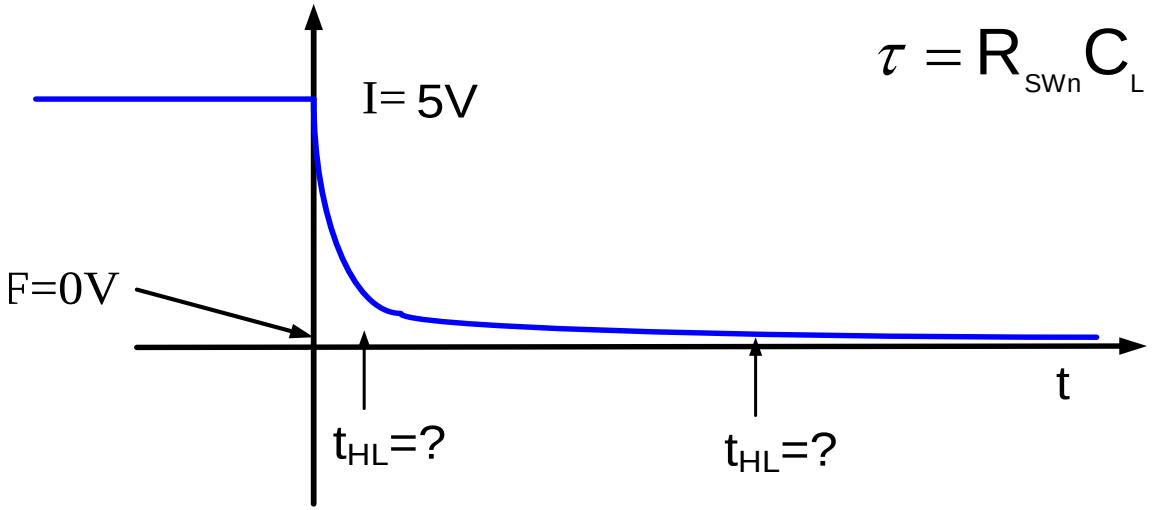


$t_{HL}=?$

$$V_{OUT}(t) = F + (I - F)e^{-\frac{t}{\tau}}$$

$$V_{OUT}(t) = 5e^{-\frac{t}{\tau}}$$

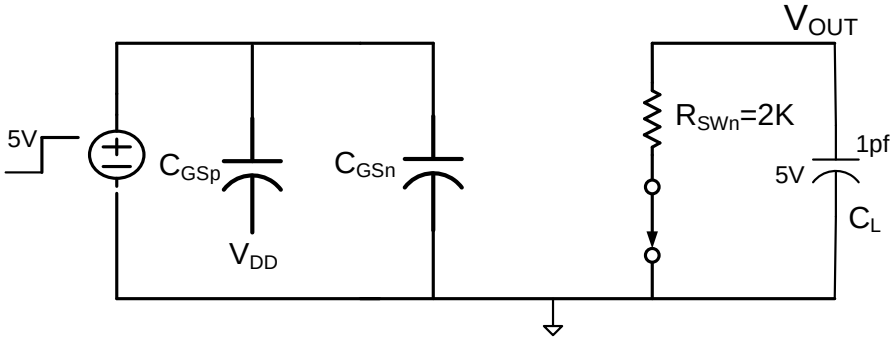
$$\tau = R_{SWn}C_L$$

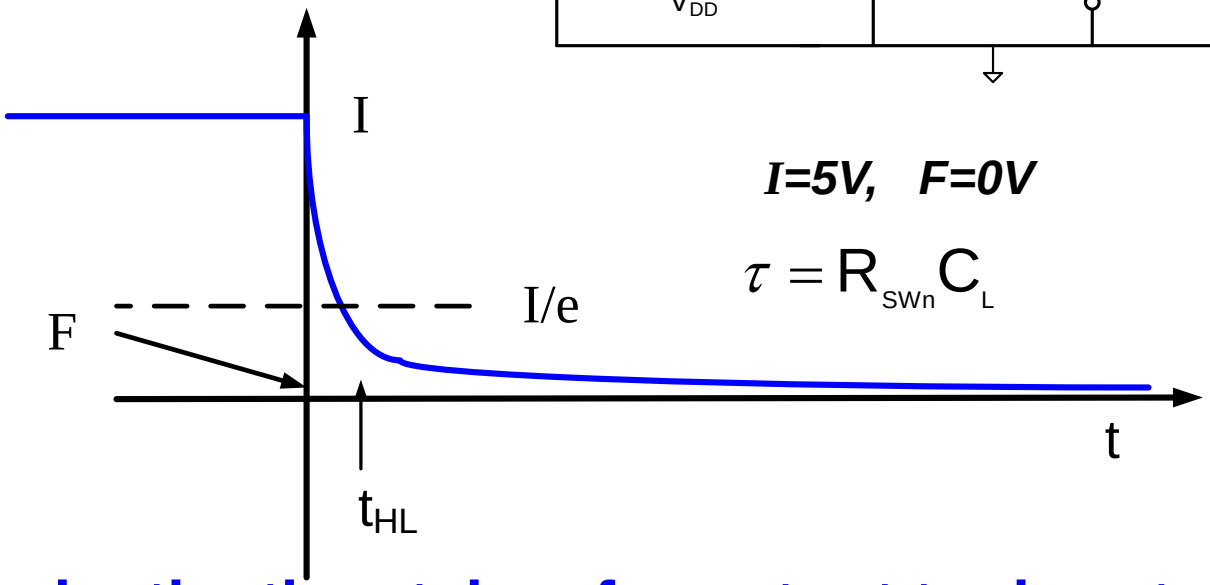


how is t_{HL} defined?

Example (cont)

t_{HL}=?





I=5V, F=0V

$$\tau = R_{SWn} C_L$$

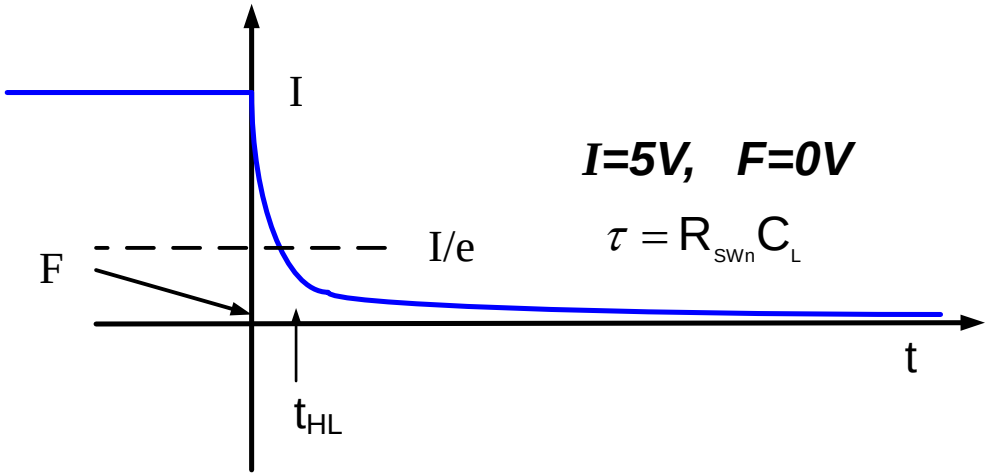
Define t_{HL} to be the time taken for output to drop to I/e

$$V_{OUT}(t) = F + (I - F)e^{-\frac{t}{\tau}} \quad \Rightarrow \quad \frac{I}{e} = F + (I - F)e^{-\frac{t_{HL}}{\tau}}$$

t_{HL} as defined here has proved useful at analytically predicting response time of circuits

Example (cont)

With improved model



$$\frac{I}{e} = F + (I - F)\, e^{-\frac{t_{HL}}{\tau}}$$

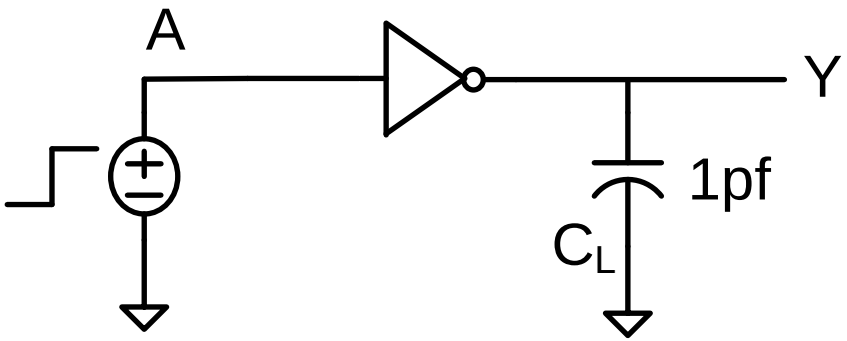
$$\frac{I}{e} = I\, e^{-\frac{t_{HL}}{\tau}}$$

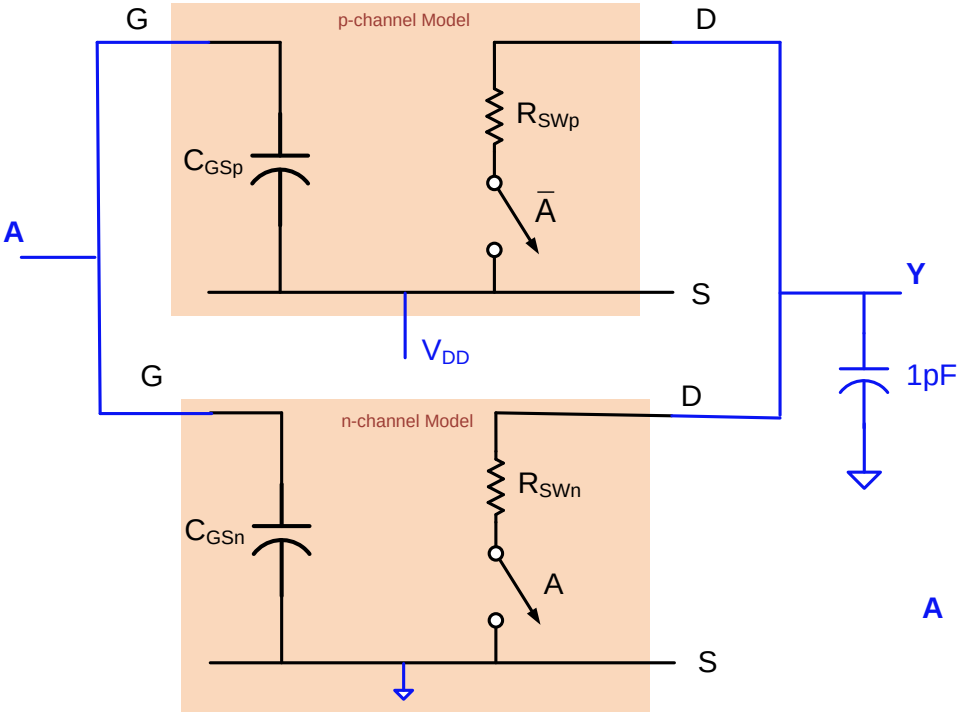
$$\frac{1}{e} = e^{-\frac{t_{HL}}{\tau}}$$

$$t_{HL} = \tau \quad \Rightarrow \quad t_{HL} = R_{SWn} C_L$$

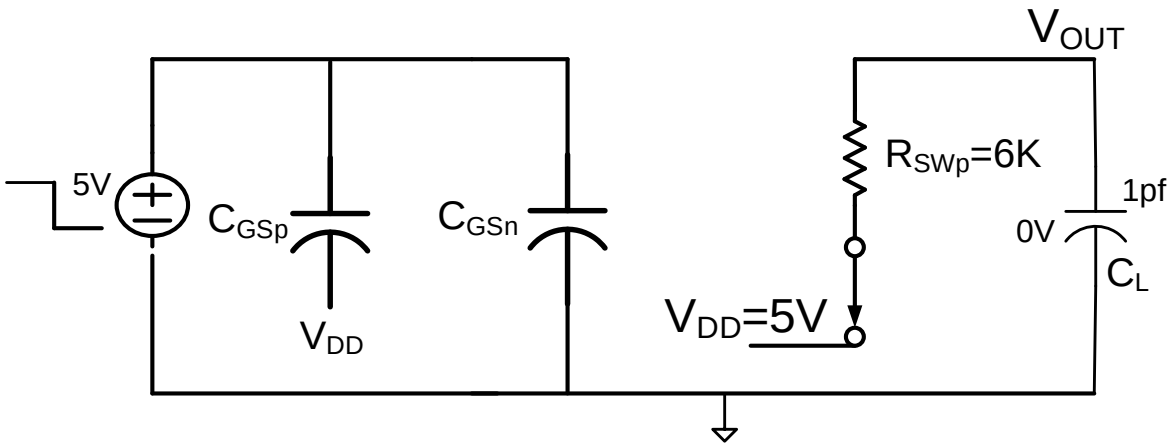
Example (cont)

With improved model $t_{LH}=?$





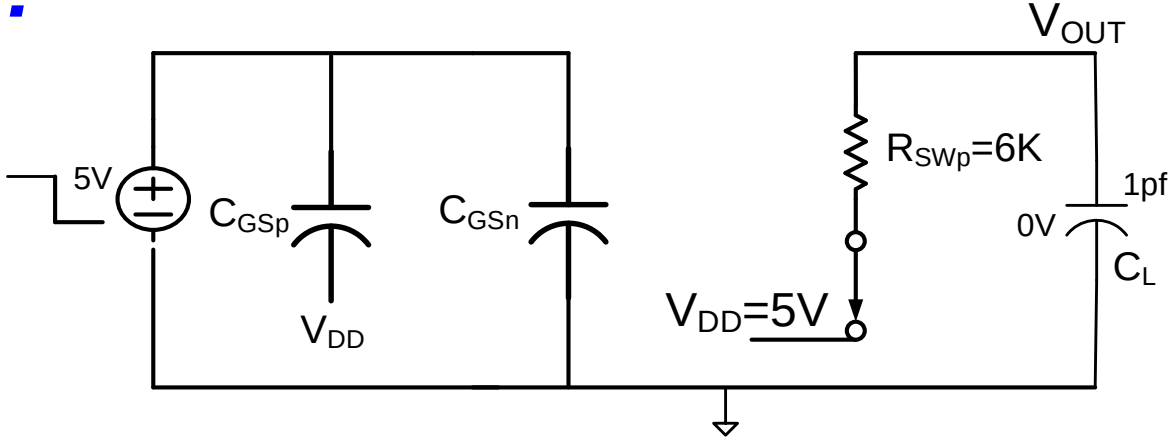
Assume output in low state for a long time and upper switch closes at time t=0



0V is the initial condition on C_L

Example (cont)

With improved model $t_{LH}=?$

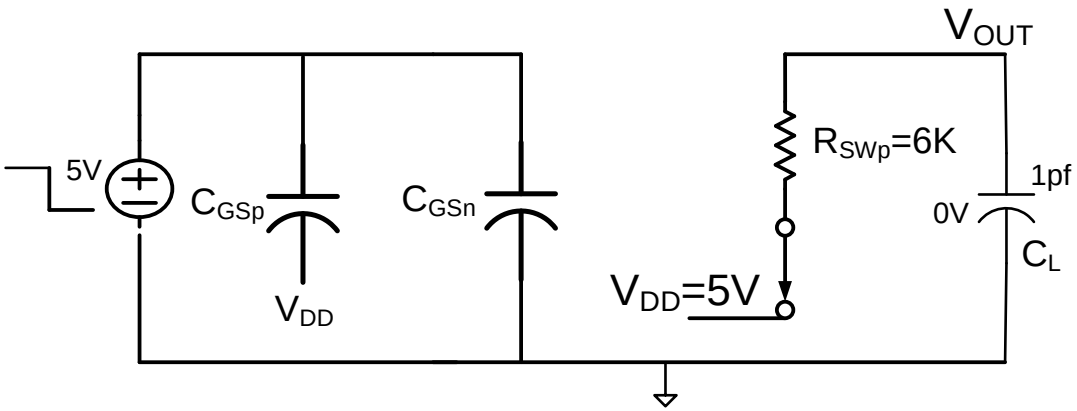


$$y(t) = F + (I - F)e^{-\frac{t}{\tau}}$$

For this circuit, F=5, I=0 and $\tau = R_{SWp}C_L$

Example (cont)

With improved model

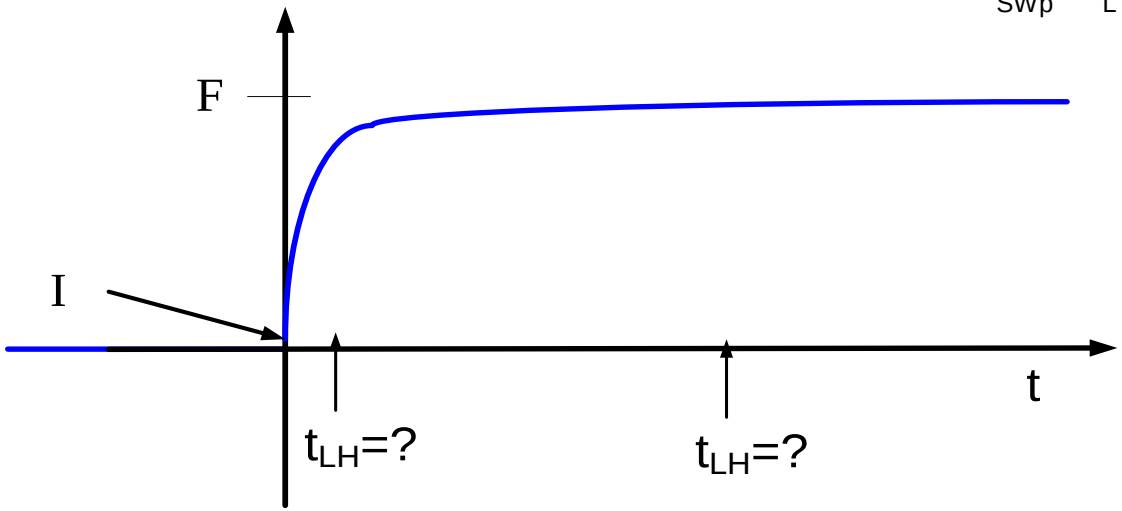


t_{LH}=?

$$V_{OUT}(t) = F + (I - F)e^{-\frac{t}{\tau}}$$

$$V_{OUT}(t) = 5\left(1 - e^{-\frac{t}{\tau}}\right)$$

$$\tau = R_{SWp}C_L$$

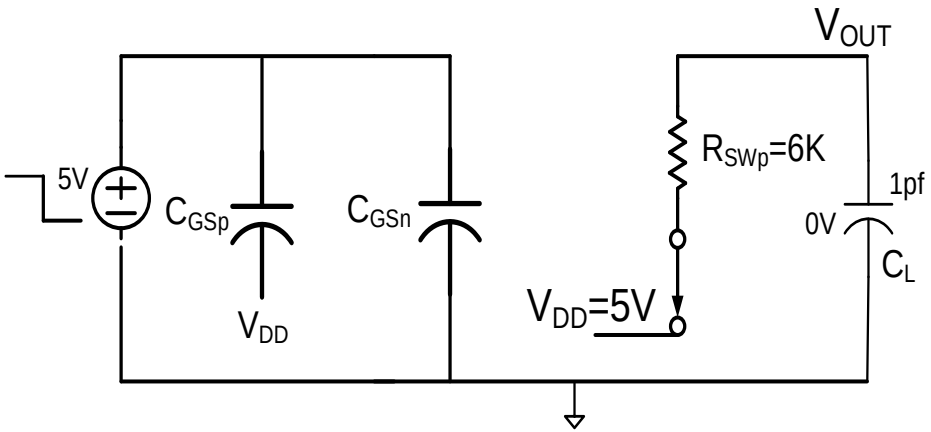


how is t_{LH} defined?

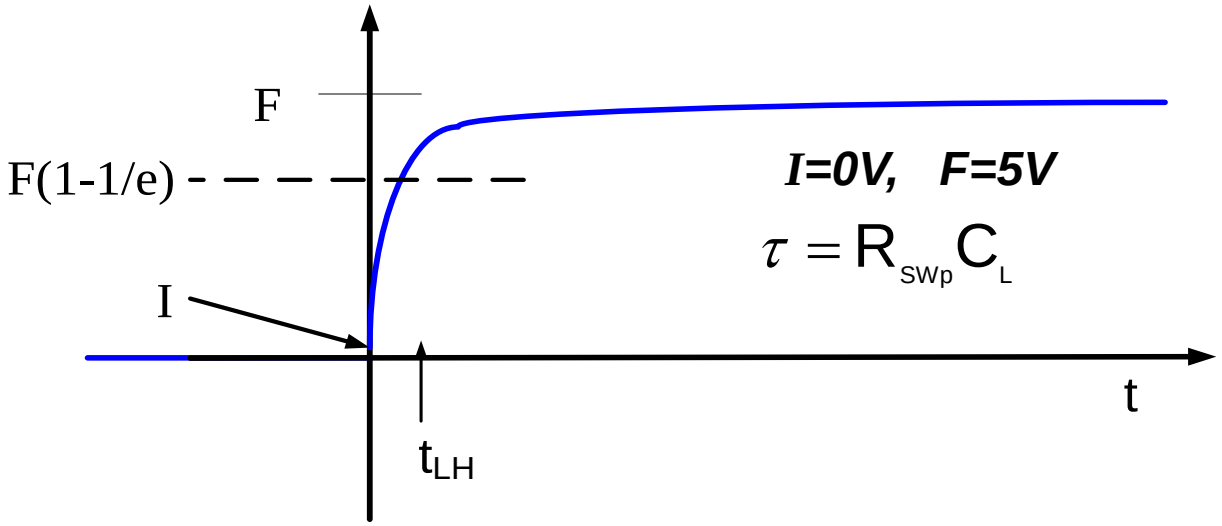
Example (cont)

With improved model

t_{LH}=?



Define t_{LH} as shown on figure



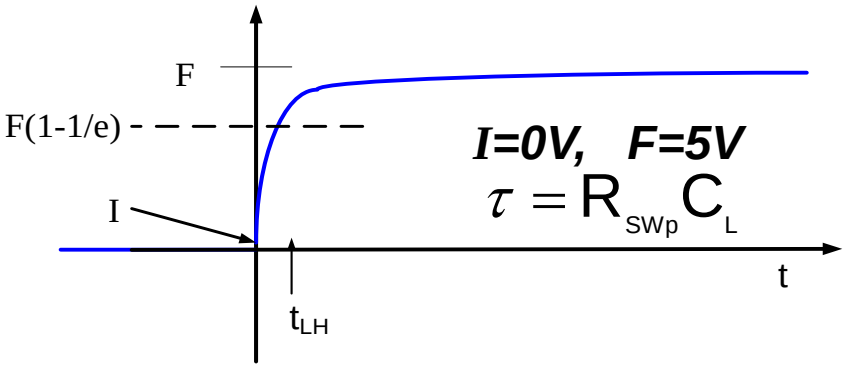
t_{LH} as defined has proven useful for analytically predicting response time of circuits

$$V_{OUT}(t) = F + (I - F)e^{-\frac{t}{\tau}} \quad \Rightarrow \quad F\left(1 - \frac{1}{e}\right) = F + (I - F)e^{-\frac{t_{LH}}{\tau}}$$

Example (cont)

With improved model

t_{LH}=?



$$F\left(1-\frac{1}{e}\right) = F + (I - F)e^{-\frac{t_{LH}}{\tau}}$$

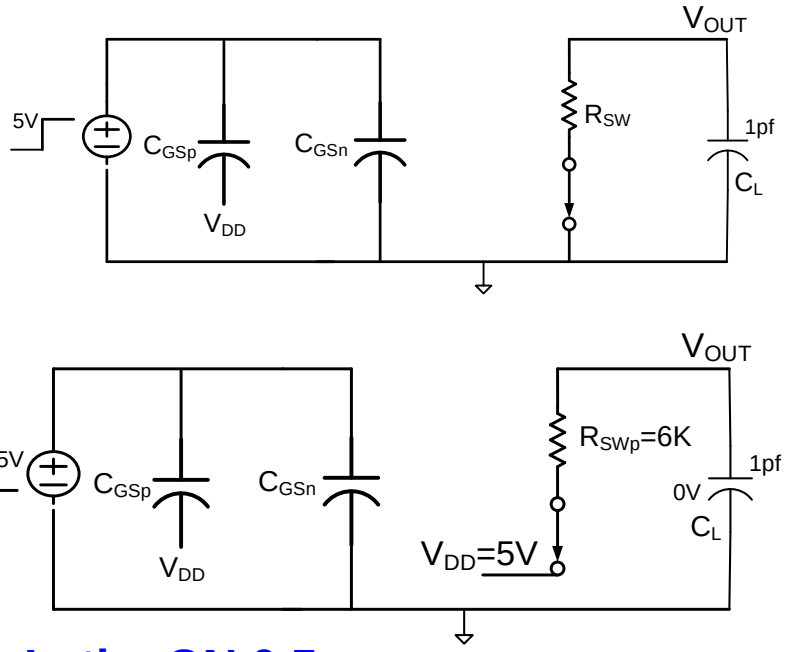
$$F\left(1-\frac{1}{e}\right) = F + (F)e^{-\frac{t_{LH}}{\tau}}$$

$$1-\frac{1}{e} = 1 + e^{-\frac{t_{LH}}{\tau}}$$

$$t_{LH} = \tau \quad \Rightarrow \quad t_{LH} = R_{SWp} C_L$$

Example (cont)

With improved model



In the ON 0.5u process

$$t_{HL} \cong R_{SWn} C_L = 2K \bullet 1pF = 2n\,\text{sec}$$

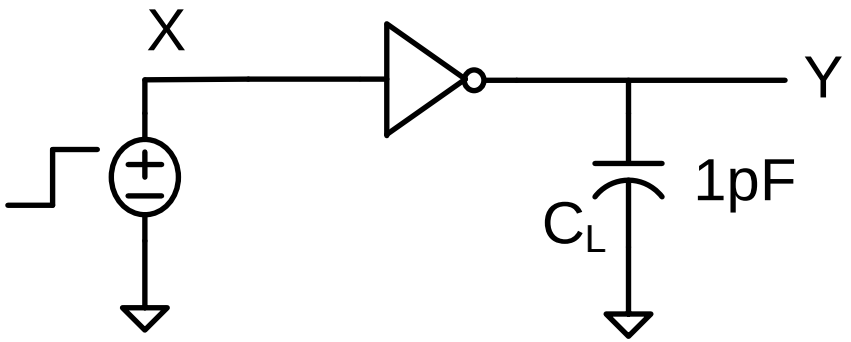
$$t_{LH} \cong R_{SWp} C_L = 6K \bullet 1pF = 6n\,\text{sec}$$

Note this circuit is quite fast !

Note that t_{HL} is much shorter than t_{LH}

Often C_L will be even smaller and the circuit will be much faster !!

Summary: What is the delay of a minimum-sized inverter driving a 1pF load?

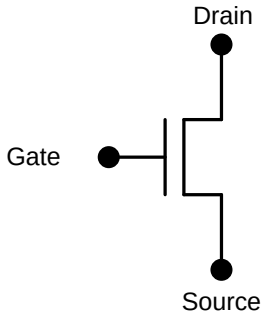


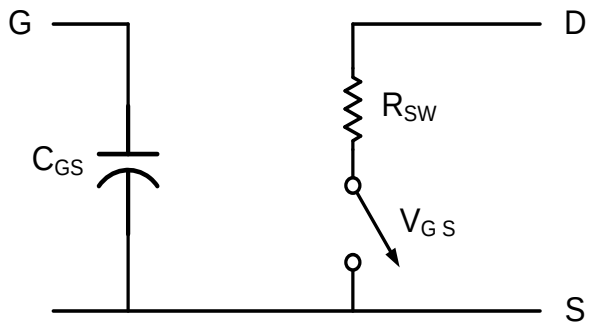
In the ON 0.5u process

$$t_{HL} \cong R_{SWn} C_L = 2K \bullet 1pF = 2n\,\text{sec}$$

$$t_{LH} \cong R_{SWp} C_L = 6K \bullet 1pF = 6n\,\text{sec}$$

Improved switch-level model





Switch closed for V_{GS}= large

Switch open for V_{GS}= small

- **Previous example showed why R_{SW} in the model was important**
- **But of what use is the C_{GS} which did not enter the previous calculations?**

For minimum-sized devices in a 0.5u process

$$C_{GS} \cong 1.5fF \qquad R_{sw} \cong \begin{cases} 2K\Omega \;\; n-channel \\ 6K\Omega \;\; p-channel \end{cases}$$

End of Lecture 6