EE 330
Lecture 9

IC Fabrication Technology
Part II

- Deposition
- Implantation
- Etching
- Oxidation
- Epitaxy
- Polysilicon
- Planarization
- Resistance and Capacitance in Interconnect

IC Fabrication Technology

- Crystal Preparation
- Masking
- Photolithographic Process
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Photolithographic Process

- Photoresist
  - Viscous Liquid
  - Uniform Application Critical (spinner)
  - Baked to harden
  - Approx 1u thick
  - Non-Selective
  - Types
    - Negative – unexposed material removed when developed
    - Positive-exposed material removed when developed
    - Thickness about 450nm in 90nm process (ITRS 2007 Litho)
- Exposure
  - Projection through reticle with stepper (scanners becoming popular)
  - Alignment is critical !!
  - E-Bean Exposures
    - Eliminate need fro reticle
    - Capacity very small

Stepper: Optics fixed, wafer steps in fixed increments
Scanner: Wafer steps in fixed increments and during exposure both optics and wafer are moved to increase effective reticle size

Deposition

Example: Chemical Vapor Deposition

Silane (SiH_4) is a gas (toxic and spontaneously combustible in air) at room temperature but breaks down into Si and H_2 above 400^{o}C so can be used to deposit Si.

$$S_iH_4 \rightarrow S_i + 2H_2$$

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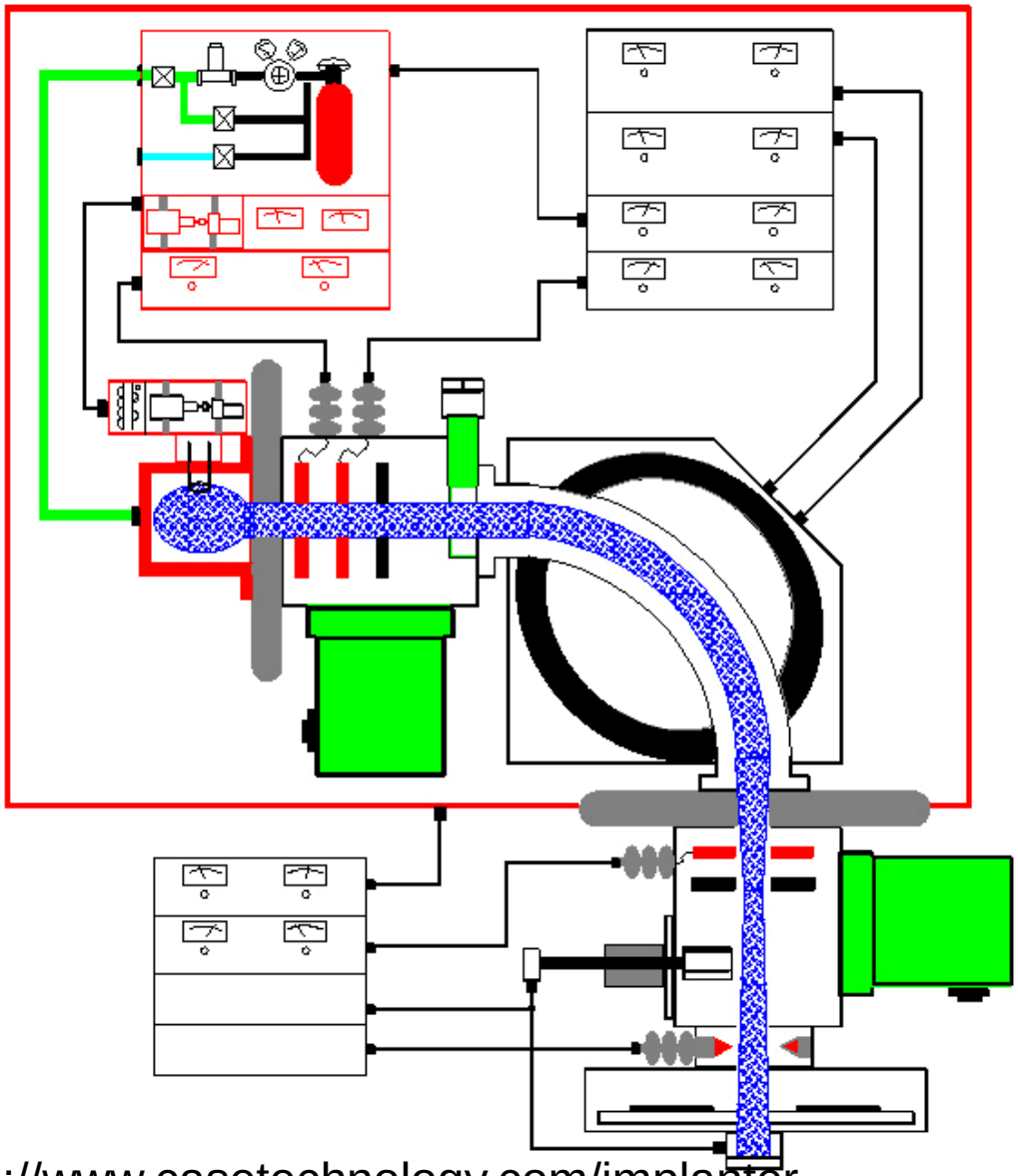
Implantation

Application of impurities into the surface of the silicon wafer or substrate

- Individual atoms are first ionized (so they can be accelerated)
- Impinge on the surface and burry themselves into the upper layers
- Often very shallow but with high enough energy can go modestly deep
- Causes damage to target on impact
- Annealing heals most of the damage
- Very precise control of impurity numbers is possible
- Very high energy required
- High-end implanters considered key technology for national security

Ion Implantation Process



From http://www.casetechnology.com/implanter

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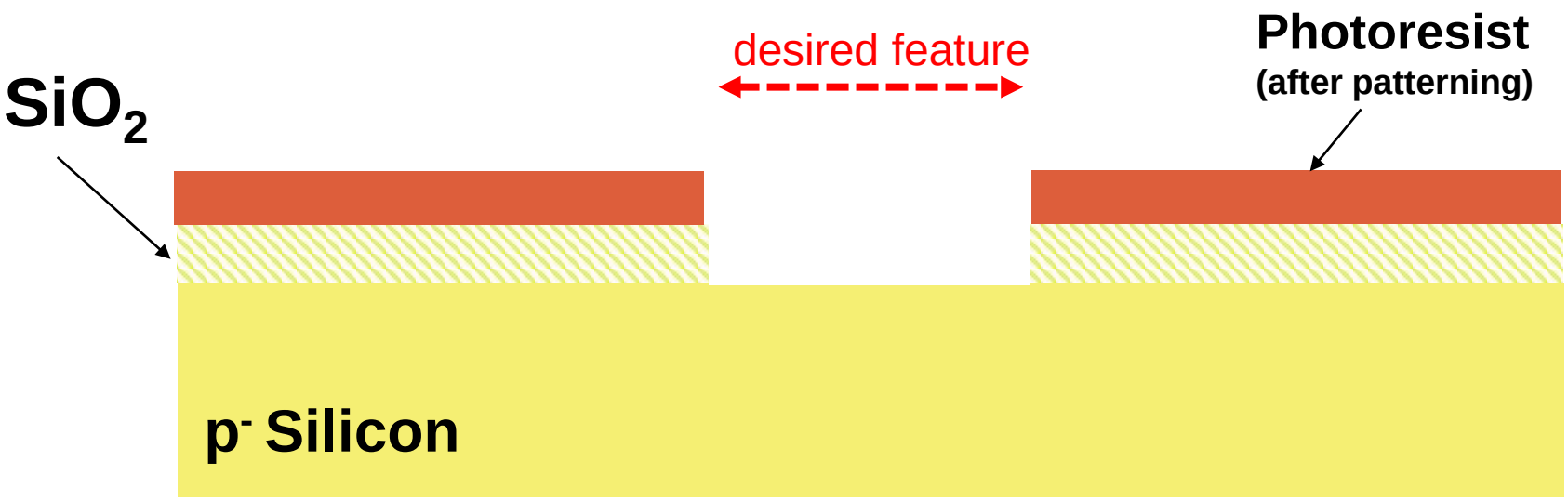
Etching

Selective Removal of Unwanted Materials

- Wet Etch
  - Inexpensive but under-cutting a problem
- Dry Etch
  - Often termed ion etch or plasma etch

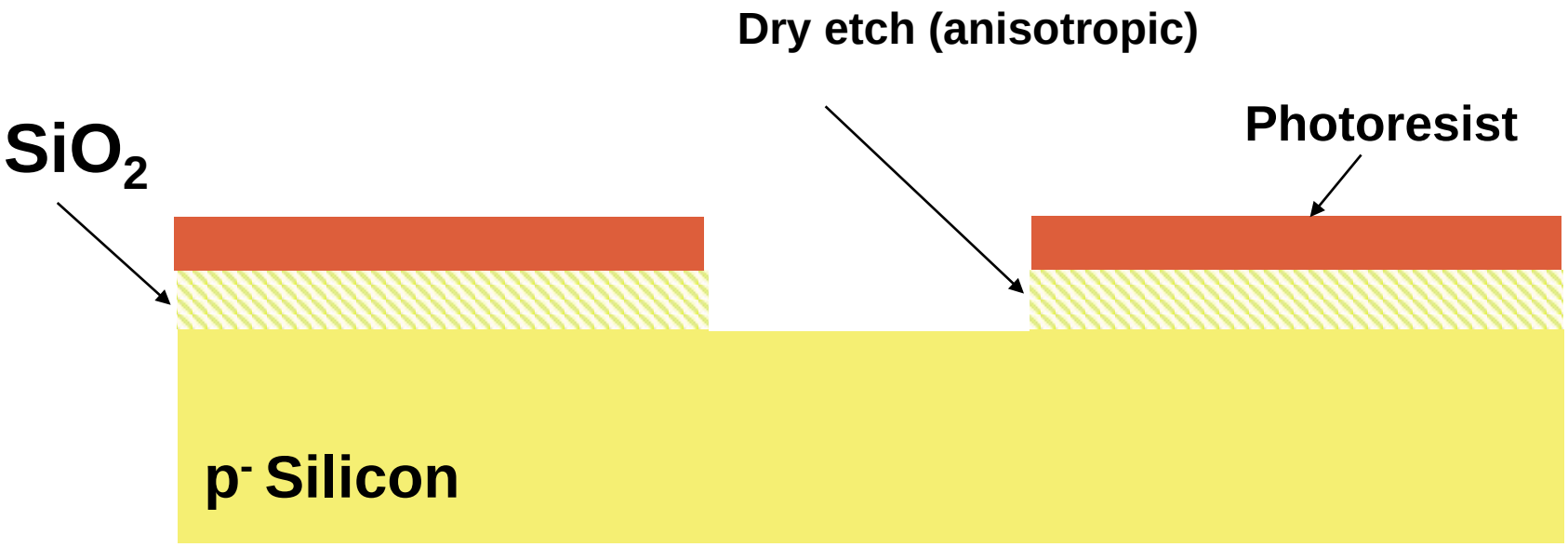
Etching



Desired Physical Features

Note: Vertical Dimensions in silicon generally orders of magnitude smaller than lateral dimensions so different vertical and lateral scales will be used in this discussion. Vertical dimensions of photoresist which is applied on top of wafer is about ½ order of magnitude larger than lateral dimensions

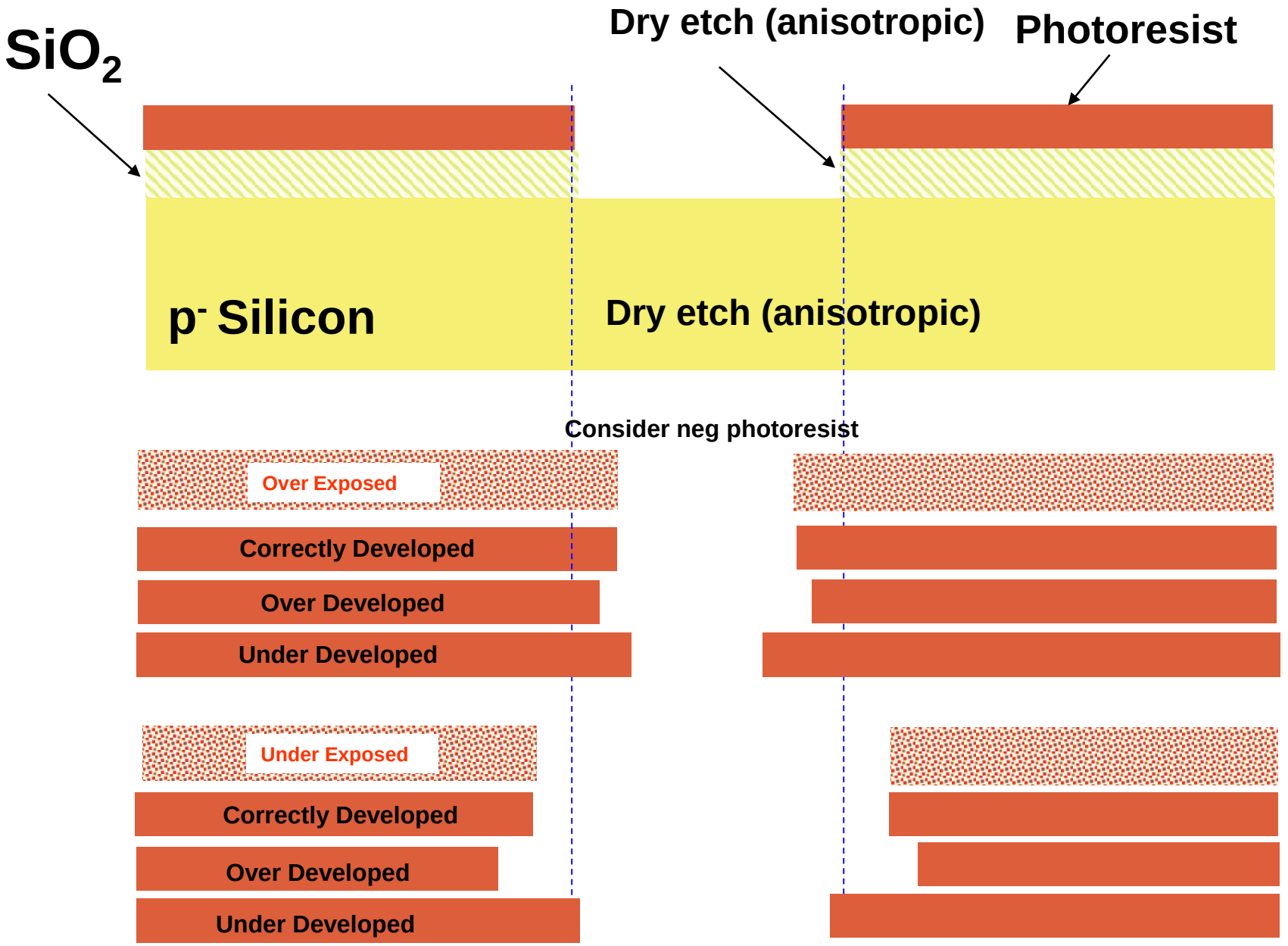
Etching



Desired Physical Features

Dry Etch can provide very well-defined and nearly vertical edges (relative to photoresist paterning)

Etching (limited by photolitghographic process)



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Diffusion

- Controlled Migration of Impurities
  - Time and Temperature Dependent
  - Both vertical and lateral diffusion occurs
  - Crystal orientation affects diffusion rates in lateral and vertical dimensions
  - Materials Dependent
  - Subsequent Movement
  - Electrical Properties Highly Dependent upon Number and Distribution of Impurities
  - Diffusion at 800^{o}C to 1200^{o}C
- Source of Impurities
  - Deposition
  - Ion Implantation
    - Depth depending on ion speed/enery
    - More accurate control of doping levels
    - Fractures silicon crystaline structure during implant
    - Annealing occurs during diffusion
- Types of Impurities
  - n-type Arsenic, Antimony, Phosphorous
  - p-type Gallium, Aluminum, Boron

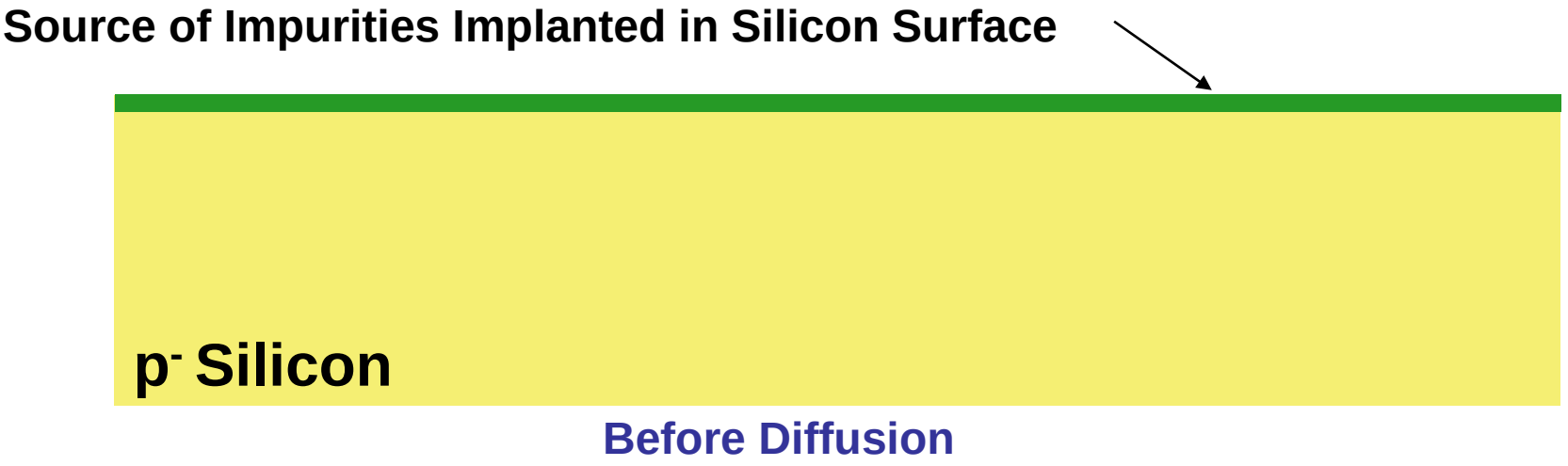
Diffusion

Source of Impurities Deposited on Silicon Surface

Before Diffusion

After Diffusion

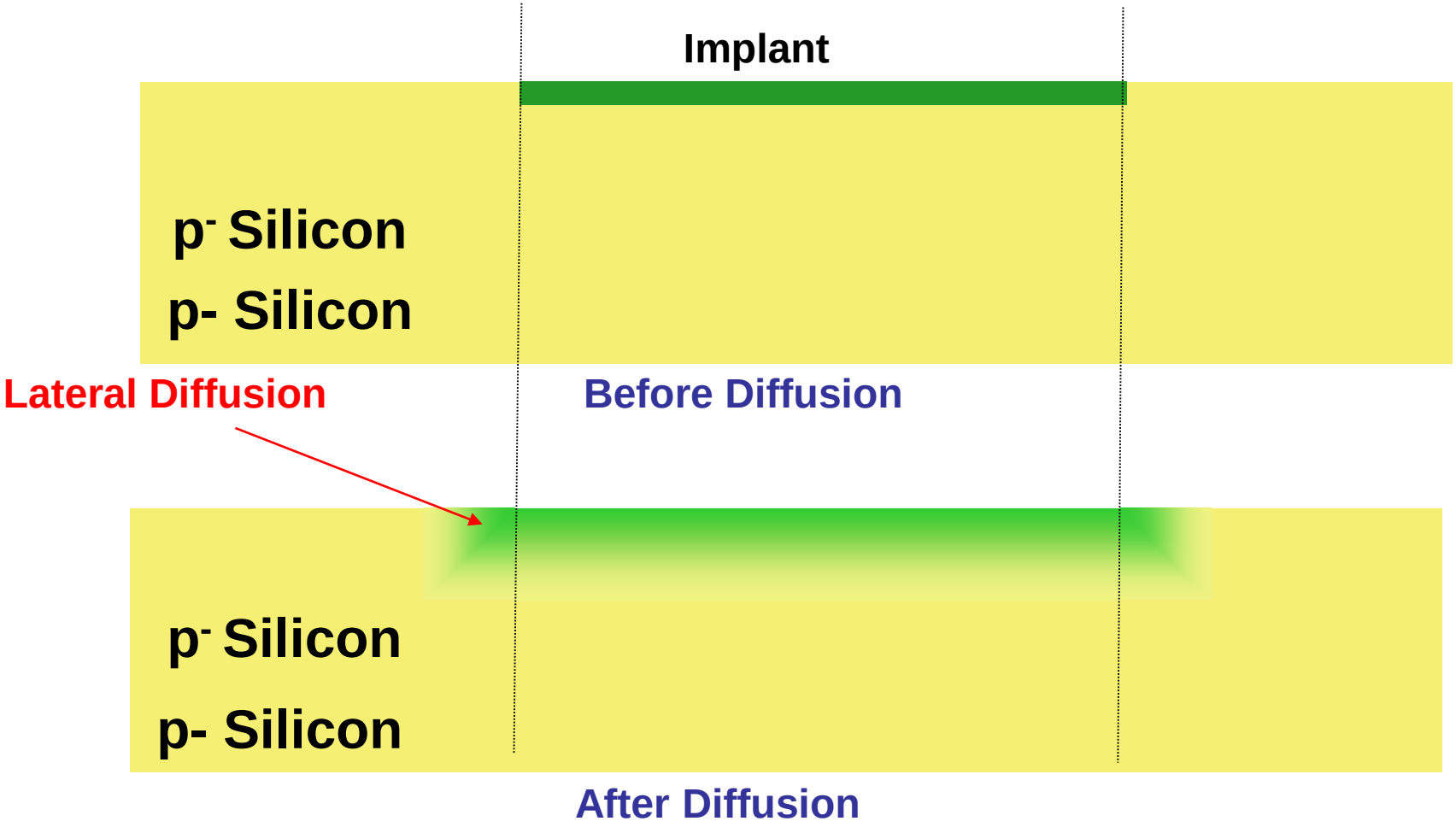
Diffusion



Before Diffusion

After Diffusion

Diffusion


Implant
p- Silicon
p- Silicon
Lateral Diffusion
Before Diffusion
p- Silicon
p- Silicon
After Diffusion

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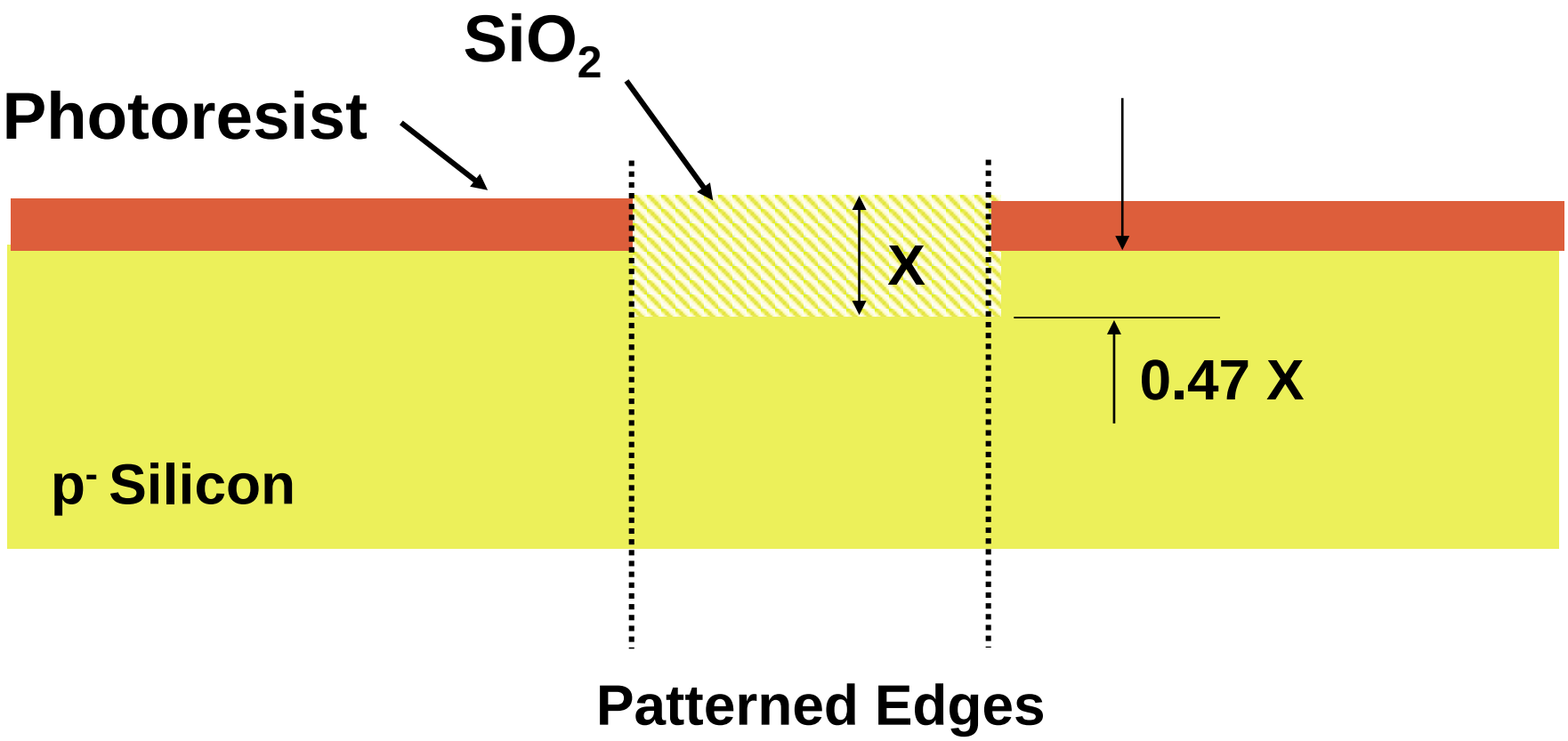
Oxidation

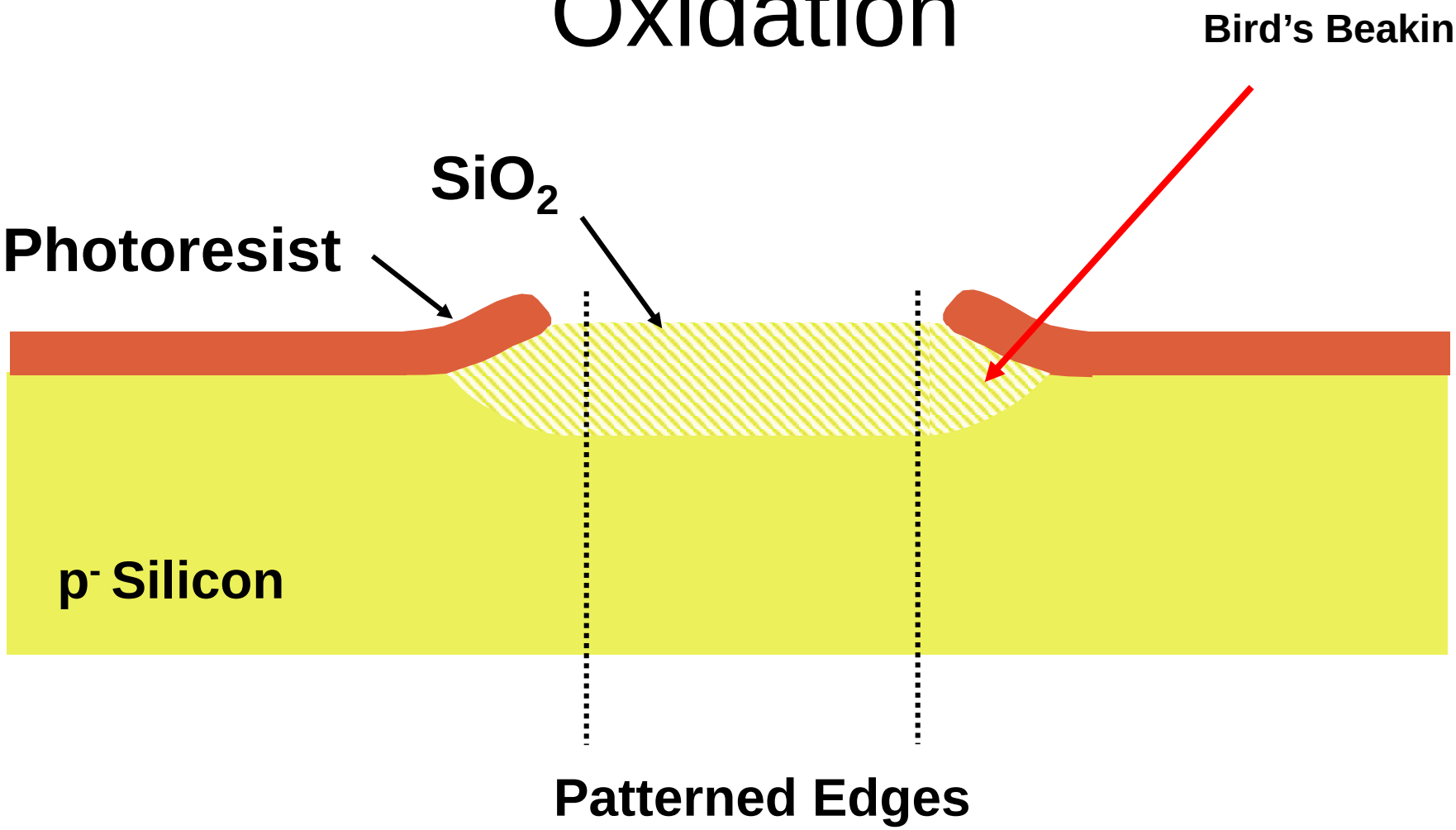
- SiO_2 is widely used as an insulator
  - Excellent insulator properties
- Used for gate dielectric
  - Gate oxide layers very thin
- Used to separate devices by raising threshold voltage
  - termed field oxide
  - field oxide layers very thick
- Methods of Oxidation
  - Thermal Growth (LOCOS)
    - Consumes host silicon
    - x units of SiO_2 consumes .47x units of Si
    - Undercutting of photoresist
    - Compromises planar surface for thick layers
    - Excellent quality
  - Chemical Vapor Deposition
    - Needed to put SiO_2 on materials other than Si

Oxidation



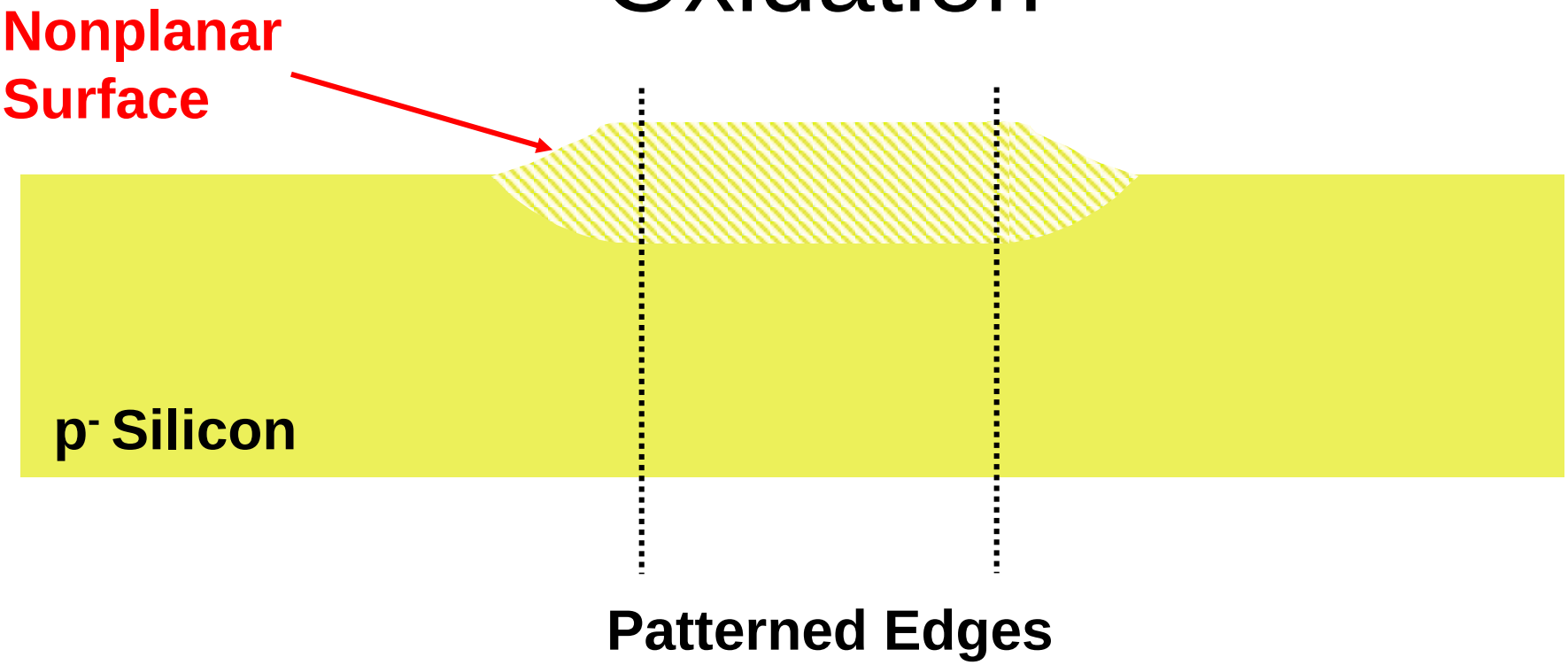
Thermally Grown SiO_2 - desired growth

Oxidation



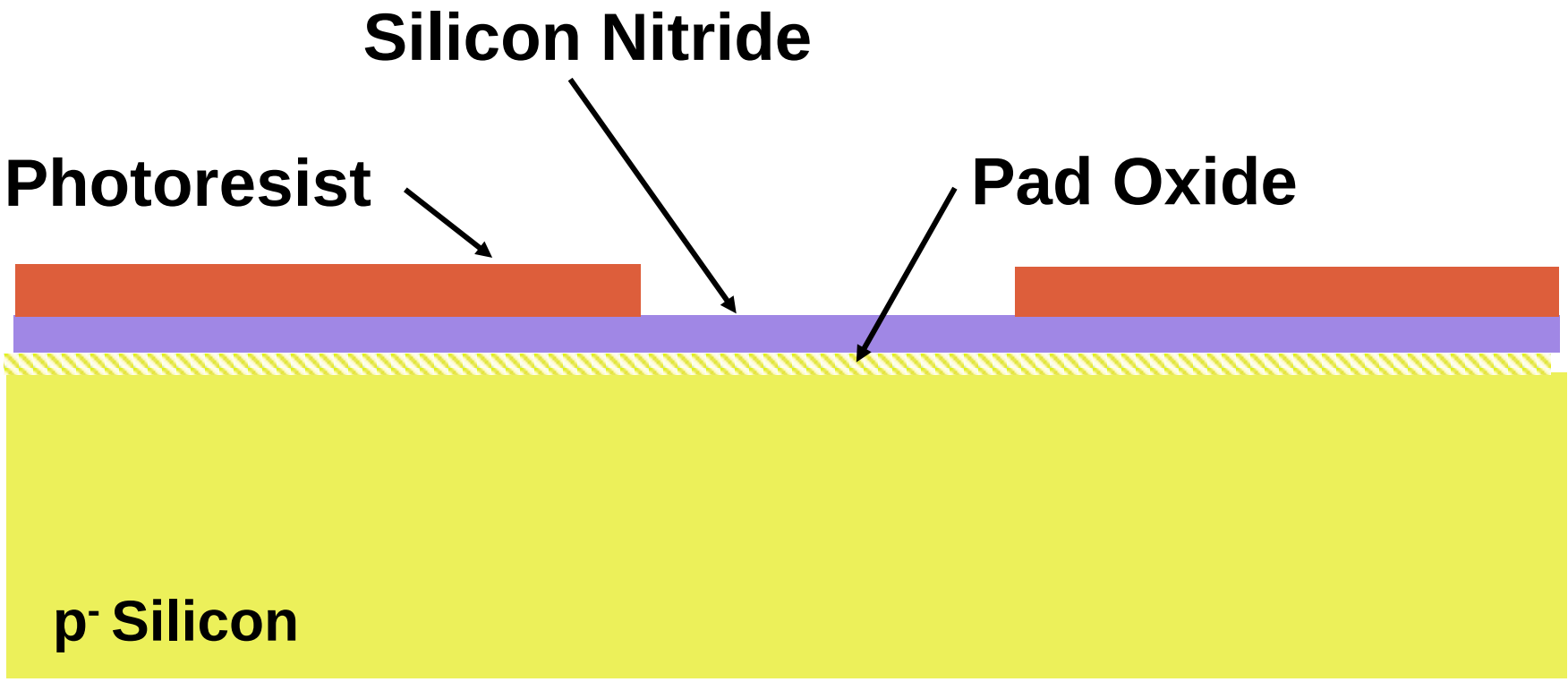
Thermally Grown SiO_2 - actual growth

Oxidation



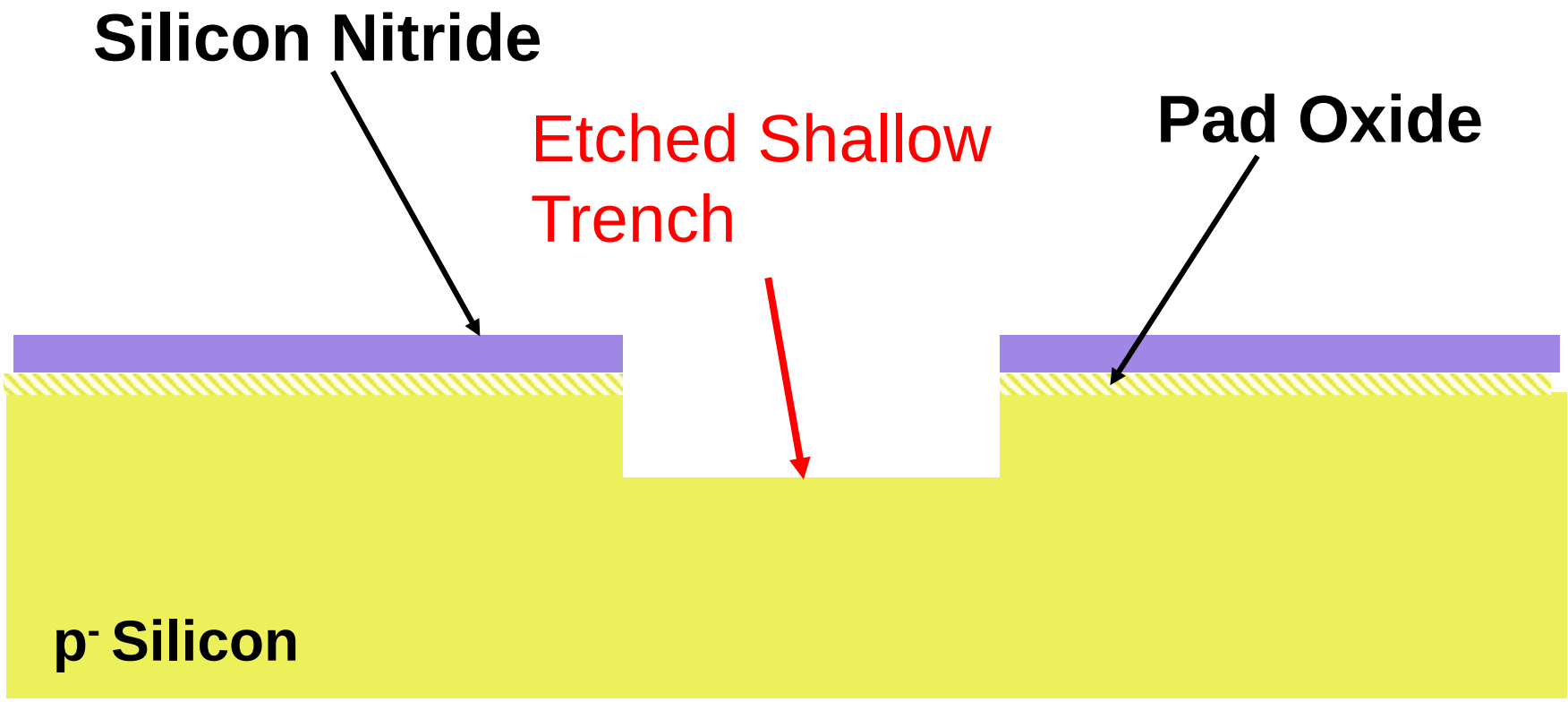
Thermally Grown SiO_2 - actual growth

Oxidation



Shallow Trench Isolation (STI)

Oxidation



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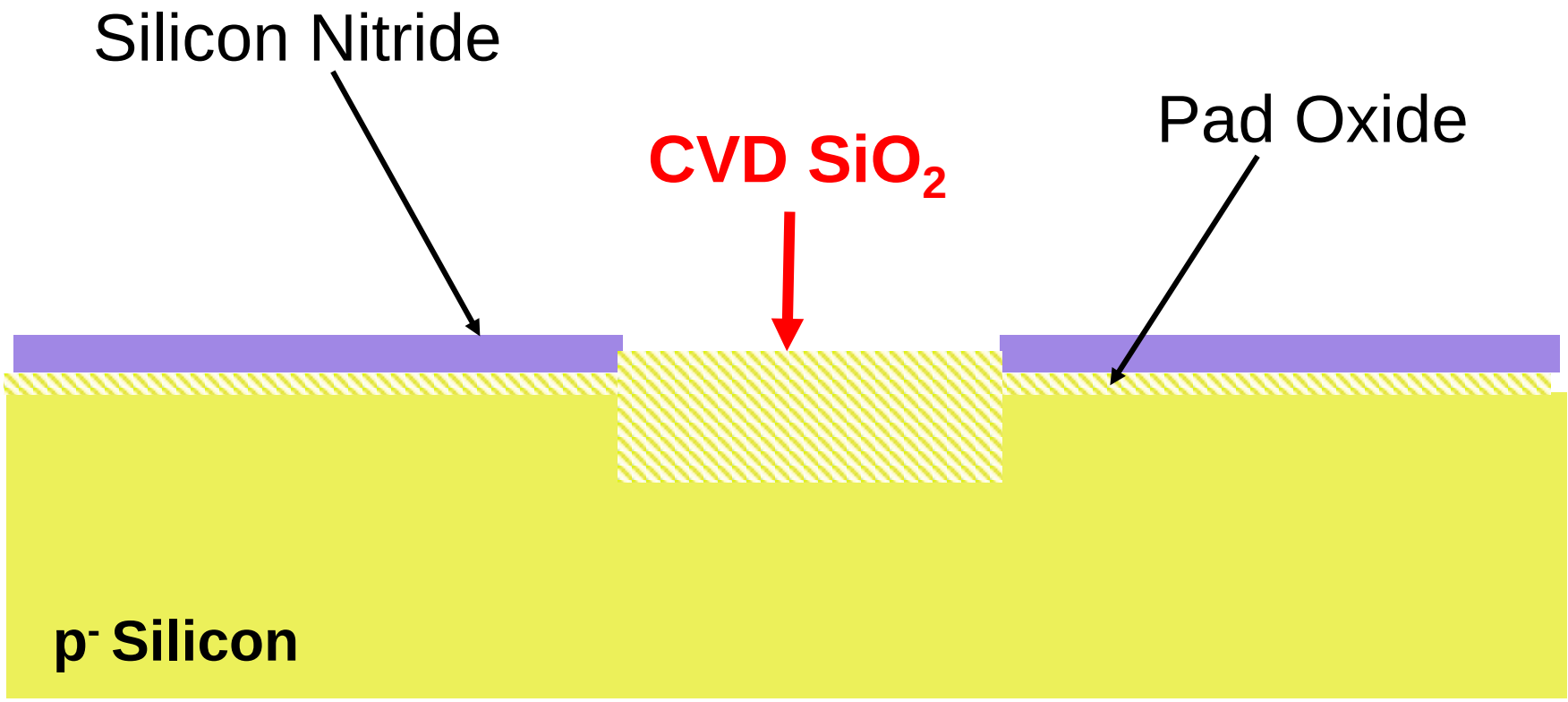
Oxidation



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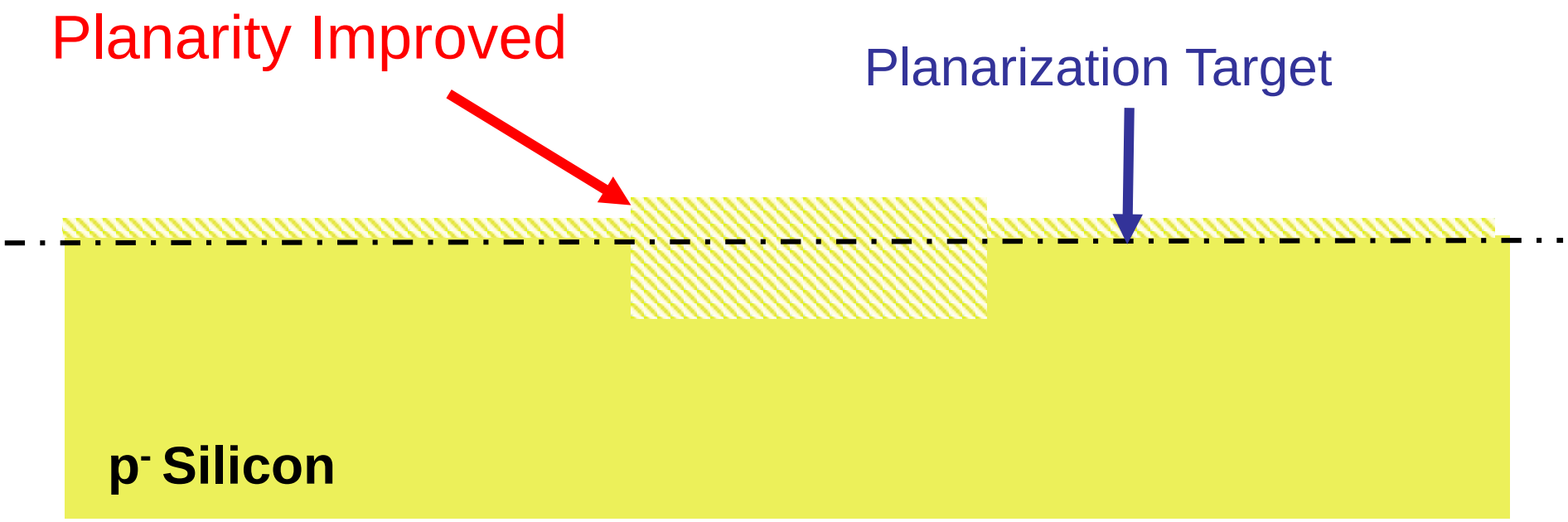
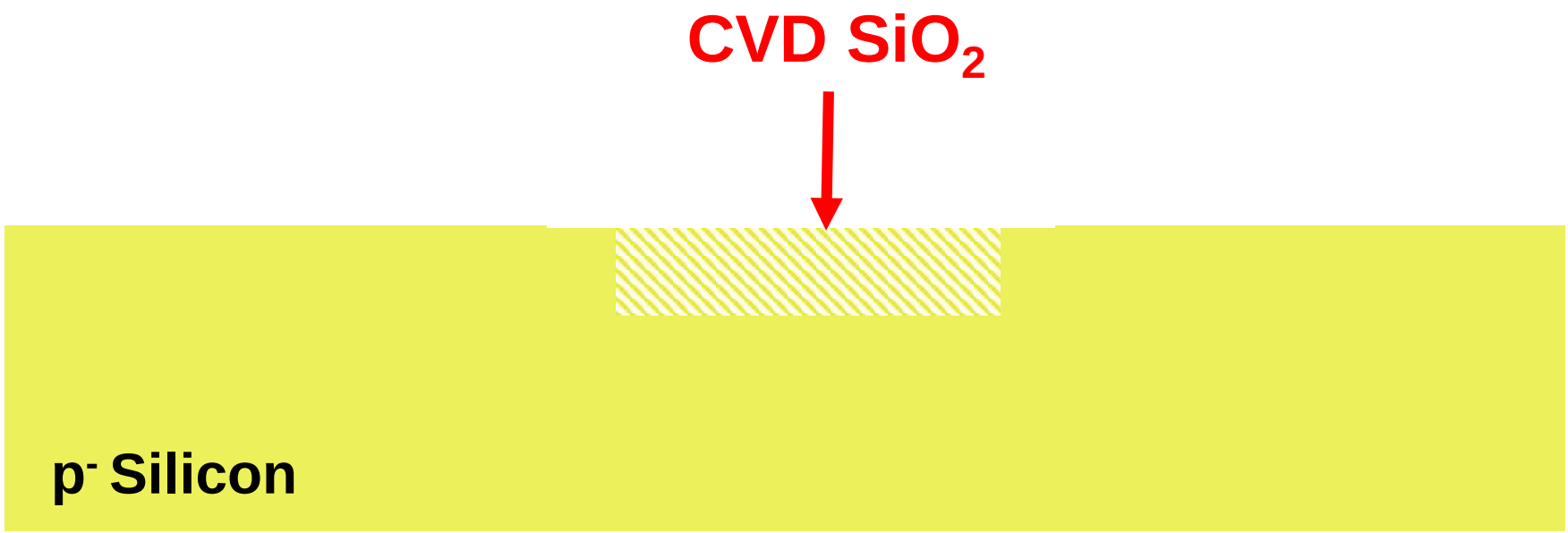


Shallow Trench Isolation (STI)

Oxidation

After Planarization



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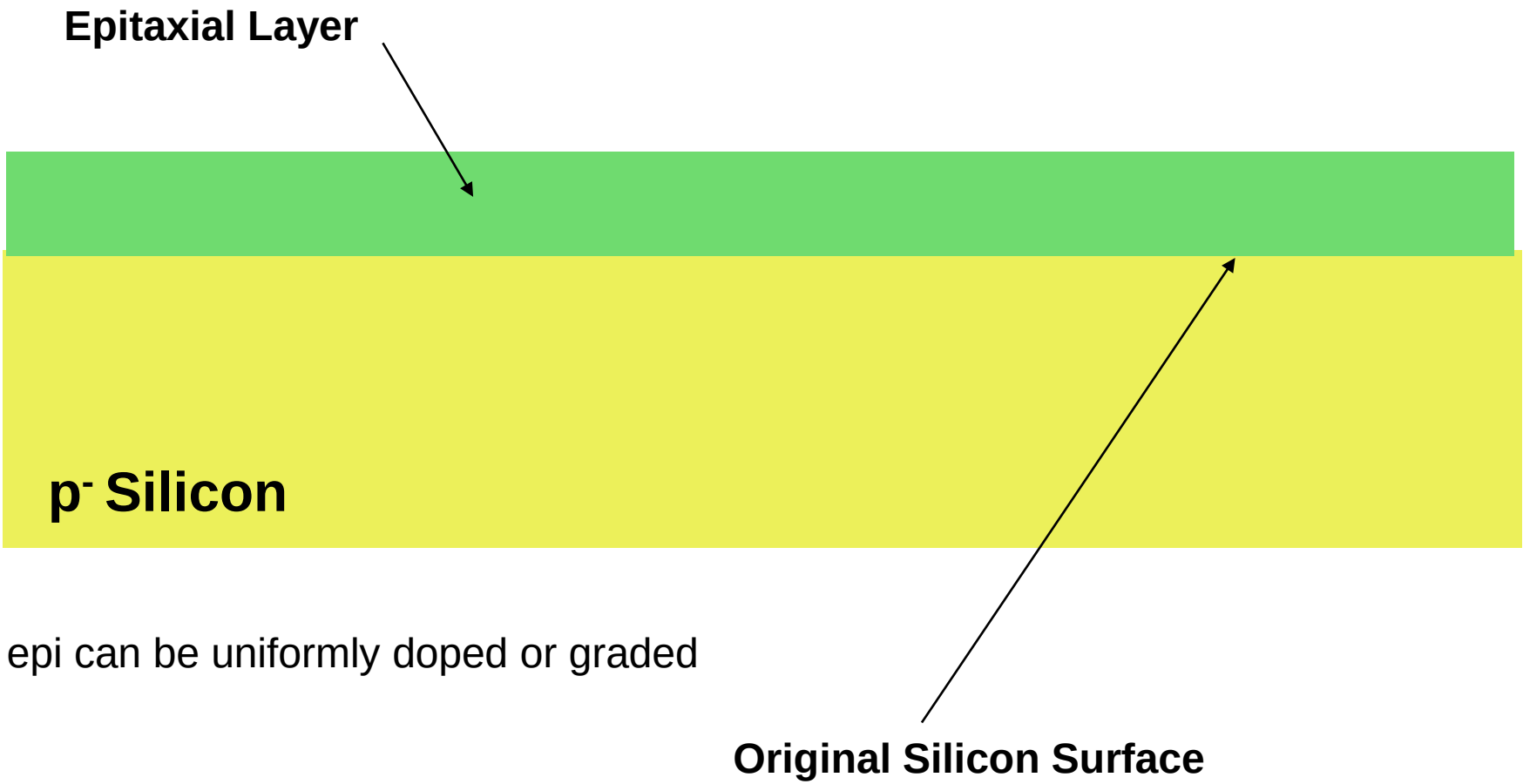
Epitaxy

- Single Crystaline Extension of Substrate Crystal
  - Commonly used in bipolar processes
  - CVD techniques
  - Impurities often added during growth
  - Grows slowly to allow alignmnt with substrate

Epitaxy



epi can be uniformly doped or graded

Question: Why can't a diffusion be used to create the same effect as an epi layer ?

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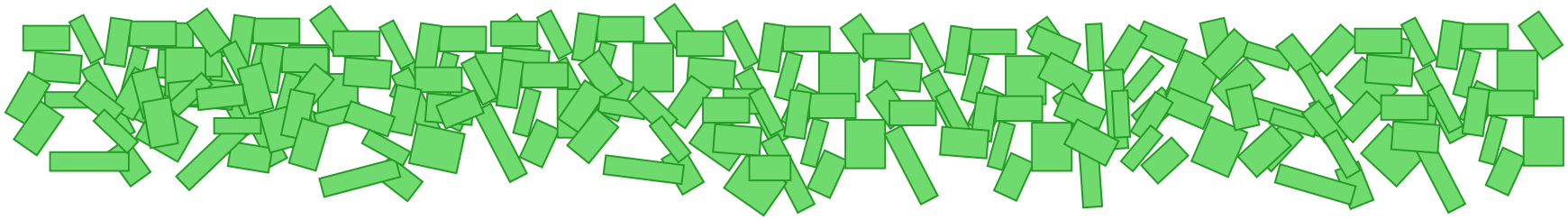
Polysilicon

- Elemental contents identical to that of single crystaline silicon
  - Electrical properties much different
  - If doped heavily makes good conductor
  - If doped moderately makes good resistor
  - Widely used for gates of MOS devices
  - Widely used to form resistors
  - Grows fast over non-crystaline surface
  - Patterned with Photoresist/Etch process
  - Silicide often used in regions where resistance must be small
    - Refractory metal used to form silicide
    - Designer must indicate where silicide is applied (or blocked)

Polysilicon



Polysilicon

Single-Crystaline Silicon

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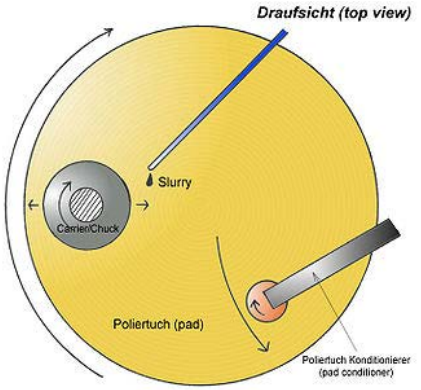
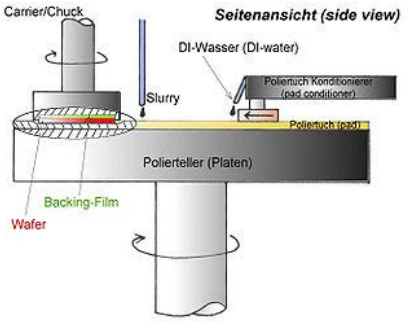
Planarization

- Planarization used to keep surface planar during subsequent processing steps
  - Important for creating good quality layers in subsequent processing steps
  - Mechanically planarized





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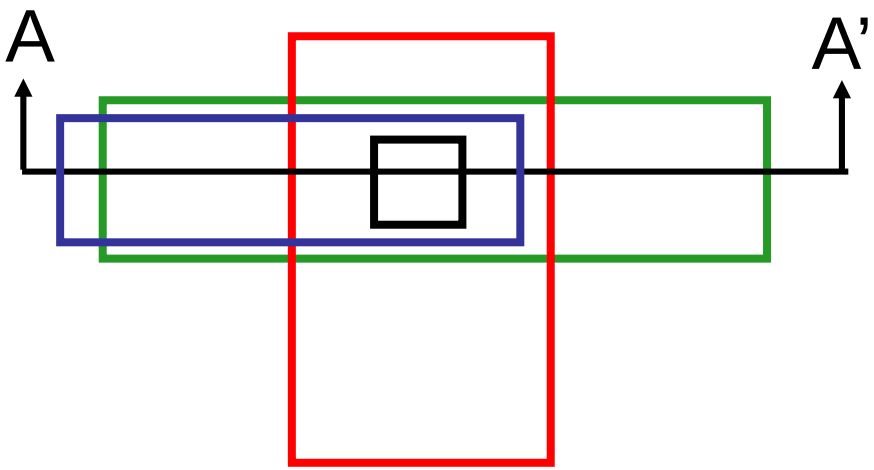
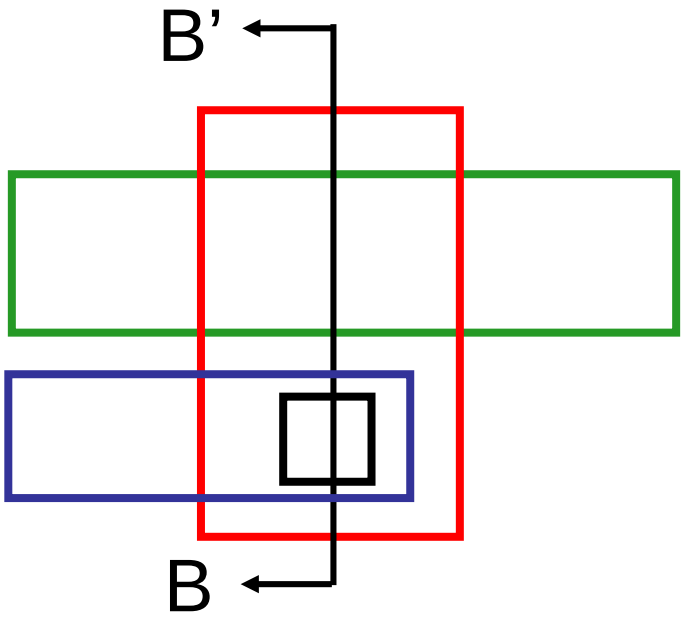
Contacts, Interconnect and Metalization

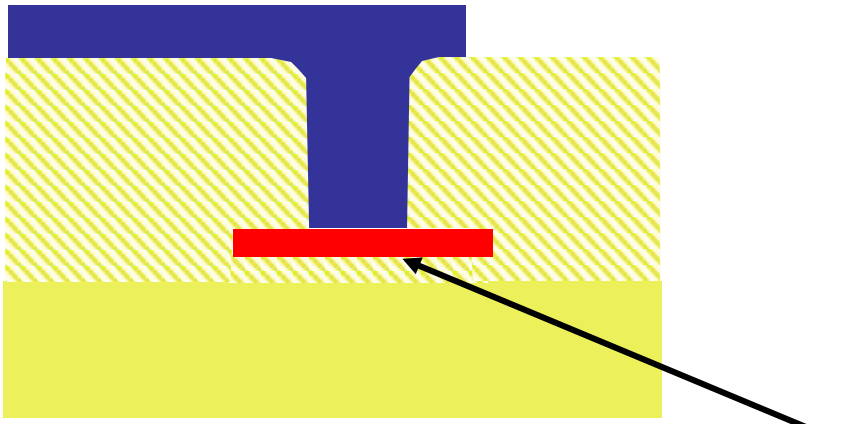
- Contacts usually of a fixed size
  - All etches reach bottom at about the same time
  - Multiple contacts widely used
  - Contacts not allowed to Poly on thin oxide in most processes
  - Dog-bone often needed for minimum-length devices

Contacts





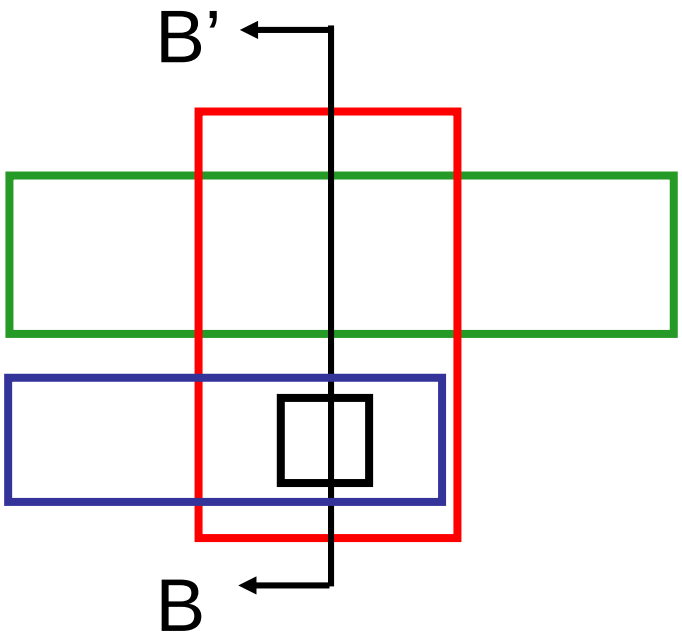
Acceptable Contact

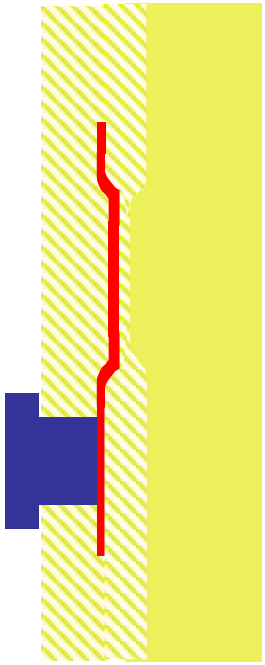


Unacceptable Contact

Vulnerable to pin holes
(usually all contacts are same size)

Contacts





Acceptable Contact

End of Lecture 9