EE 330 Quiz #14

Name: Score

Grader:

Briefly answer the following questions:

1. For an enhancement MOS TET, when there is no |VGS| applied, the channel under the gate is­­­­­­­­­­­­­­­\_\_\_nonexistent/nonconducting\_\_; (the MOST is in off state)
2. When the applied |VGS| is larger than a threshold, and |VDS| is very small, the channel under the gate becomes ­­­­­­­­­­­\_\_inversion layer/conducting\_\_; (the MOST is in triode)
3. As |VDS| increases to larger than a certain value, the D-side of the inversion layer will become \_\_\_\_pinched-off\_\_. (the MOST is in saturation)
4. For a depletion MOS TET, when there is no |VGS| applied, the channel under the gate is­­­­­­­­­­­­­­­\_\_conducting\_\_;
5. When the applied |VGS| becomes larger, the thickness of channel conducting layer becomes ­­­­­­­­­­­\_\_thinner\_\_\_;
6. If an applied |VDS| also increases to larger than a certain value, the D-side of the conducting layer will become \_\_pinched-off\_\_\_.
7. A JFET is similar to a depletion MOS FET, but a JFET gate is not a poly on top of SiO2, p-channel JFET’s gate is \_\_\_\_\_n-type\_\_\_\_\_\_\_\_\_ material.
8. For a p-channel JTET, when there is no |VGS| applied, the channel under the gate is­­­­­­­­­­­­­­­\_\_\_conducting\_\_;
9. When the applied |VGS| becomes larger, the PN junction depletion becomes thicker, and the thickness of the p-channel conducting layer becomes ­­­­­­­­­­\_\_\_\_thinner\_\_\_;
10. If an applied |VDS| also increases to larger than a certain value, the D-side of p-channel conducting layer will become \_\_\_pinched-off\_\_\_\_.