EE 330 Final Design Projects
Spring 2019

Students may work individually, in groups of 2, or in groups 3 (depending on the project) on the final design project. Partners need not be in the same laboratory section. Please start early on your project, and recognize that projects may require a bit of research and on-your-own learning. If you get stuck on how to accomplish a task, please consult with project's primary TA or with the course instructor for guidance on how to resolve issues that may arise.

READ each project carefully and thoroughly! You will not be able to switch projects once you have been assigned to the project.

A primary TA will be assigned to each project to help you with the project. That TA will be your primary point of contact, but you may address questions to any TA.

Each project may have a maximum number of teams working on the project which will be decided later. A signup sheet will be released and projects assigned first come first serve. We will email the class when the signup will be released so everyone knows when they can sign up.

The project's type (Anlaog, Digital, etc) and Primary TA's name is listed next to the project's name.

Project List

Generally Helpful Notes

Op-Amps

Many projects require or are greatly helped with the use of an Op-Amp. One the course website there are resources to assist with building an Externally Compensated Op-Amp, including a spreadsheet to help design the size of the transistors.

Input and Output components

Many projects require an output display, some require input devices such as keypads. Choosing the correct devices for your project can greatly simplify the project. When choosing which of these devices to use consider what they require sent to them or what information they give you, for example a keypad that sends numbers entered into it in Binary Coded Decimal (BCD) may be more or less useful in your design than one that sends binary data.

Debouncers

When a switch opens or closes it can “bounce”, jumping between digital high and low values multiple times very quickly. A debouncing circuit smooths out the transmission so a switch only changes once, often though an RC time constant.

Comparators

Comparators are going to be used in multiple projects as well. A comparator can be made out of an op-amp, or simpler designs such as transistor-level schmitt triggers.

Analog Switch

There are multiple ways to create analog switches, a switch that uses a signal, normally boolean, to allow an analog signal to pass through. Depending on the complexity of the analog signal this could be a single transistor, or something more complex like a transmission gate.

Microcontrollers Not Allowed

Unless specifically stated in a discrete projects description, microcontrollers are not allowed to be used for these projects.

Project 1: Temperature sensor using diodes [ANALOG] ***OMAR***

Team size = 2/3 students. The project's list of deliverables for a group of 3 will be longer than the deliverables for a group of 2.

This project is for the design of an integrated low power, sensitive, linear temperature sensor with digital output over a temperature range of -20 to 100 °C. The design should be in a 0.18u CMOS process and should include layout and post-layout simulation results.

Digital temperature sensors are used in many devices. They work using the output of temperature dependant devices such as diodes. The design can make use of resistors and diodes/silicon. To generate the basic V_{BE} voltages and hence Proportional To Absolute Temperature (PTAT) voltage and will likely require an op-amp. Design the circuit to use a single 1.8V source and split it into V_{DD}=0.9 V and V_{SS}=-0.9 V.

The temperature should be displayed on a 7-segment display. You must specify the exact display that you will be using for your design. It should drive the display directly without the need for any additional components. You will likely need to create a simple Analog to Digital Converter to display the temperature as digital output. A single slope ADC, comprised of determining how much time it takes to charge a capacitor with the voltage, is advised.

Project 2: Water Fountain Controller [DIGITAL] ***LOGAN***

Team size: 2 students

This project is for the design of a high capacity water fountain controller. The circuit should operate with a dc supply voltage of V_{DD}=1.8V. The design should be in a 0.18u CMOS process and include layout and post-layout simulation results.

In a high-traffic area there is a water fountain that is able to provide both hot water and cold water. The water fountain has two tanks, one for hot water and the other for cold water. The water fountain has a mechanism to heat up or cool down the water. The temperature of the hot water is ideally 160°F and the temperature of the cold water is ideally 40°F. However, during periods of high use, water entering the tanks will change the temperature of the water.

During normal operation under low-use conditions the standard heater for the hot water tank will turn on any time the temperature of the water near the outlet drops to 155°F and then turn off when the temperature reaches 160°F. Correspondingly, any time the temperature of the water near the outlet of the cold-water tank rises above 45°F the standard cooler will turn on and it will turn off when the temperature is reduced to 40°F.

During high use periods, high capacity coolers and heaters will be used. Any time the hot water temperature drops below 150°F the high capacity heater will come on and will turn off when the temperature reaches 160°F. Correspondingly any time the cold-water temperature exceeds 50° degrees, the high capacity cooler will come on and will turn off when the temperature drops to 40°F. Assume the tanks have circulating pumps to keep the temperature in the tanks reasonably uniform.

Each tank has four water level sensors that indicate when the water level is above 95%, above 80%, above 30% or above 20%. Whenever the water level drops below 80% a signal is sent to a valve that turns on the water supply to the tank. Any time the water level reaches 95%, the water entry valve is turned off. The 20% water level sensor is used for safety control. Any time the water level drops below 20% in either tank, all heaters/coolers and valves (except the inlet valve) are turned off for that tank. The valves and heaters/coolers turn back on once the water returns to above 30%.

During high use, replacement water entering the tank may be coming in so fast that the hot water temperature or the cold-water temperature cannot be maintained at the target levels. If the water temperature drops below 148°F in the hot water tank, or above 52°F in the cold-water tank, their respective valves will be disabled. When the water returns to above 148°F in the hot water tank, or below 52°F in the cold-water tank, the vales will be reactivated.

This project involves the design of a controller for this water fountain. Assume the water level sensors have a standard Boolean output that changes states when the set water level is reached. Assume the temperature sensors have an analog output, The

high temperature sensor having an output

$$V_{HIGH}(T) = \begin{cases} 1.8 & T > 165 \\ \dfrac{T-140}{1.8} & 140 < T < 165 \\ 0 & T < 30 \end{cases}$$

The low temperature sensor having an output

$$V_{LOW}(T) = \begin{cases} 1.8 & T > 55 \\ \dfrac{T-30}{1.8} & 30 < T < 55 \\ 0 & T < 30 \end{cases}$$

where T is in degrees F.

Thus, each tank has 4 Boolean outputs summarized as

For hot water tank:

B0: Level above 95%
B1: Level above 80%
B2: Level above 30%
B3: Level above 20%

For cold-water tank:

B4: Level above 95%
B5: Level above 80%
B6: Level above 30%
B7: Level above 20%

The controller is to have 10 Boolean outputs. Each should provide 0V and 1.8V as standard high and low logic levels and should be able to sink or source a load current of at least 25 mA with a change in the high or low logic level of at most 0.5V.

B8: Turn on water to hot water tank
B9: Turn on water to cold water tank
B10: Disable outlet valve on hot water tank
B11: Disable outlet valve on cold water tank
B12: Turn on red LED for water not available in hot water tank
B13: Turn on red LED for water not available in cold water tank
B14: Turn on standard heater in hot water tank
B15: Turn on high capacity heater in hot water tank
B16: Turn on standard cooler in cold water tank
B17: Turn on high capacity cooler in cold water tank

Project 3: Digital Potentiometer/Amplifier/DAC [MIXED SIGNAL]

ABDULLAH

Team size: 2 students

This project is for the design of a digital potentiometer/Amplifier/DAC integrated circuit. The design should be in a 0.18u CMOS process and should include layout and post-layout simulation results.

This multi-purpose digitally controlled analog building block structure can serve as a digital potentiometer, an inverting or noninverting amplifier, or as a DAC depending upon the state control inputs. A method of designing the operational amplifier can be found on the class website under the link for Externally Compensated Op-Amp. Assume V_{DD} =0.9 V and V_{SS} =-0.9V. The state control signal (AO,A1) will identify one of four states of operation of this device. The operation control signals CO, C1, C2 and C3 are used to control the characteristics of the device in each of the four states.

When (A0,A1)=(1,1), the circuit is to perform independently as a digital potentiometer and an operational amplifier. The digital potentiometer should have 16 taps, each with a nominal impedance of 5K.

When (A0,A1)=(1,0), the circuit is to perform as a 4-bit DAC where the op amp is connected in a unity gain configuration to a tap on the potentiometer and the DAC output is determined by the control settings on the potentiometer. The DAC input, often termed “VREF” should be connected to one end of the resistor string and the other end should be grounded.

When (A0,A1)=(0,1), the circuit is to perform as a programmable inverting finite gain amplifier. One end of the resistor string should go to the op amp output, the “wiper” to the “-“ input and the other end of the resistor string to the input.

Finally, when (A0,A1)=(0,0), the circuit is to perform as a programmable noninverting finite gain amplifier.

The digital potentiometer is similar in principle to the Maxim DS 1666 but with a reduced number of taps, with parallel rather than serial control of the tap position, and with a linear taper rather than an audio taper. This device will need an analog MUX.

Project 4: Optical Transmitter/Receiver [HARDWARE] ***ANTHONY***

Team size: 2 students

Create an optical transmitter and receiver that will work together to create an audio-visual presentation. The receiver should be able to receive and make decisions on the signal from at least 2 feet.

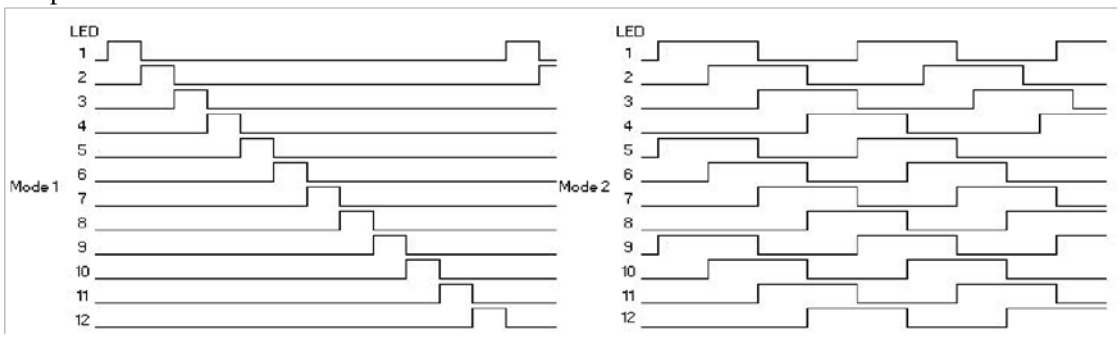
The transmitter should be able to transmit an audio signal and generate and send two different control signals. You may control which signals are being sent with buttons, switches, etc.

1. Audio
    a. Send audio signal between 10 Hz and 10k Hz, this can be generated by a computer in lab, a cell phone, etc.
2. Visual Control Signals
    a. Generate and send one of two constant signals in each of the visual control bands, 15k-20k Hz and 25k-30k Hz.
3. Audio and Visual
    a. Mix the two signals above so the receiver gets both the audio signal and one of the two visual control signals. It should be able to send either visual signal with the audio.

The receiver shall determine what signal is being sent and activate lights or speakers. It should be able to run in both modes at the same time.

1. Audio
   When the receiver detects a signal below 10k Hz the receiver will play the signal as audio through speakers. This mode may be active at all times.
2. Visual Display
   When the receiver detects a signal between 15k-20k Hz and 25k-30k Hz the receiver will blink a bank of 12 LEDs. If no signal in these ranges is detected, neither mode should be active.
    a. Mode 1: When the incoming signals is between 15k-20k Hz the 12 LEDs should blink in series, one after another. Each should turn on for half a second, then when it turns off the next in line should blink. When the series gets to the end of the line of LEDs start back at the beginning.
    b. Mode 2: When the incoming signal is between 25k-30k Hz the 12 LEDs should blink as groups. Have the LEDs split into four groups of three. Have them blink at 0.75 Hz, with two groups on at the same time, but stagger their blinking so a switch happens at 1.5 Hz (ex: group 2 will turn on half-way through the cycle of group 1, group 3 will turn on half-way through the cycle of group 2, etc.) The timing diagram below shows how these groups will cycle through each other.

Example of LED Waveforms for mode 1 and mode 2



Project 5: PUF [ANALOG] ***KUSHAGRA***

Team size: 2 students

The project is for the design of an integrated Physically Unclonable Function(PUF) circuit which can be used to authenticate silicon chips. The design should be in a 0.18u CMOS process and include layout and post-layout simulation results.

Within the semiconductor industry there is a problem with simple components being counterfeited and sold illegally. In an attempt to prevent this the industry has the idea of using PUFs, small circuits that can be added without affecting the chip but which can be used to uniquely identify the component. They work by exploiting the random component of manufacturing variations to create a digital device that provides unique IDs for each IC chip. By using components that start up when the device is turned on, but rather they produce a 1 or 0 at startup is considered a 50-50 chance, decided by manufacturing defects. Once manufactured this creates a unique binary string which is different for every chip, and using a long enough string the chances of any two ever having the same bit string approaches zero.

Design a 32-bit PUF having pins Vdd, Gnd, Vout, clock out (90 degree shifted clock signal), and output serially. Include a monte-carlo simulation showing the random data output of your design.

Project 6: Nonsynchronous Traffic Intersection Controller [DIGITAL] ***PRAISE***

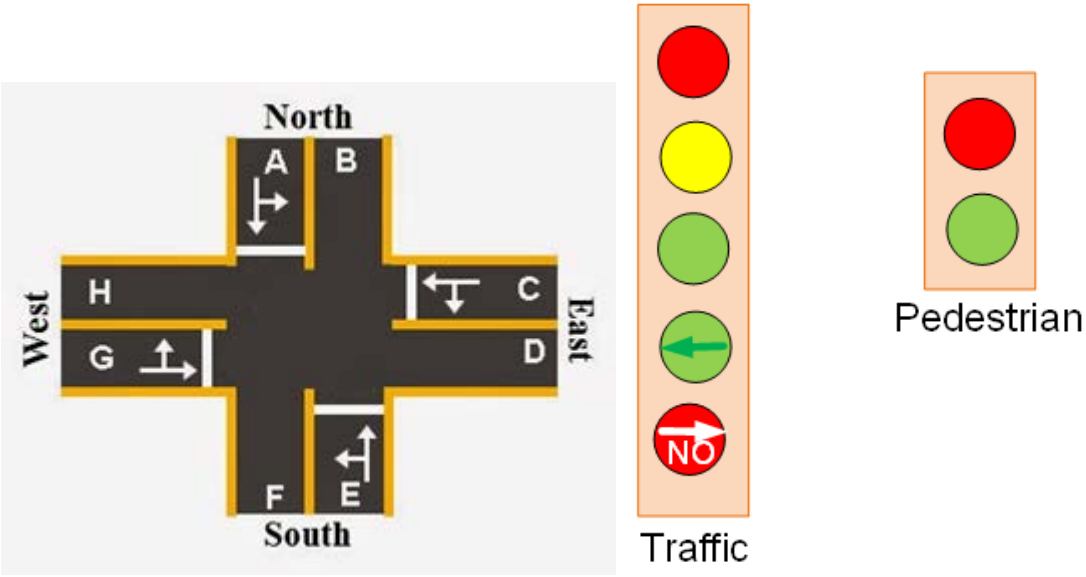
Team size: 2 students

This project is for the design of a 4-way traffic intersection controller. The design should be in a 0.18u CMOS process and include layout and post-layout simulation results. The circuit should operate with a dc supply voltage of V_{DD}=1.8V.

The controller will have 8 inputs and 20 outputs for traffic lights and 16 outputs for pedestrian crossing light and 16 outputs for each pedestrian crossing request acknowledgement. The inputs are push-button inputs with two buttons located at each corner of the intersection for the purpose of pedestrian interrupts that allow the pedestrian to request a green pedestrian crosswalk light for crossing the intersection in either direction. The outputs should all be a port that can drive a 5V, 1mA incandescent lamp (by sinking current) when "ON" The voltage drop across the port should be at most 500mV when carrying a current of up to 1mA. The 1mA lights are meant to model the traffic lights and the crosswalk lights.

There will be four clusters of 5 traffic lights facing each direction. The lights in each cluster, as depicted below, will be designated as Red (R), Green (R), Yellow (Y), Left Turn (LT), and No Right Turn (NRT). There will be 8 clusters of 2 pedestrian crosswalk lights. The lights in each crosswalk cluster, as depicted below, will be designated as Walk (W) and don't walk (DW). Red and Green will be used for W and DW respectively. There will be an indicator light by each pedestrian request light button.

The vehicular traffic flow can be classified into four phases as described by the traffic intersection depicted in the following figure. In the intersection vehicles are allowed to make a right turn on Red or Green provided they do not cross an active pedestrian crosswalk. A description of the system based upon a 4-phase model follows.



PHASE I-East/West

- Green signal in A and E permits vehicles to pass through while red will appear for east and west roads to stop east/west travel

PHASE II-North/South

- Green signal in C and G permits vehicles to pass through while red will appear for north and south roads to stop north/south travel

PHASE III-East/West Left Turn

- Green signal in LT permits vehicles to make left turns from A to D and from E to H. Other traffic flow is stopped.

PHASE IV-North/South Left Turn

- Green signal in LT permits vehicles to make left turns from G to B and from C to F. Other traffic flow is stopped.

The cycle repeats itself continuously jumping to Phase I every time Phase IV is completed.

Timing of the signals:

Programming should be done such that in every phase the red signal will be on for 60 sec yellow will be on for 15 seconds and green will be on for 45 seconds before switching the flow to the next phase except when a pedestrian interrupt occurs. During normal operation during Phase 1 and Phase 2, pedestrians moving in East and West directions will have a green light when the East and West traffic flow light is green and pedestrians moving in the North and South directions will have a green light when the North and South Traffic lights are green irrespective of whether a valid pedestrian interrupt occurs. Correspondingly, during normal operation, during Phase 3 and Phase 4 pedestrians that will not cross an active left-turn path will have a green light irrespective of whether a valid pedestrian interrupt occurs. Any time a pedestrian interrupt occurs, the NRT light will prevent a right hand turn for the requested pedestrian path crossing for the immediately following phase that would have a right turn cross a requested pedestrian path. (If the request for a pedestrian crossing occurs during the time which a pedestrian crossing will conflict with an active right turn traffic path, the request will be treated as if it occurred just after the corresponding phase is completed). All pedestrian path crossings will be of duration 30 sec. and will be coincident with the first 30 seconds of the corresponding 45 second green traffic path lights. The pedestrian crossing lights will always be red for the last 15 seconds of a green traffic path light.

An interrupt requires that a request button be pressed for a minimum of 5 seconds and the interrupt becomes valid only after the 5 seconds elapses. If the duration of the request is less than 5 seconds, it is ignored. The request acknowledgement light should turn on as soon as a valid request has been detected and remain on until the resultant crossing path has been made available to the pedestrian and turn off only after the corresponding pedestrian path light turns red. Multiple pressings of the pedestrian request button should be ignored if the acknowledgement light is still on.

The clock signal should be generated internally. Each phase is designated to last for 60 seconds but process variations will make it difficult to generate a clock that has an absolute accuracy of 60 sec. The circuit should be designed so that the nominal phase period is 60 seconds. Since the clock period can vary somewhat, this is a nonsynchronous traffic controller and would be most suitable for use where traffic lights are isolate and not coordinated with other traffic lights in the immediate vicinity.

Note that Students **may** be required to demonstrate and present their project using Simulink (Matlab) as test bench. With this, the traffic lights can be seen more clearly and simulated instead of just observing 1's and 0's with Verilog test bench.

Since the project involves a lot of signals and time interrupts, a strong knowledge of Verilog coding and syntax will be considered an added advantage. Before the project starts, teams will be briefed about the project to answer confusing questions and avoid ambiguous definitions on traffic issues.

Project 7: Self-Defined

Team size: 2 students

This project will be personalized to the individual interests of the students. All proposals for the self-defined projects should be approved by the course instructor. Self-defined projects can be either for an integrated circuit design or for a hardware implementation.

No primary TA will be assigned to supervise self-defined projects. The TAs will help you with general issues, but you are responsible to solve the more in-depth problems.