**EE435**

**Lab3: Design a common source amplifier**

**Objective:** In this lab you will design a common source amplifier which should meet all the specifications listed below.

**The op-amp should achieve:**

* Output swing range: 4v
* Slew rate: 40V/us
* Gain bandwidth:40MHz
* DC gain: at least 35 dB

**Available device:**

* Current source Iref=10uA
* Power supply: Vdd=5v, Vss=0v
* Load capacitor CL=5pF
* MOSFETS you can choose the channel length of 1.5Lmin, 2Lmin

**Report requirements:**

* Test bench and results for the specifications
* Briefly discuss your sizing strategy
* Report the output resistance
* Show bode plot (both magnitude and phase)
* Report the phase margin

**Additional task:**

If you still have time after doing above parts you can try to measure the closed loop gain by adding two resistors.