**EE435**

**Lab4: Design a common source amplifier**

**Objective:** In this lab you will design a differential amplifier with the common source (CS) amplifier we designed last week. The specifications listed below.

**Specifications:**

* Output swing range: 4v
* Slew rate: 40V/us
* Gain bandwidth Product:40MHz
* DC gain: at least 35 dB and 70dB for the Cascode structure
* Current source Iref=10uA
* Power supply: Vdd=5v, Vss=0v
* Load capacitor CL=5pF
* MOSFETS you can choose the channel length of 1.5Lmin, 2Lmin

**Part 1**

Starting from your CS, design a differential pair with the output branch. Add an additional transistor and fine tune its bias (Vi\_Q) so that the outputs (+/-) are exactly in the middle of the output swing range. A good starting point can be the Vin\_Q of last week’s CS amplifier. Note that your tail current has to be double last week’s value. Also, connect the gate of the pmos of the differential pair to the pmos gate of the CS amplifier.

Now apply a common mode voltage +/- half differential voltage at the (+) and (-) input respectively and fine tune Vi\_Q again. It is important to notice that this is a painful process.

**Part 2:**

In this part, we will use the (-) output to bias the gate of the pmos and get rid of the CS amplifier. This will introduce some offset at the output that needs to be tune so that the output voltage is exactly in the middle of the swing range.

**Part 3:**

Using the differential amplifier in part 1, we are going to design a differential cascade amplifier using the same sizes. To bias the new transistor, you can use Vb\_pmos -1.5Veffp and Vic + 1.3Veff\_n. Again, here you will need to readjust the Vi\_Q of the tail transistor to provide the correct output quiescent voltage.

**Report requirements:**

* Test bench and results for the specifications
* Briefly discuss your sizing strategy
* Report the output resistance
* Show bode plot (both magnitude and phase)
* Report the phase margin