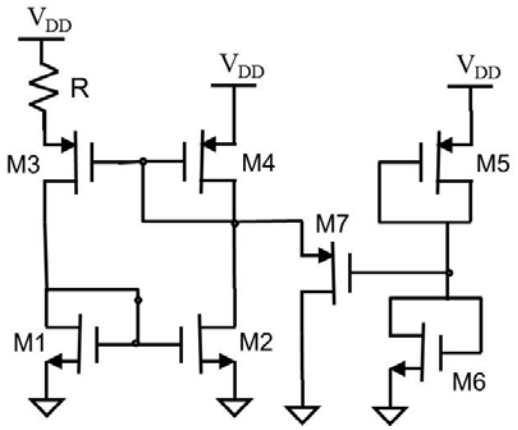
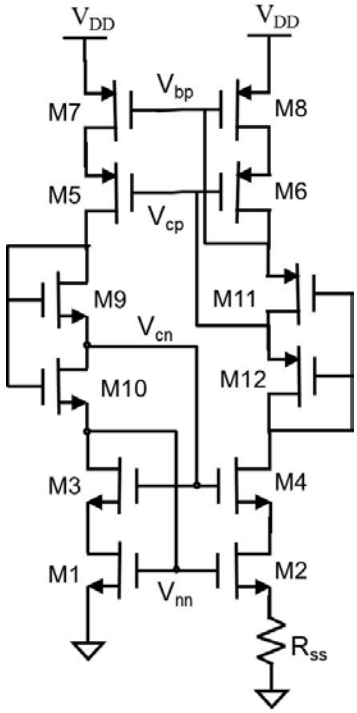
HW 6

1. Shown to the right is the p-version of the Widlar structure. Suppose we want an Iref of 10 uA. The desired Veff for M1, M2, and M4 are all 0.5V. For convenience we want M3 to have Veff = 0.25 V. For better robustness, we want to use L=4Lmin.
   a. Finish the design for M1-M4 and R.
   b. Design a start-up circuit. Size M5 and M6 to have Wmin and large L so that current very small (<1uA), and that Vg7 is about Vg4 – |Vtp| + V_{eff4}/2. Size M7 to be minimum size. Explain how the start-up circuit works.
   c. Enter your design into Cadence. Adjust R to achieve approximately the right Iref in DC analysis with VDD=5V.
   d. Do a transient simulation to gradually ramp up VDD from 0V to 6V in 0.1 second. (This is simulating the power up process.)
   e. Plot Id1, Id7, Id5, and VDD vs time. Comment on the graph.



2. Shown to the right is a self-biased cascoded Iref generator. We want: Iref ≈ 10uA, Veff ≈ 0.5V and L=4Lmin for M1, M7 and M8, Veff ≈ 0.25V and L=2Lmin for M2, M3, M4, M5, and M6. M9 to M12 are up to you. Size all transistors and Rss. Ensure all transistors to be in saturation. What is the smallest VDD that can be used? Add a suitable start-up circuit. Describe advantages and disadvantages of this Iref generator as compared to the one in problem 1.



3. 7.4
4. 7.8
5. 7.12
6. 7.17