HW8, Due time: Friday 4/5 in class.

Consider the three circuits shown below. In class, we analyzed the performance assuming identical biasing currents in all transistors. In this problem, each circuit is to have the same total currents. That is, the second circuit will have ½ the current in each transistor, and the third circuit will have 1/3 current in each transistor, as compared to the first circuit. Assume all Cp's are equal, each stage in a multi-stage circuit has an Ro to make each stage to have the same gain, and the total gain of each circuit is the same. Approximate each circuit to have an overall equivalent first order response.
a) Find the equivalent time constant. b) Estimate the propagation delay. c) Determine a strategy to decide on the number of stages to use. d) What Cpi's depend on? e) If you keep all transistors to have the same Veff's, how does that affect your results?



- 2. In class, we talked about how an external positive feedback can create a hysteresis loop in a comparator.
 - a. Carry out the analysis assuming the circuit represented by the triangle to be an ideal comparator. Obtain the transfer curves.
 - b. What is the effective resolution of the comparator with hysteresis?
 - c. If the triangle has an offset voltage Vos, how does that change the hysteresis loop?



- 3. 10.1
- 4. 10.2
- 5. 10.4
- 6. 10.9
- 7. 10.11
- 8. 10.5 (bonus)
- 9. 10.12 (bonus)