1. For the position control system shown bellow, find the value of preamplifier gain, K, to yield a 9.5% overshoot in the transient response for a step input. Use only frequency response methods.

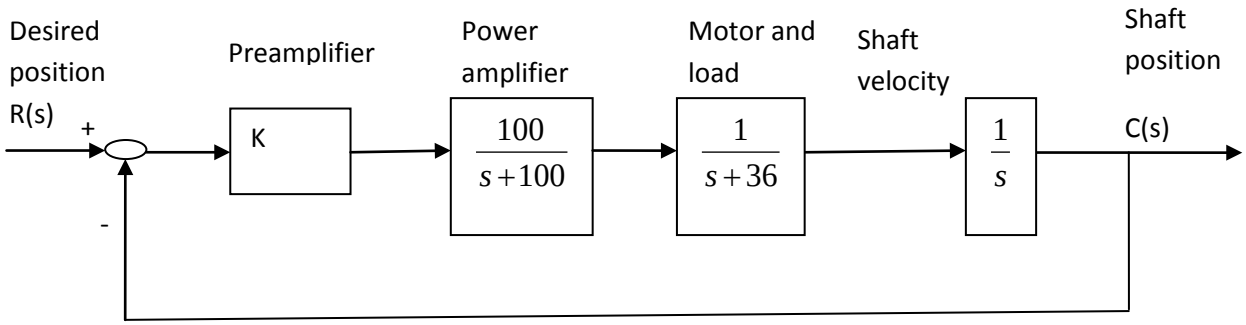

Figure 1

2. Given the system of Figure 1, use Bode diagrams to design a lag compensator to yield a tenfold improvement in steady-state error over the gain –compensated system while keeping the percent overshoot at 9.5%.
3. For a unity feedback system with a forward transfer function

$$G(s) = \frac{K}{s(s+50)(s+120)}$$

Design a lag compensator for the system that will improve the steady-state error tenfold, while still operating with 20% overshoot.

4. Given the system of Figure 1, design a lead compensator to yield a 20% overshoot and Kv=40, with a peak time of 0.1 second.
5. For a unity feedback system with a forward transfer function

$$G(s) = \frac{K}{s(s+50)(s+120)}$$

Design a lead compensator for the system to meet the following specification: %OS=20%, Ts=0.2s, and Kv=50.

6. Given a unity feedback system where

$$G(s) = \frac{K}{s(s+1)(s+4)}$$

Design a passive lag-lead compensator using Bode diagrams to yield a 13.25% overshoot, a peak time of 2 seconds, and Kv=12.

7. Design a lag-lead compensator for a unity feedback system with the forward-path transfer function

$$G(s) = \frac{K}{s(s+8)(s+30)}$$

to meet the following specifications: %OS=10%, Tp=0.6s, and Kv=10. Use the frequency response techniques.

8. Given the antenna azimuth position control system block diagram, use frequency response techniques and design cascade compensation for a closed-loop response of 20% overshoot for a step input, a fivefold improvement in steady-state error over the gain-compensated system operating at 20% overshoot, and a settling time of 3.5 seconds. (Note: Differential preamplifier: K, and Power amplifier: $\frac{K1}{s+a}$)

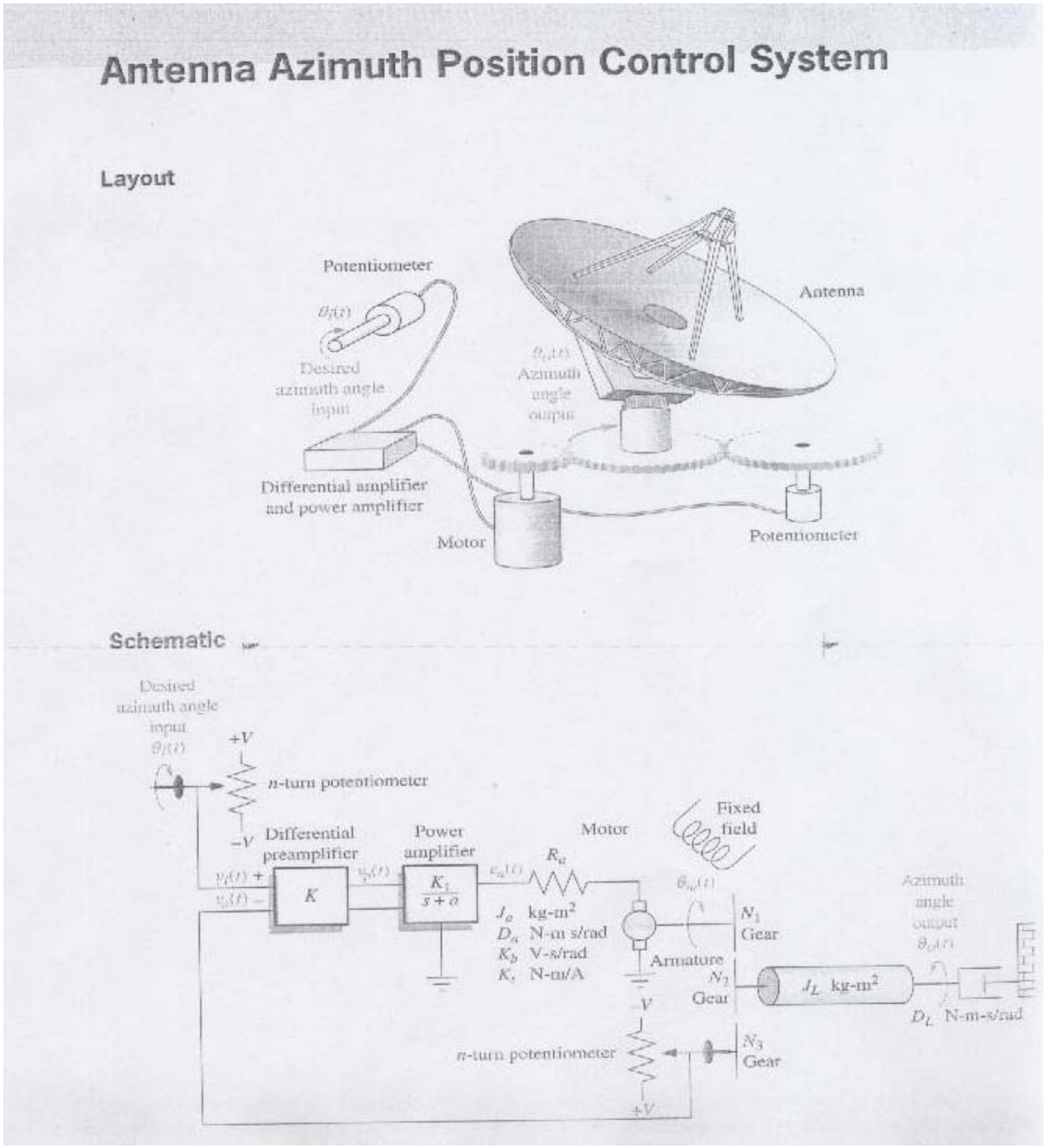

Figure 2

9. Consider the system shown bellow, it is desired to design a PID controller $G_c(s)$ such that the closed loop system step response will have ≤16% overshoot and ±1% settling time is ≤ 5seconds. For the PID controller, choose a=0.2 and then determine the values of K and b.

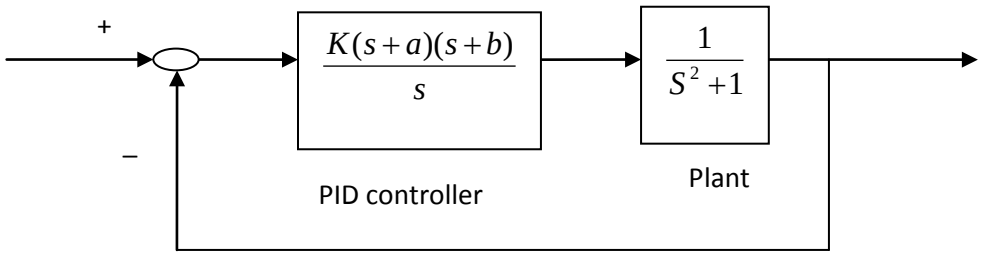

Figure 3

10. Consider the system shown bellow. That is a PID control of a second-order plant G(s). Assume that disturbance $U_d(s)$ enter the system as shown in the diagram. It is assumed that the reference input r(t) is normally held constant, and the response characteristics to disturbances are a very important consideration in this system.

    Design a control system such that the response to any step disturbance is damped out quickly (in 2 to 3 second in terms of 2% settling time). Furthermore, the reference step response should also settle in less than 2 to 3 seconds, and should have <10% overshoot. After your design, you should obtain the response to the unit-step disturbance input, and also obtain the response to the unit-step reference input.

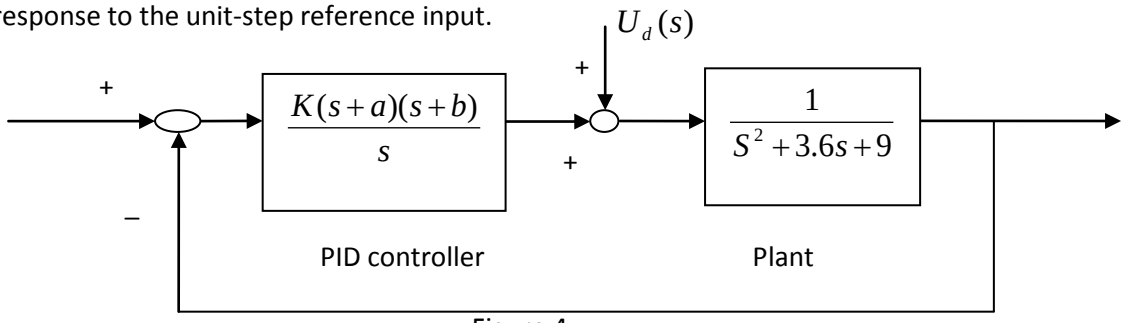

Figure 4