EE 475 HW #7

1. For the system given on slide 14 of lecture 16, design a PD controller to achieve: Mp ~<= 10% and tr ~<= 0.8 sec. You may have to tune your design but give the final version of your controller TF and the annotate step response for verification.
2. Redo the above problem with a lead controller instead of a PD controller. Do it with two methods: a) select your lead zero by mouse, b) bisection. Give your final controller TF and the annotated closed-loop closed loop step response.
3. For the system given on slide 24 of lecture 17, design a lead-lag controller to achieve the following time domain specifications: Mp ~<= 10%, ts ~<= 7 sec, tr ~<= 3 sec, ess to step = 0, and ess to ramp ~<= 0.2.
4. Redo the above problem with desired ess to ramp = 0. In this case, you have to use a PI. So your overall controller could be either a lead-PI, or a PID.
5. For the system given on slide 33 and specifications given on slide 35 in lecture 17 except ess to ramp = 0, design a PID controller and verify your design.
6. For the system given on slide 33 of lecture 18, add another requirement: ts ~<= 1 sec. Design a whatever controller to achieve the specifications.
7. Design a lead-lag for a plant with TF $G(s) = \frac{1}{s^2(s+5)}$, and achieve the following design specifications: Mp <= 15%, tr <= 1 sec, and ess to acceleration <= 0.5.
8. B-6-22, but target a Mp of 15% and ess to ramp <= ¼.
9. B-6-21, replace specs by: Mp<=20%, ts<=2s (tol=2%), tr<=0.5s, ess_ramp <=0.01.
10. For the system given in Figure 7-166 (B-7-32), design a controller to achieve the following specifications: ts <=1.5 sec, tr <= 0.5 sec, Mp <= 12%, and ess to a unit acceleration signal is <=2.5.