EE 501 Analog IC Design

- **Instructor Contact Information**

  Degang Chen, 329 Durham

  djchen@iastate.edu; 294-6277

  Office Hour: MWF 12:00 – 2:00 pm

  or any other time that I am available

  Please include "EE501" in the subject line in all email communications to avoid auto-deleting or junk-filtering

- **TA**

  To be announced

Class Webpage

- http://class.ece.iastate.edu/djchen/ee501/
  - Currently pointing to old web site
  - Will ask csg to fix and let you know
- Please check the page for
  - Any announcement
  - Class notes
  - HW assignments
  - Lab assignments
  - Final project requirements
  - Class policy and other info

Course Description

- Design techniques for analog and mixed-signal VLSI circuits.
- Amplifiers: operational amplifiers, transconductance amplifiers, finite gain amplifiers and current amplifiers.
- Linear building block: differential amplifiers, current mirrors, references, cascoding and buffering.
- Performance characterization of linear integrated circuits: offset, noise, sensitivity and stability.
- Layout considerations, simulation, yield and modeling for high-performance linear integrated circuits.
- CAD tools: Cadence.

Final Grade Weighting

- Laboratory: 25%
- Final project: 20%
- Homework: 20%
- Midterm Exams: 15%
- Final exam: 20%

- Bonus for original creative work (publishable/patentable work)

Fabrication Privilege

- Circuit fabrication is not required for the course
- It is offered free as a privilege
- Requirements for this privilege
  - Detailed simulation results demonstrating that circuit is highly likely to work
  - Sufficient testing plan (what to measure and how)
  - Promise to test (availability and commitment of time)
  - Promise to submit a satisfactory report to MOSIS
- Benefits:
  - Valuable experience
  - Increased marketibility
- Limits: max two submission per student

Required Text Book

- Allen and Holberg, *CMOS Analog Circuit Design,* 2nd Edition, Oxford, 2002
- Available at Amazon
  - Significant discounts vs bookstore
  - Links in a previous email

References

- Gray, *et al, Analysis and Design of Analog Integrated Circuits,* 4th Ed., Wiley, 2001
- Hastings, *The Art of Analog Layout,* Prentice Hall, 2nd ed
- William Liu, *Mosfet Models for Spice Simulation, Including BSIM3v3 and BSIM4*, Wiley-IEEE, 2001
- Daniel P. Foty, *MOSFET Modeling With SPICE: Principles and Practice,* Prentice Hall, 1996
- Yannis Tsividis, *Operation and Modeling of the MOS Transistor,* Oxford University Press; 2nd edition (May 1, 2003)
- Laker and Sansen, *Design of Analog Integrated Circuits,* McGraw Hill, 1994
- David Johns & Ken Martin , *Analog Integrated Circuit Design*, John Wiley & Sons, Inc. 1997
- Behzad Razavi, *Design of Analog CMOS Integrated,* CircuitsMcGraw-Hill, 1999
- Geiger, *et al, VLSI Design Techniques for Analog and Digital Circuit*, McGraw Hill, 1990

- Baker, *CMOS Circuit Design, Layout and Simulation,* IEEE Press, 1997
- Alan B. Grebene, *Bipolar and MOS Analog Integrated Circuit Design* (Wiley Classics Library), 2001

MOSIS links

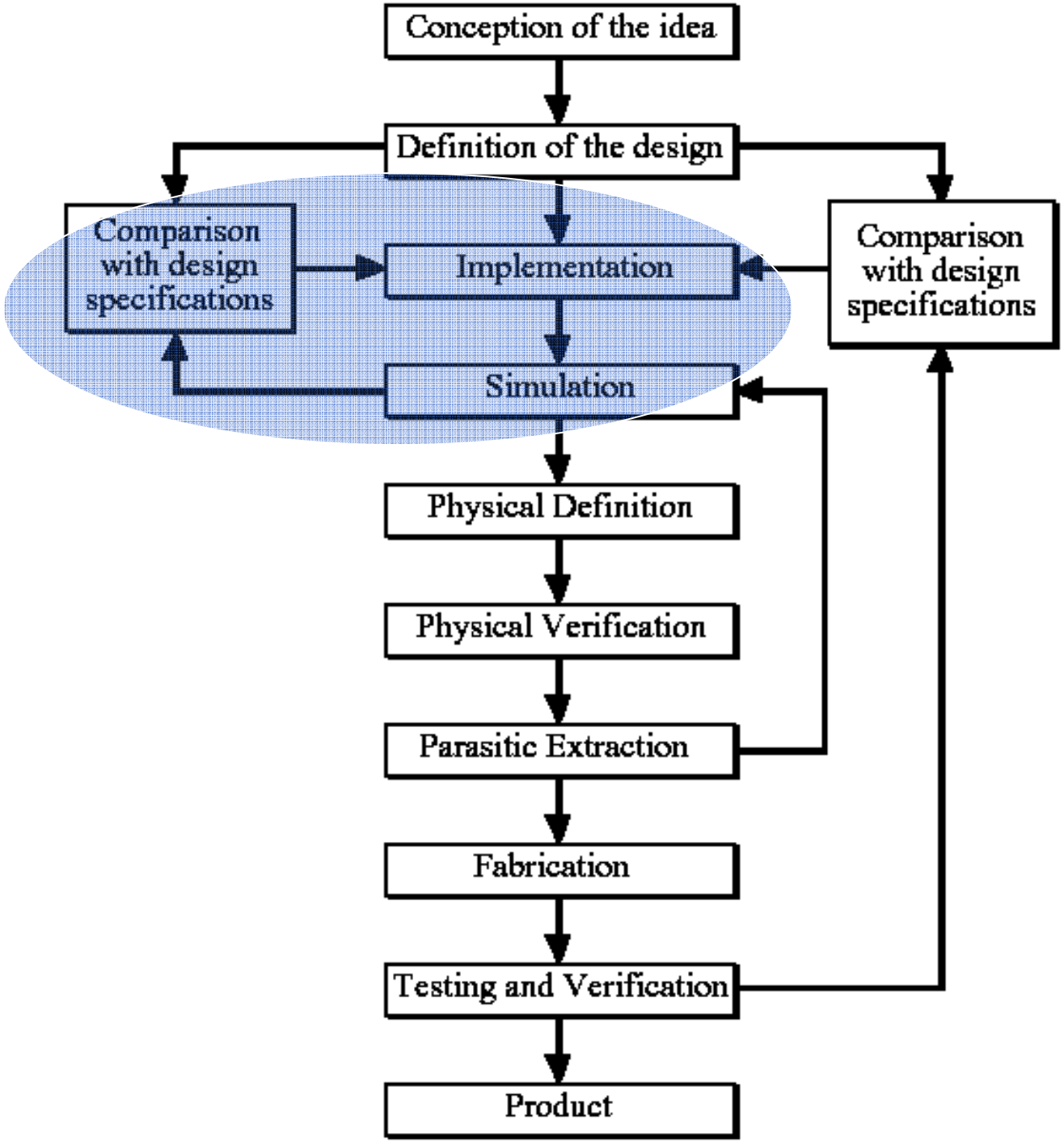
- MOSIS web site
- FAQ from comp.lsi.cad
- MOSIS scalable design rules
- MOSIS Pads directory.
- Process description: TSMC 0.25, AMI 0.5
- SPICE model parameters: TSMC 0.25, AMI 0.5

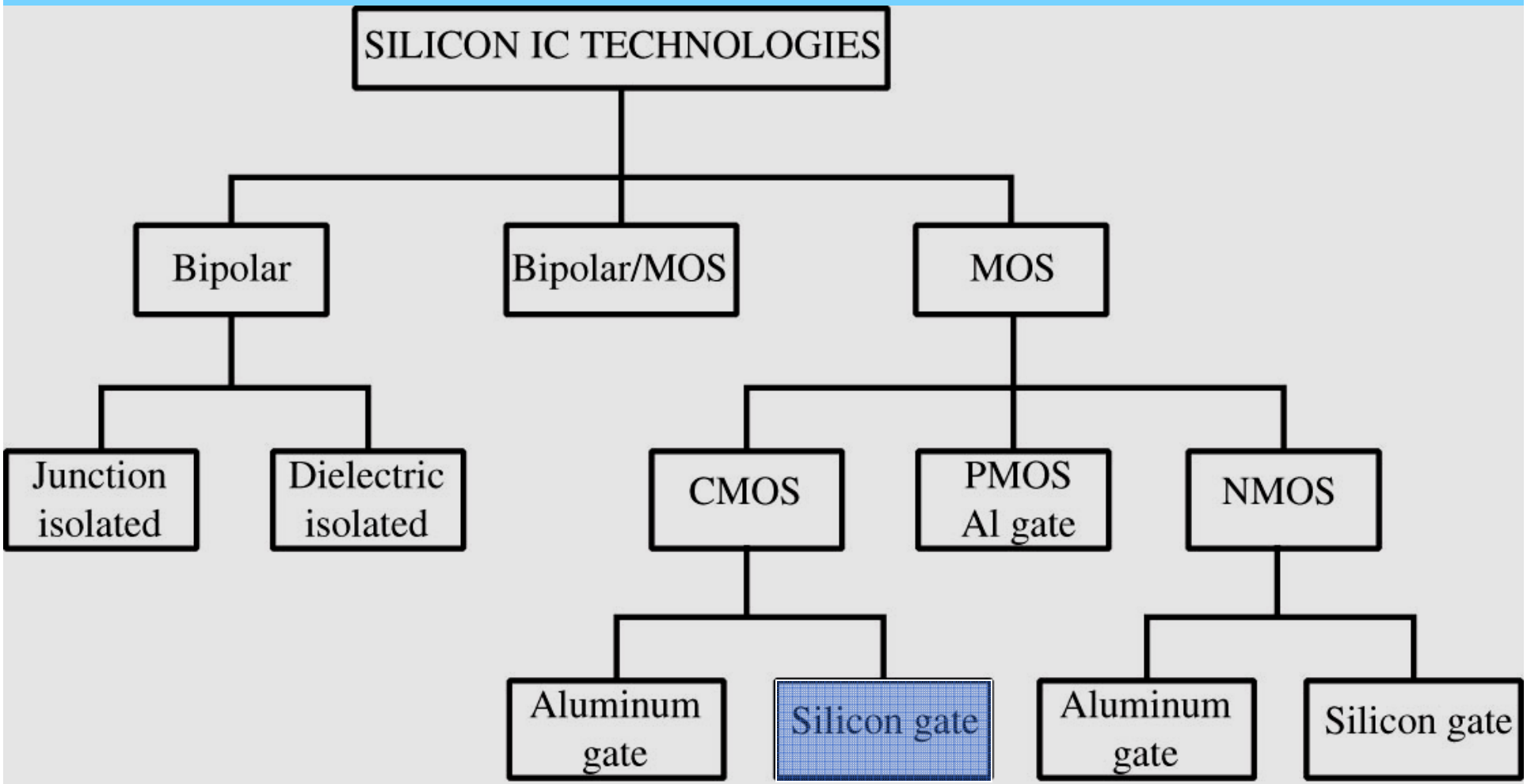
Links for information sources

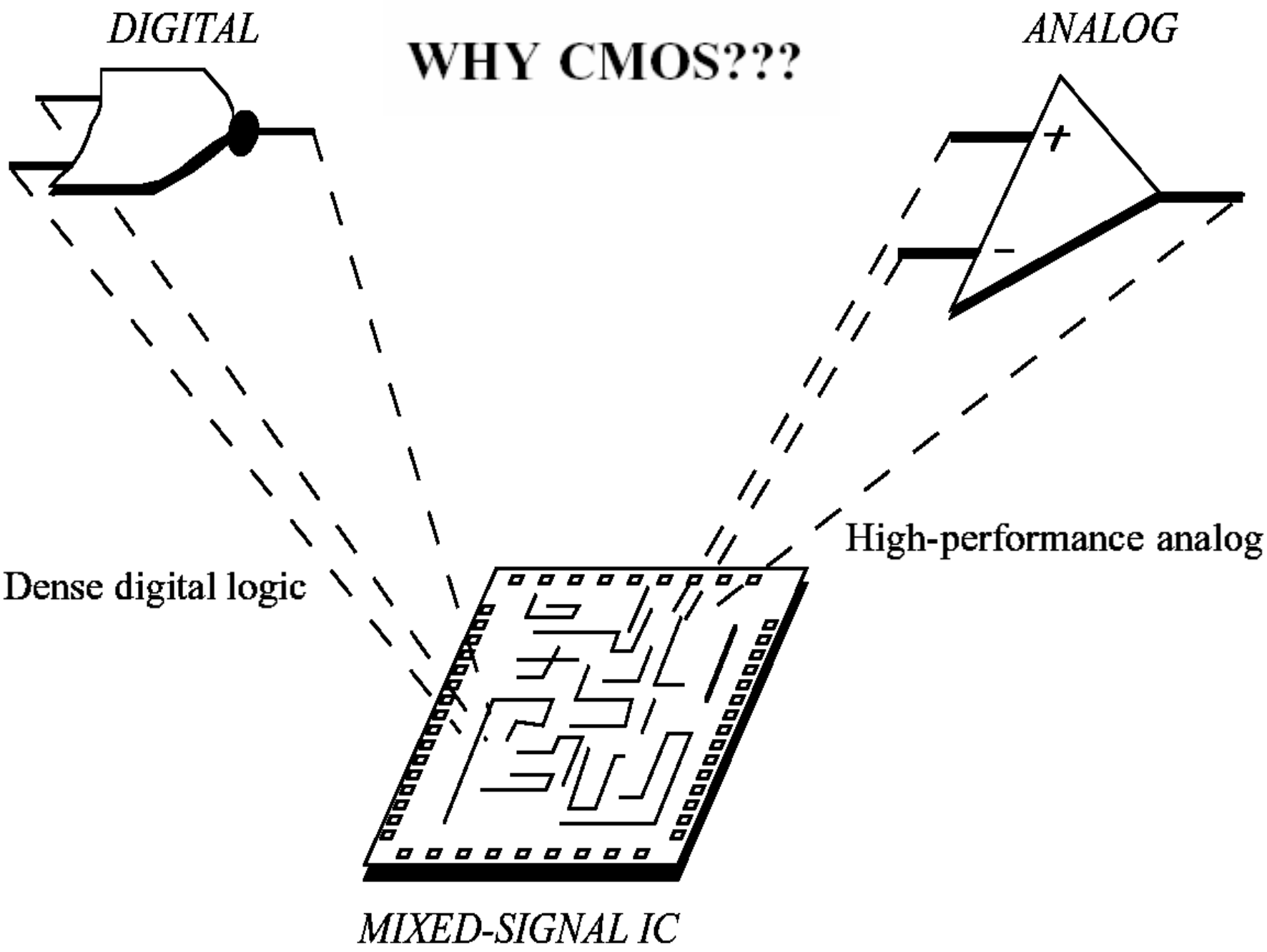
- IEEE IEL
- Science Citation Index / ISI Web of Knowledge
- U.S. Patent Office
- International Technology Roadmap for Semiconductors
- Semiconductor Research Corporation

Links for technical writing

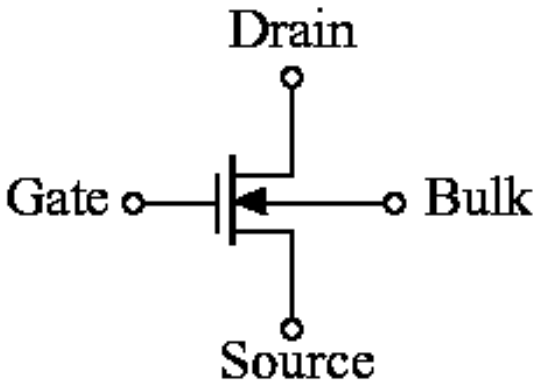
- Things to think about while writing papers
- A nuts and bolts guide to college writing
- The Barleby refence site
- William Shrunk's "Elements of Style"
- Dictionary.com
- Visual Thesaurus
- Latex style files for IEEE journals


Conception of the idea
Definition of the design
Comparison with design specifications
Implementation
Simulation
Comparison with design specifications
Physical Definition
Physical Verification
Parasitic Extraction
Fabrication
Testing and Verification
Product

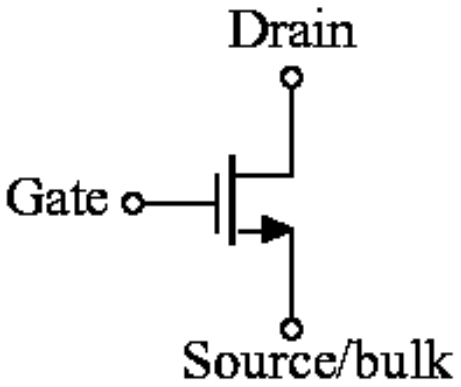

SILICON IC TECHNOLOGIES
Bipolar
Bipolar/MOS
MOS
Junction isolated
Dielectric isolated
CMOS
PMOS Al gate
NMOS
Aluminum gate
Silicon gate
Aluminum gate
Silicon gate


DIGITAL
WHY CMOS???
ANALOG
+
–
High-performance analog
Dense digital logic
MIXED-SIGNAL IC

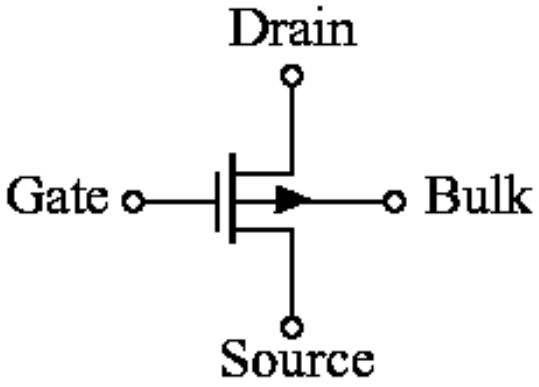
NOTATION



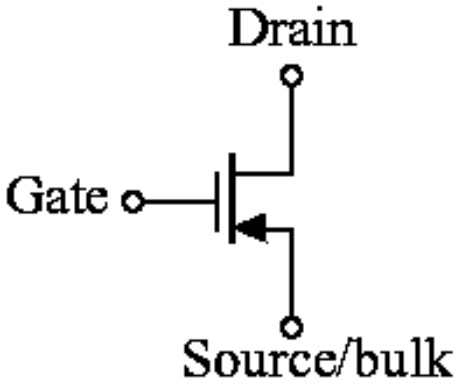
n-channel, enhancement, $V_{BS} \neq 0$



n-channel, enhancement, bulk at most negative supply

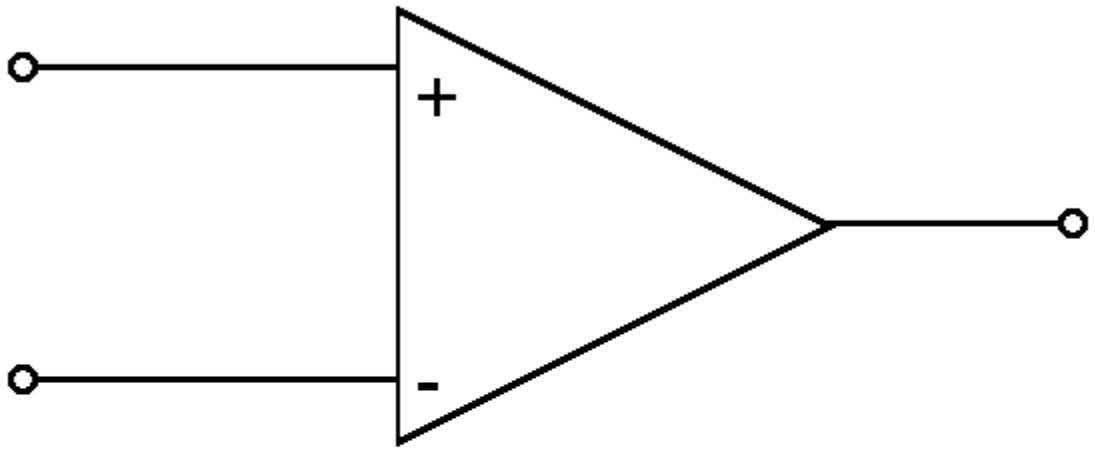


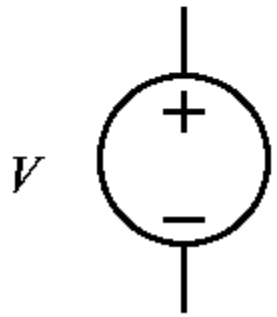
p-channel, enhancement, $V_{BS} \neq 0$

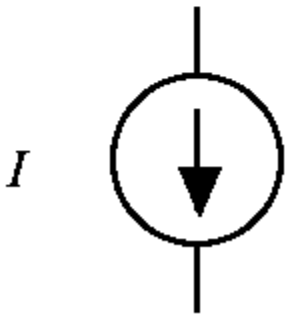


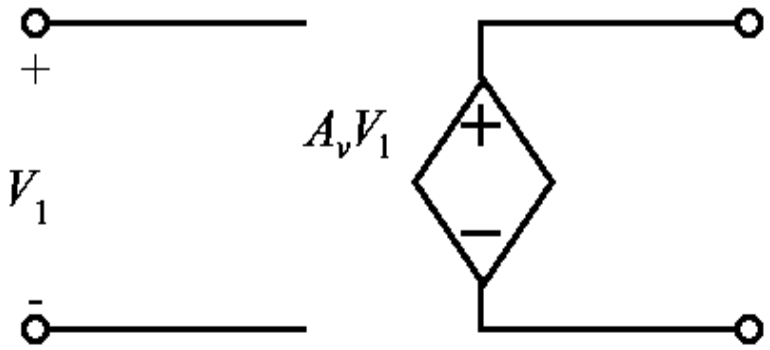
p-channel, enhancement, bulk at most positive supply

Operational Amplifier/Amplifier/OTA

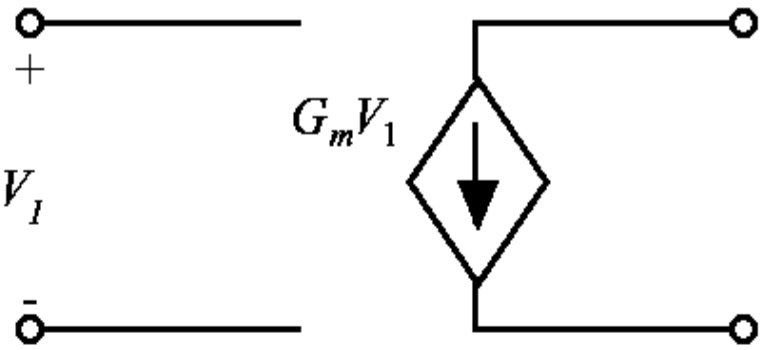




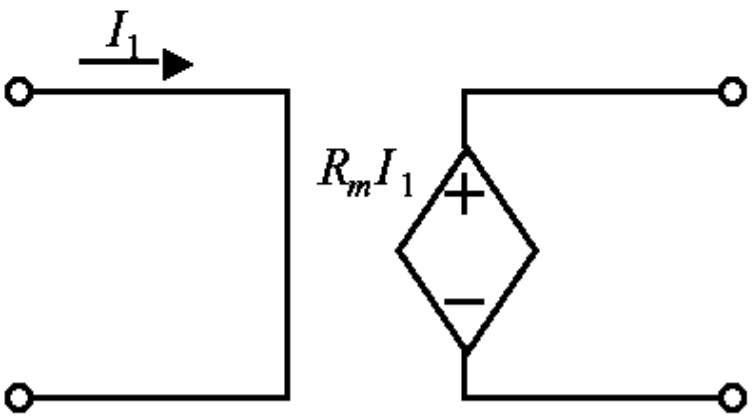




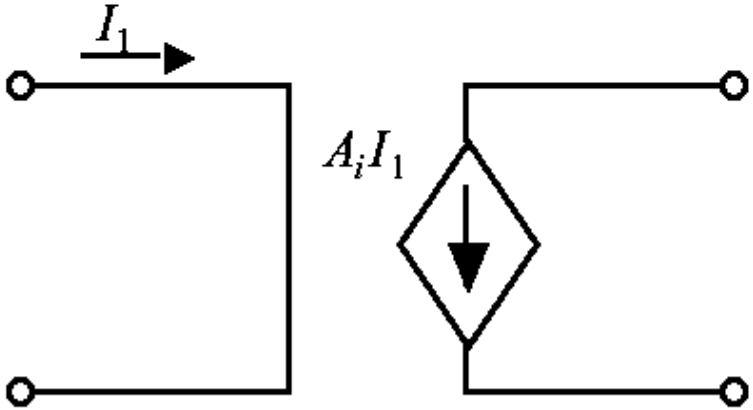
VCVS



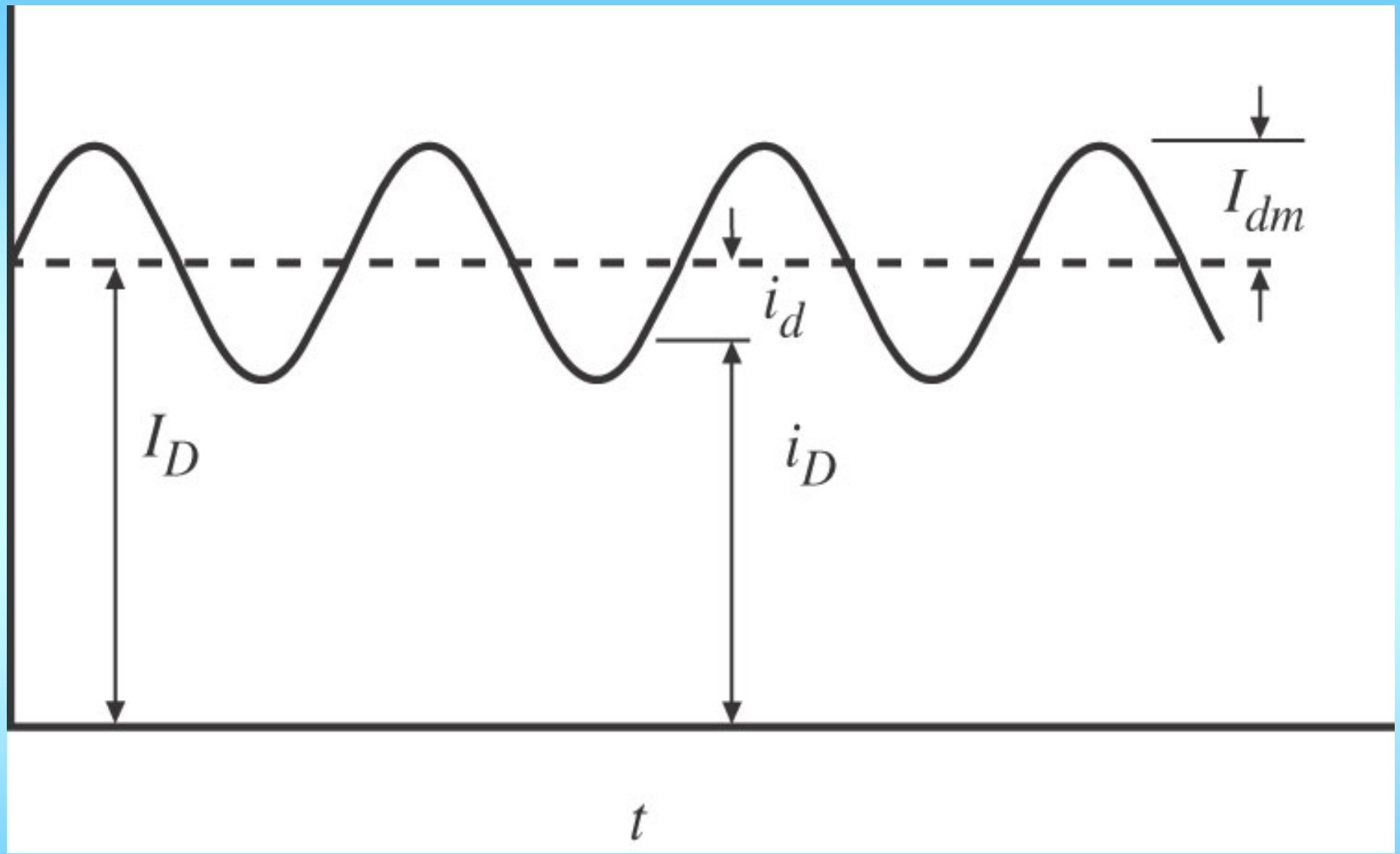
VCCS



CCVS

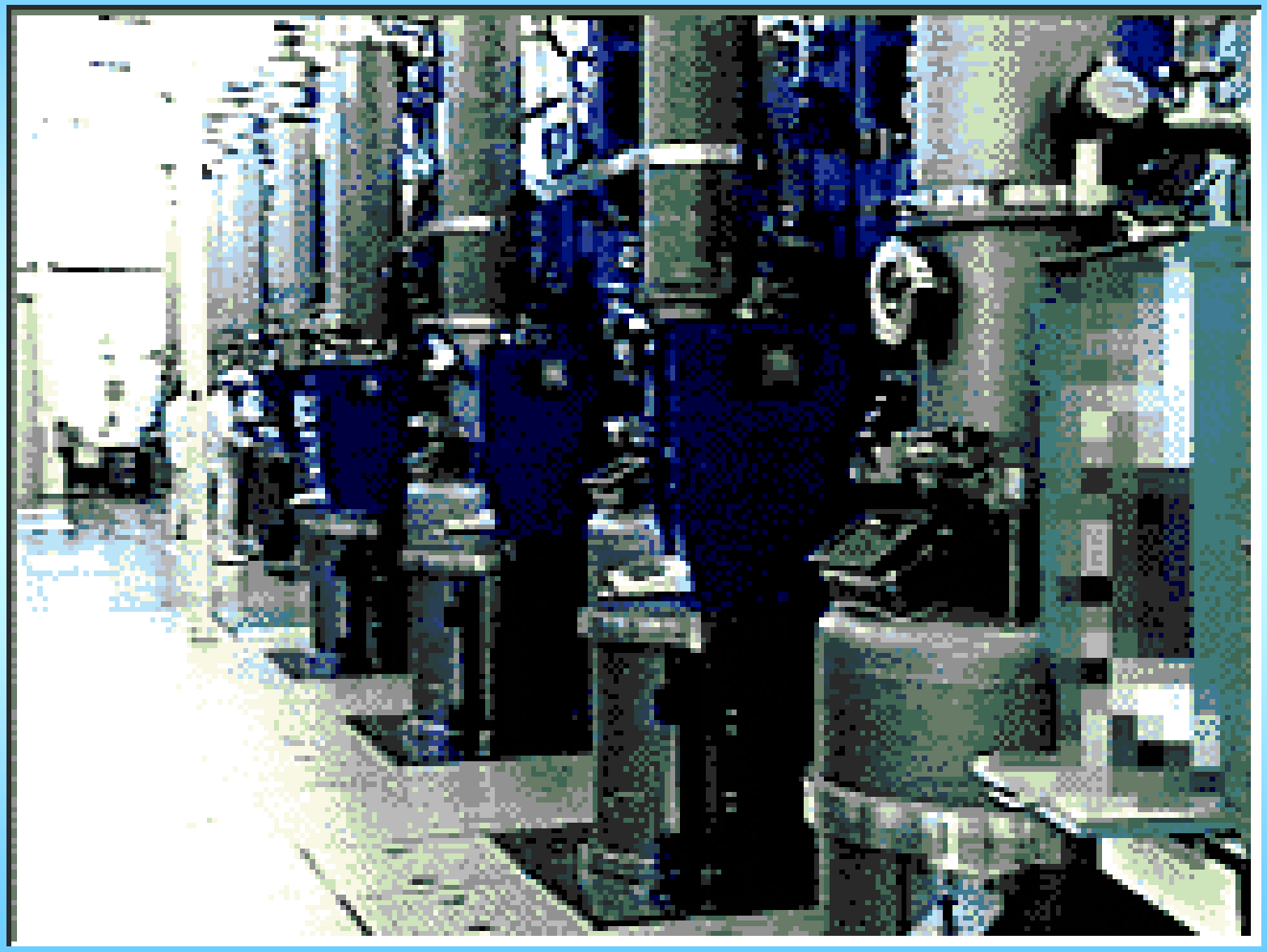


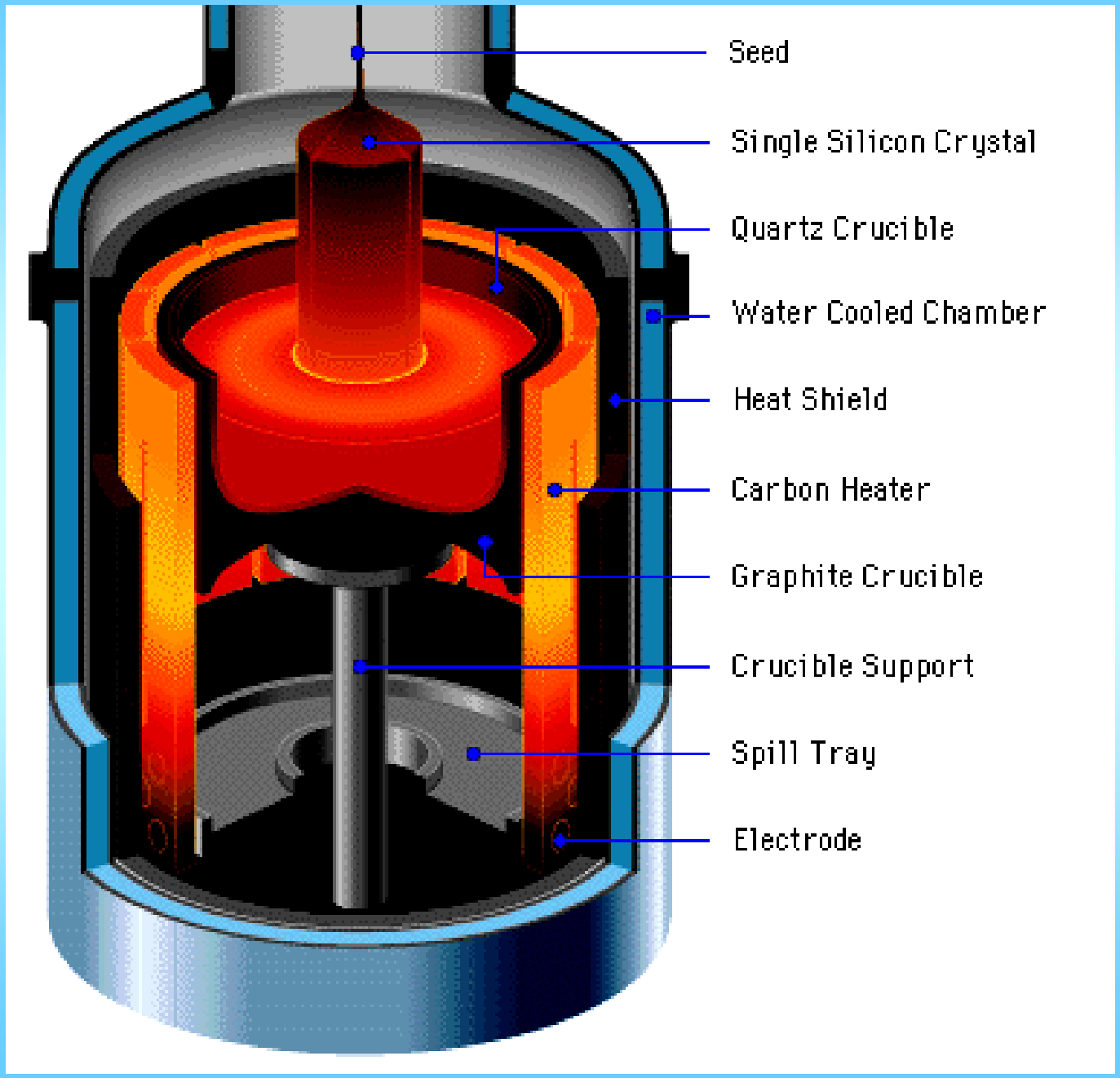
CCCS

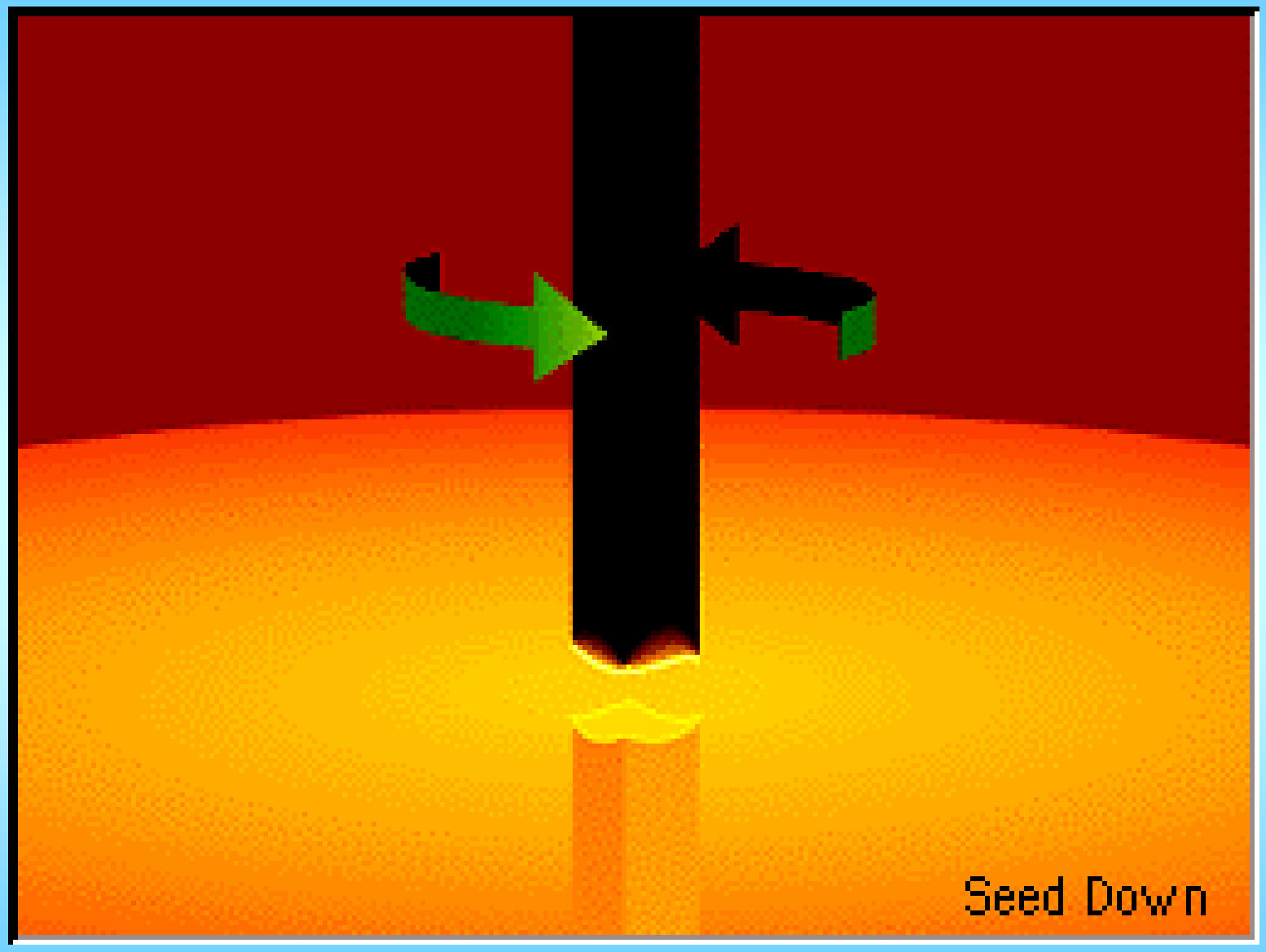

I_{dm}
i_d
I_D
i_D
t

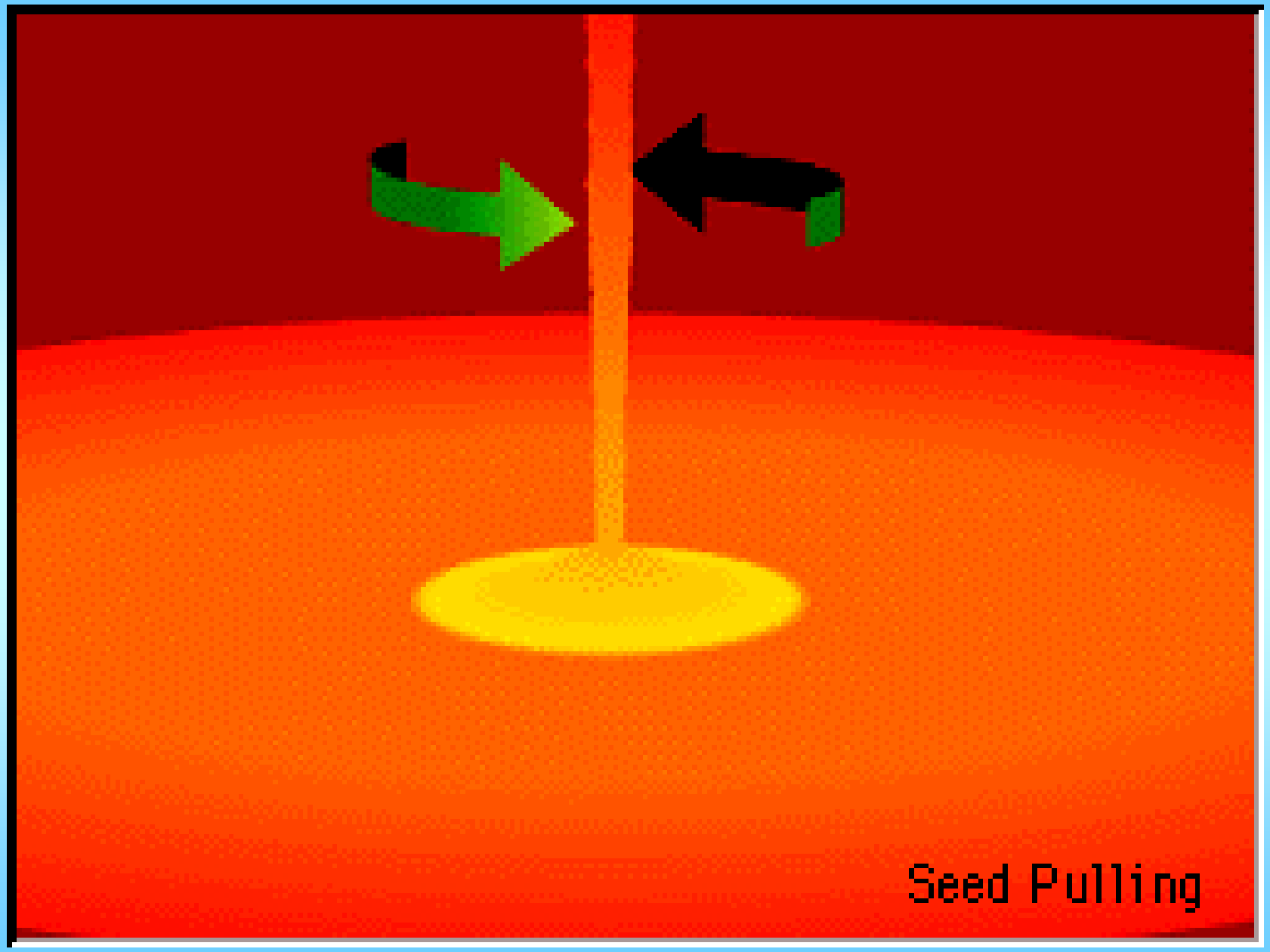
Polycrystalline

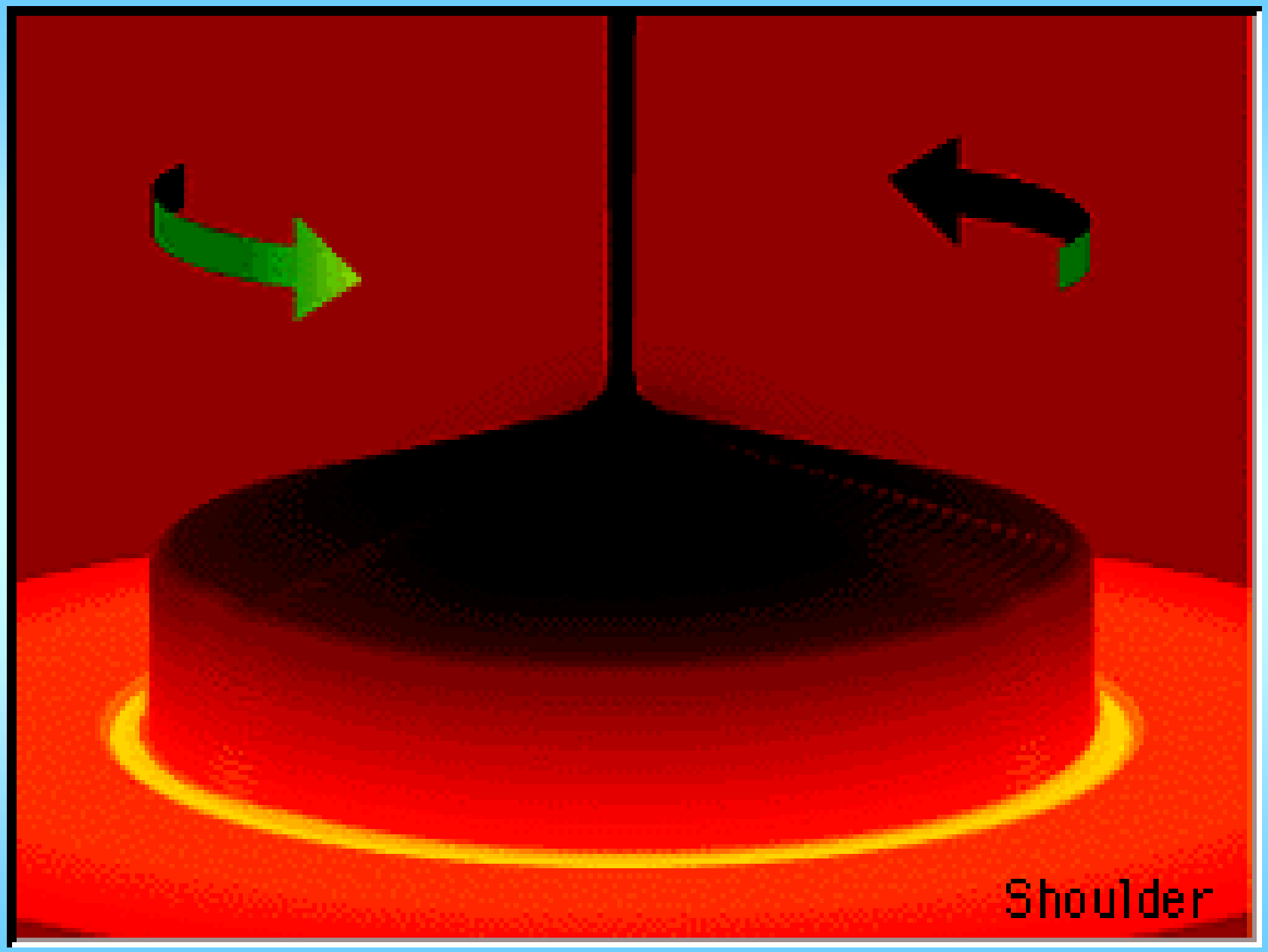
Furnaces

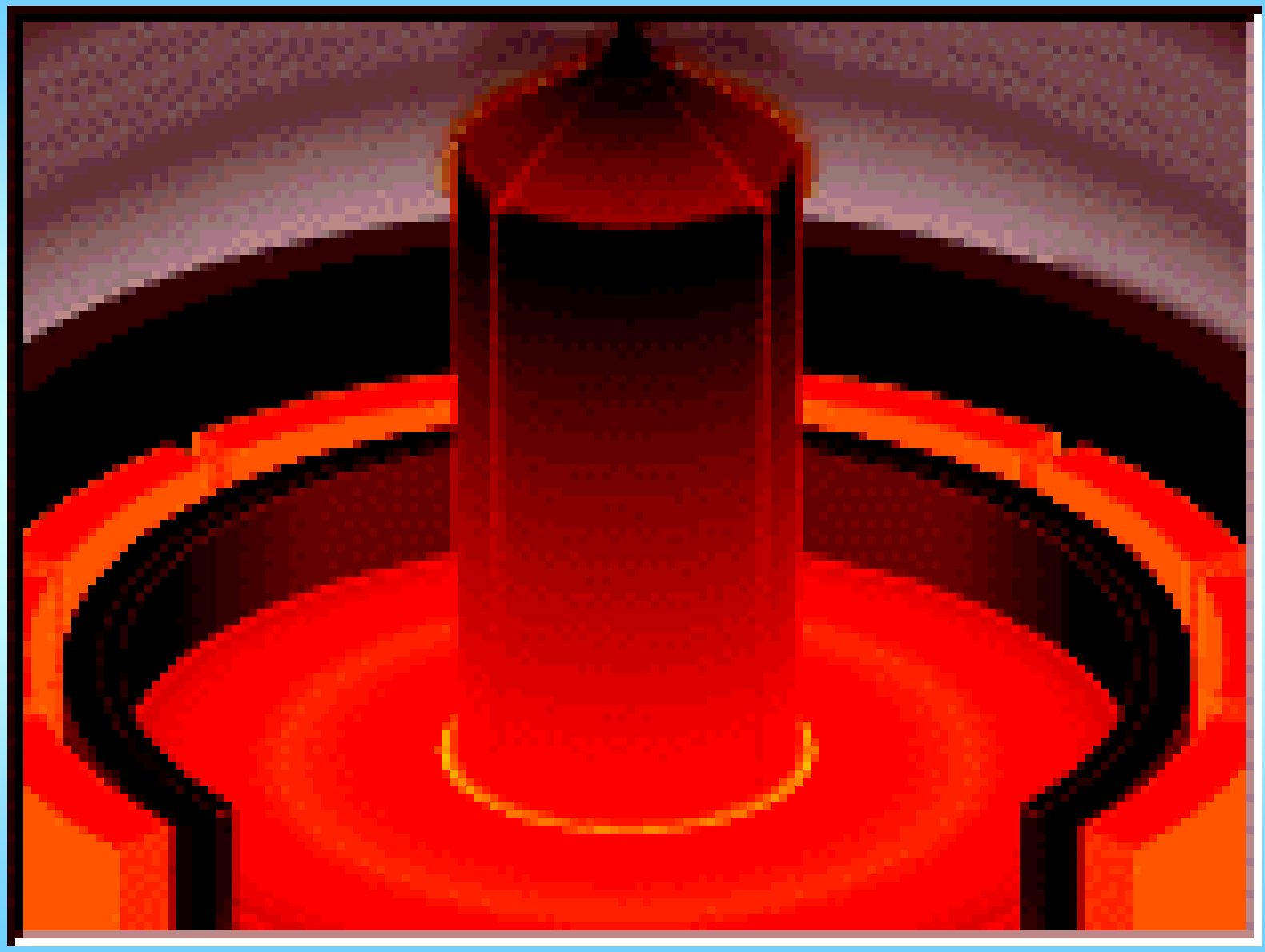


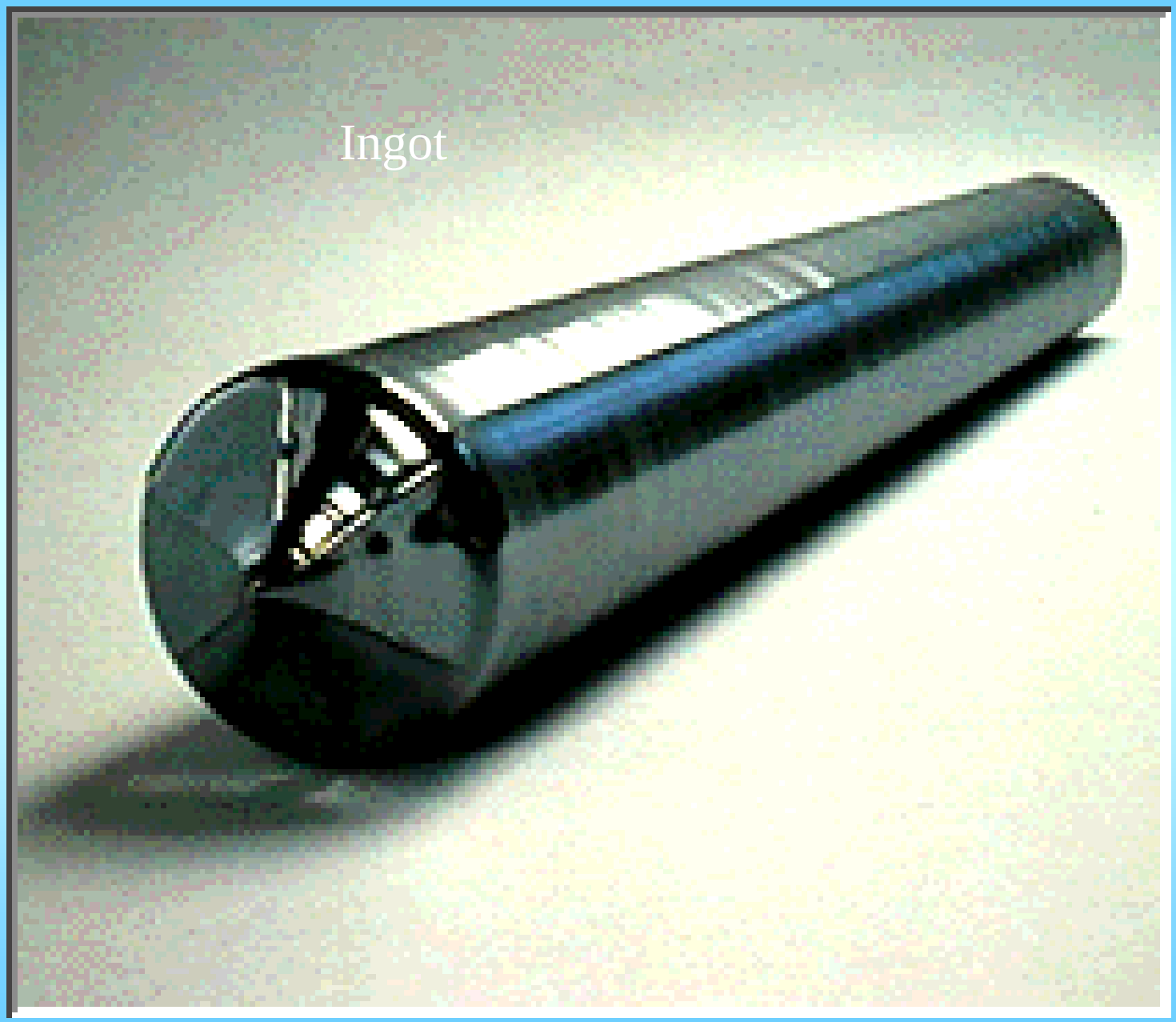

Seed
Single Silicon Crystal
Quartz Crucible
Water Cooled Chamber
Heat Shield
Carbon Heater
Graphite Crucible
Crucible Support
Spill Tray
Electrode

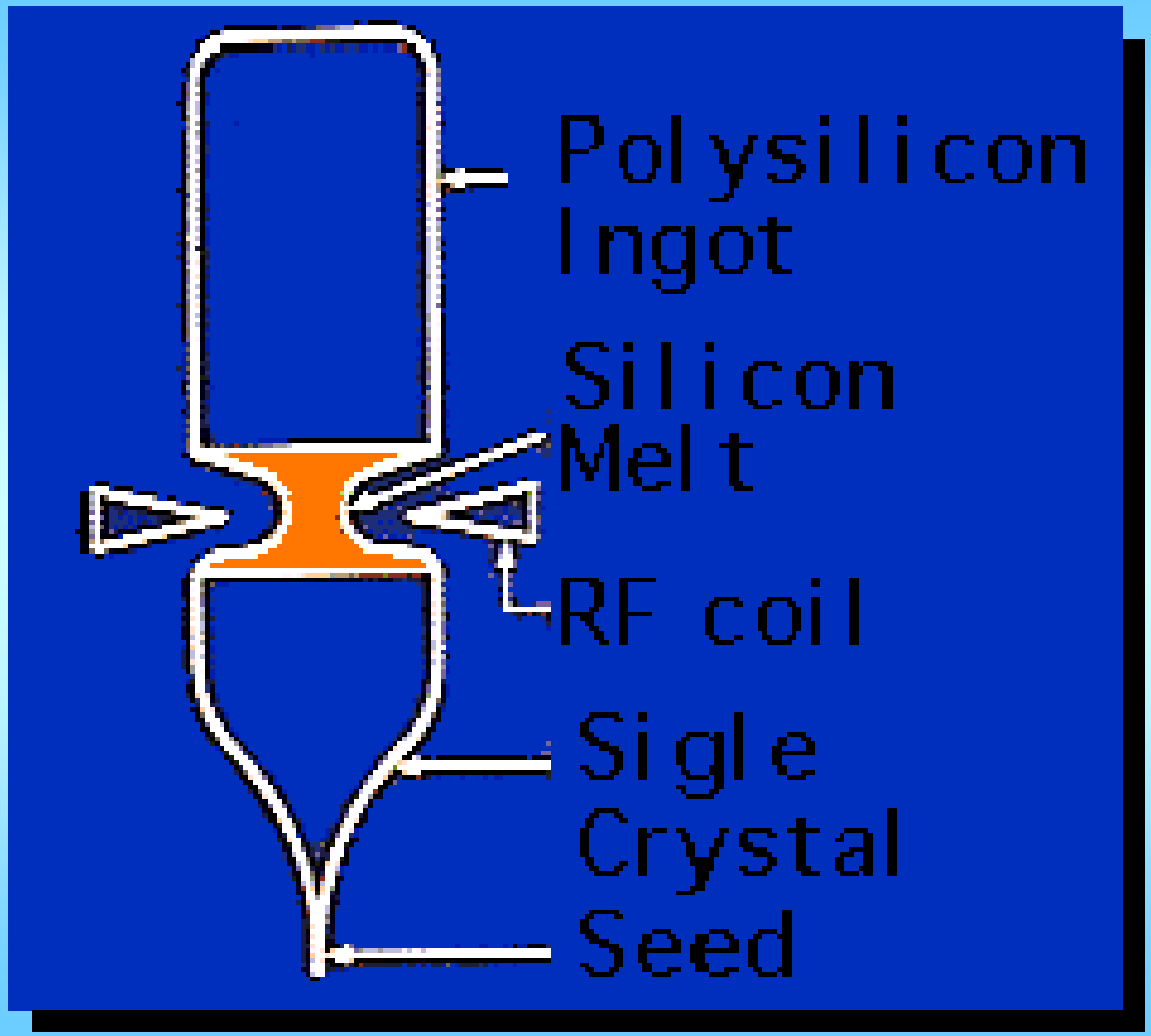

Seed Down


Seed Pulling

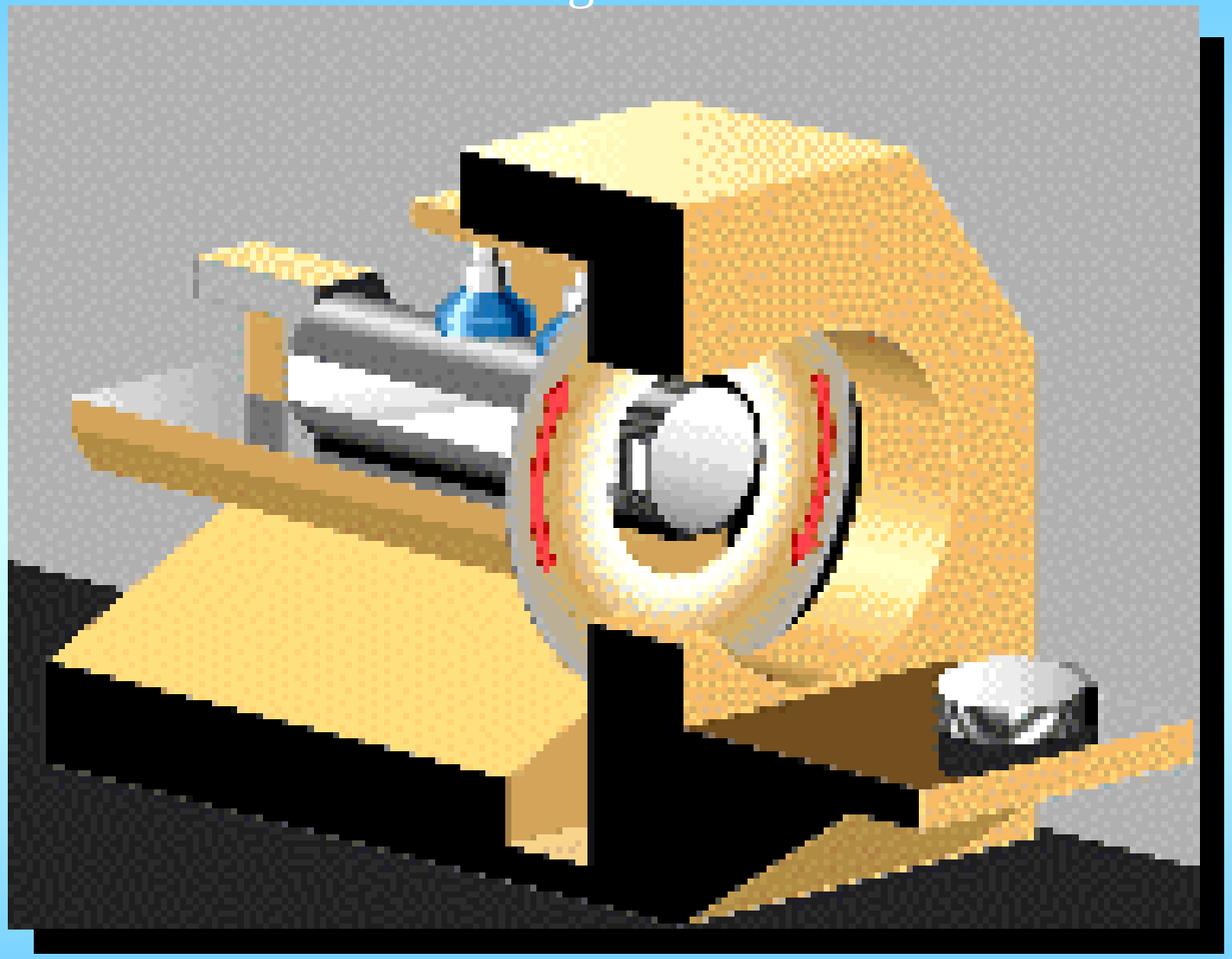

Shoulder

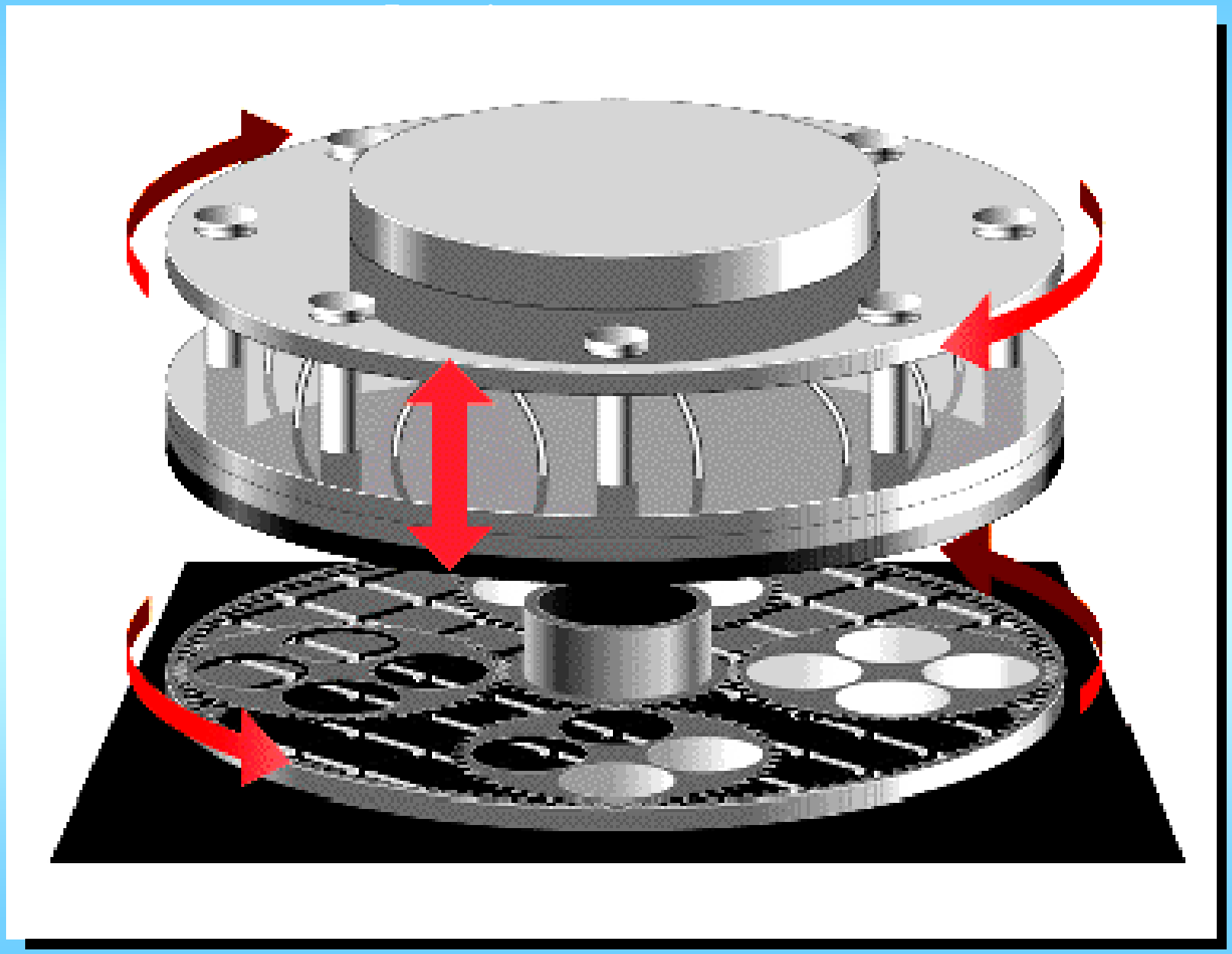



Ingot

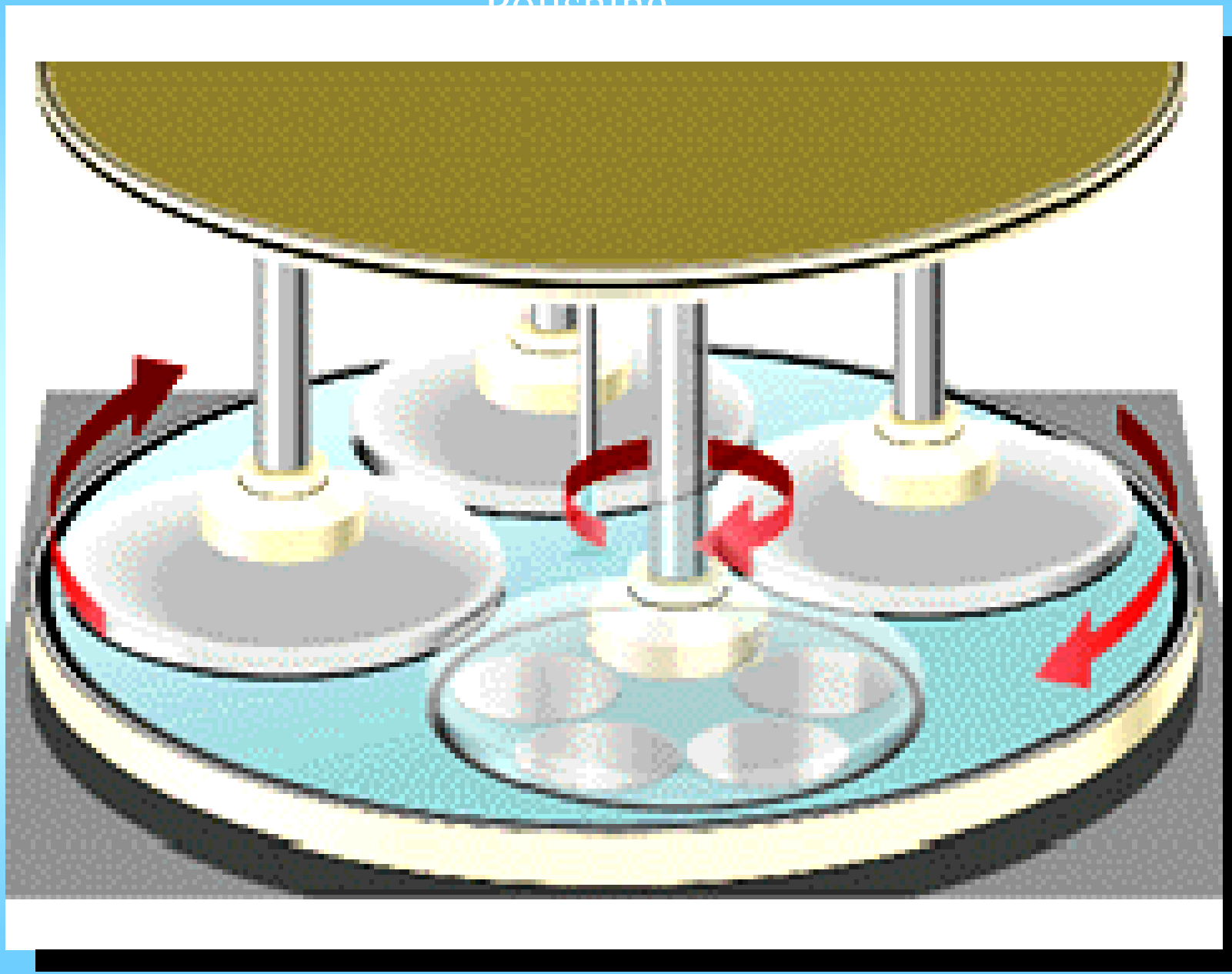

Polysilicon
Ingot
Silicon
Melt
RF coil
Sigle
Crystal
Seed

Slicing

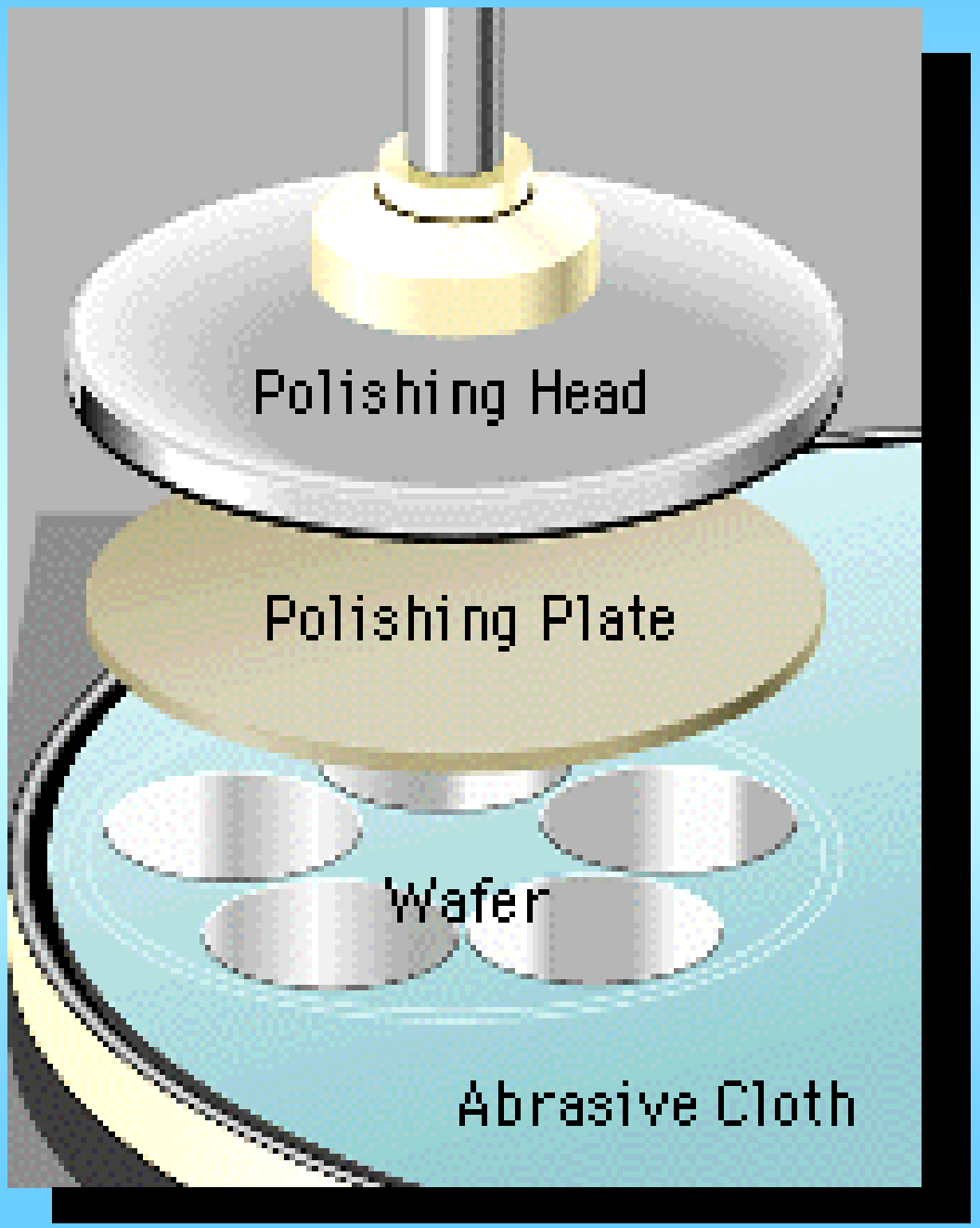


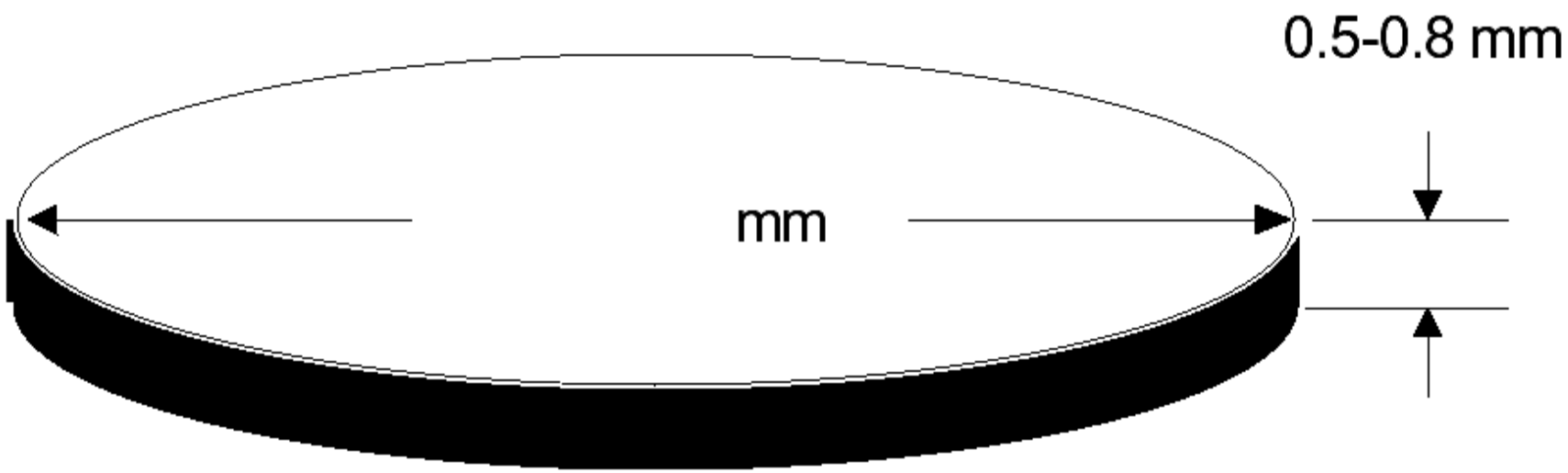


Polishing



Closer View Of Polishing





n-type: 3-5 Ω-cm

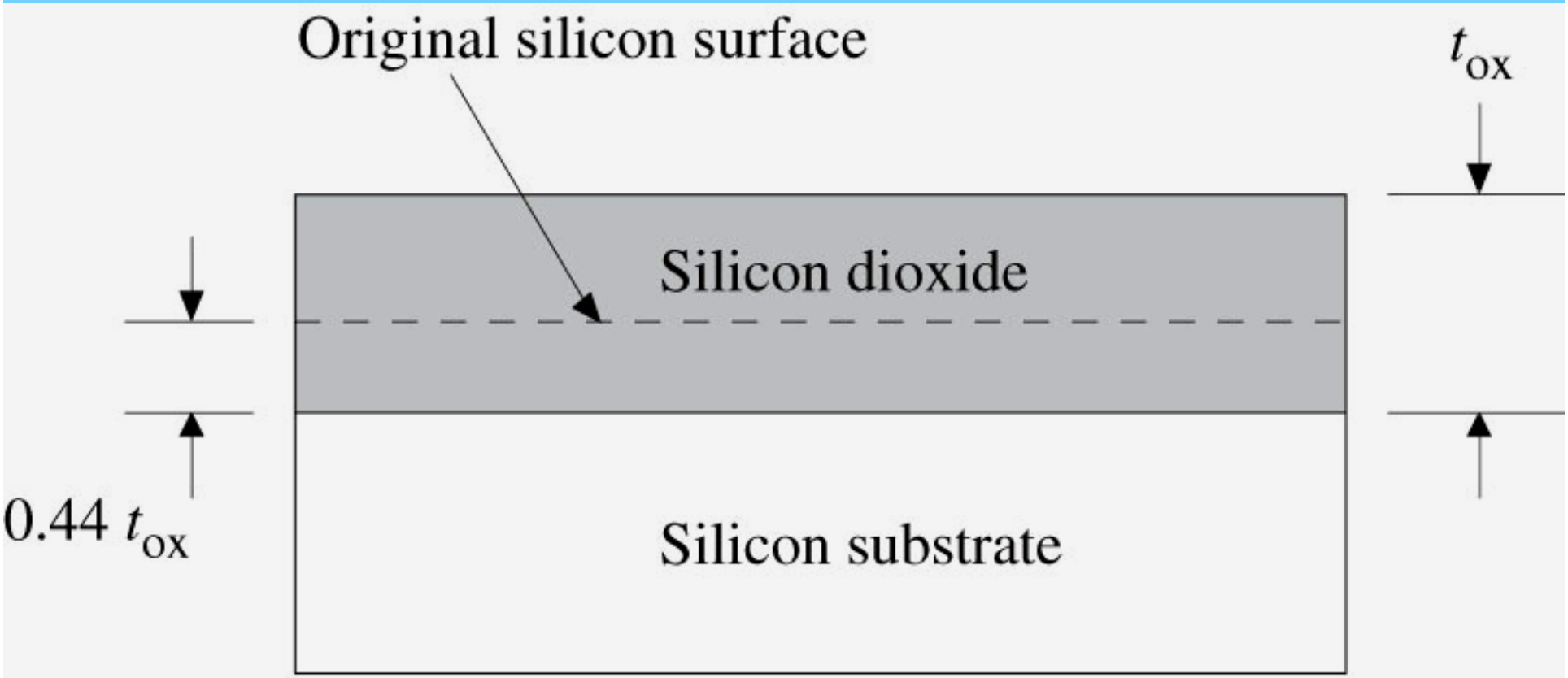
p-type: 14-16 Ω-cm

BASIC FABRTICATION PROCESSES

- Oxide growth
- Thermal diffusion
- Ion implantation
- Deposition
- Etching
- Photolithography

Oxidation

- **The process of growing a layer of silicon dioxide (SiO2)on the surface of a silicon wafer.**
- **Uses:**
  - ✓ **Provide isolation between two layers**
  - ✓ **Protect underlying material from contamination**
  - ✓ **Very thin oxides (100 to 1000 Å) are grown using dry-oxidation techniques.**
  - ✓ **Thicker oxides (>1000 Å) are grown using wet oxidation techniques.**

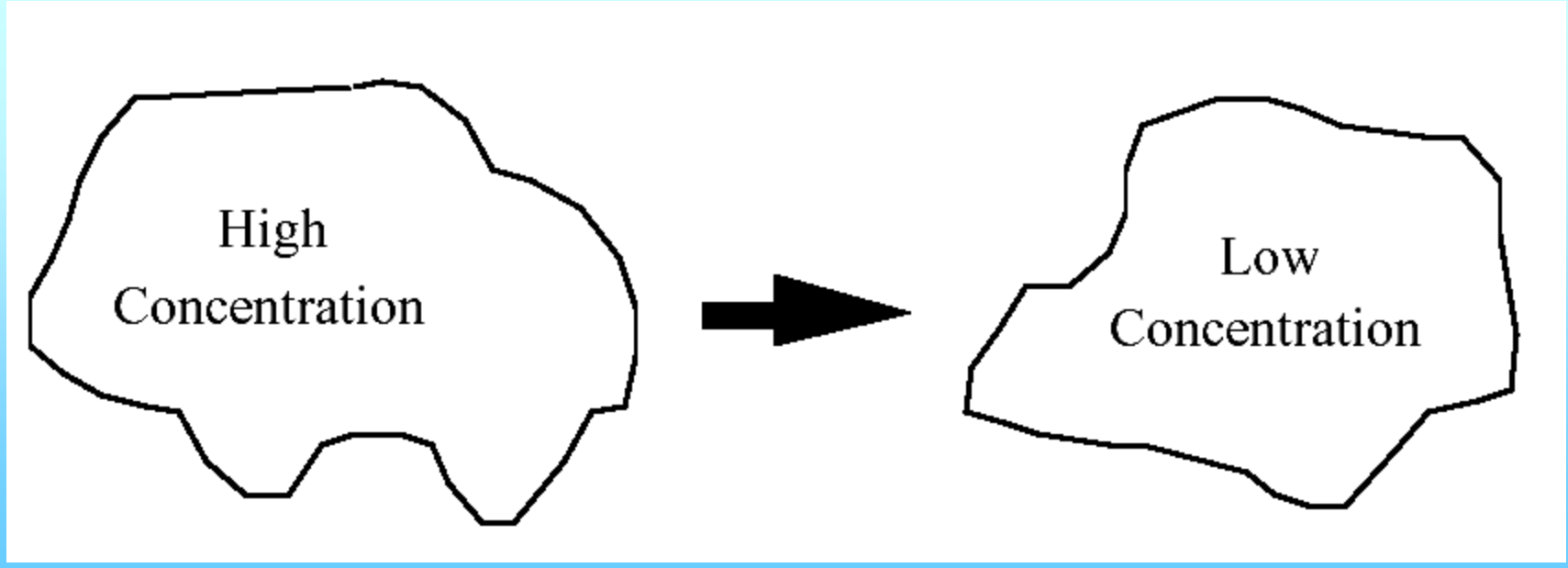


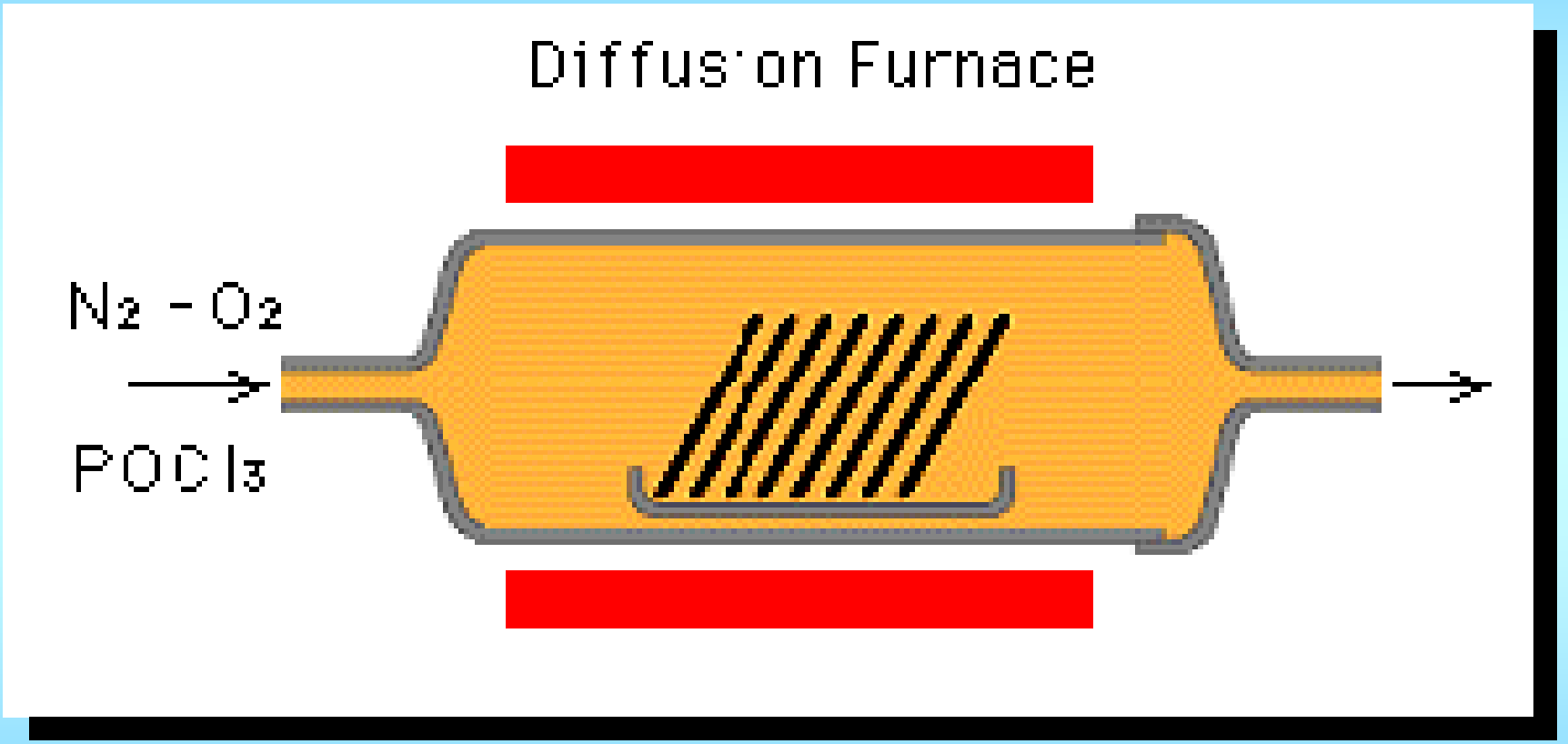
(Thickness of SiO_2 grossly exaggerated.)

Diffusion

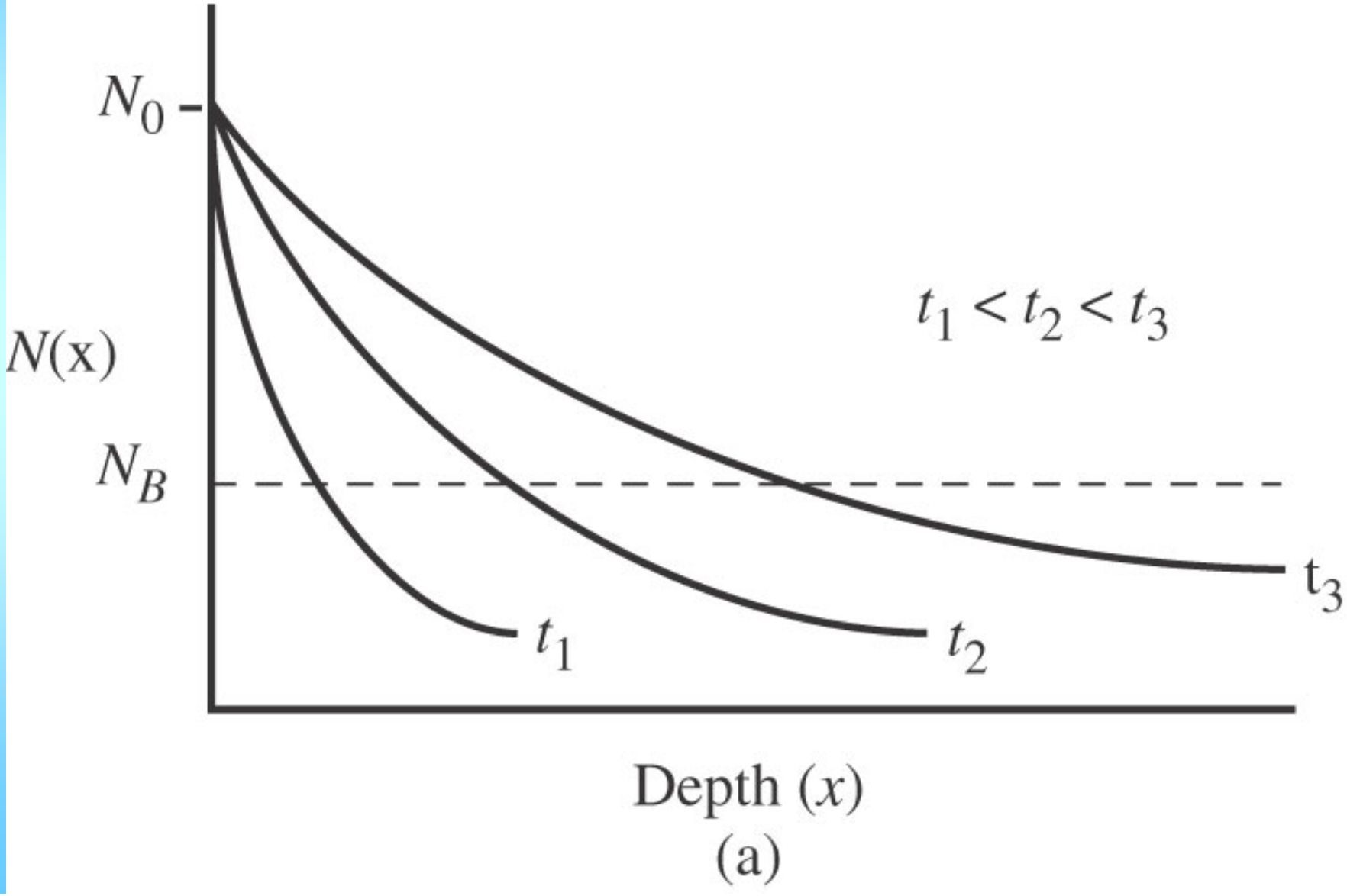
Movement of impurity atoms at the surface of the silicon into the bulk of the silicon

- **From higher concentration to lower concentration.**
- **Done at high temperatures: 800 to 1400 °C.**

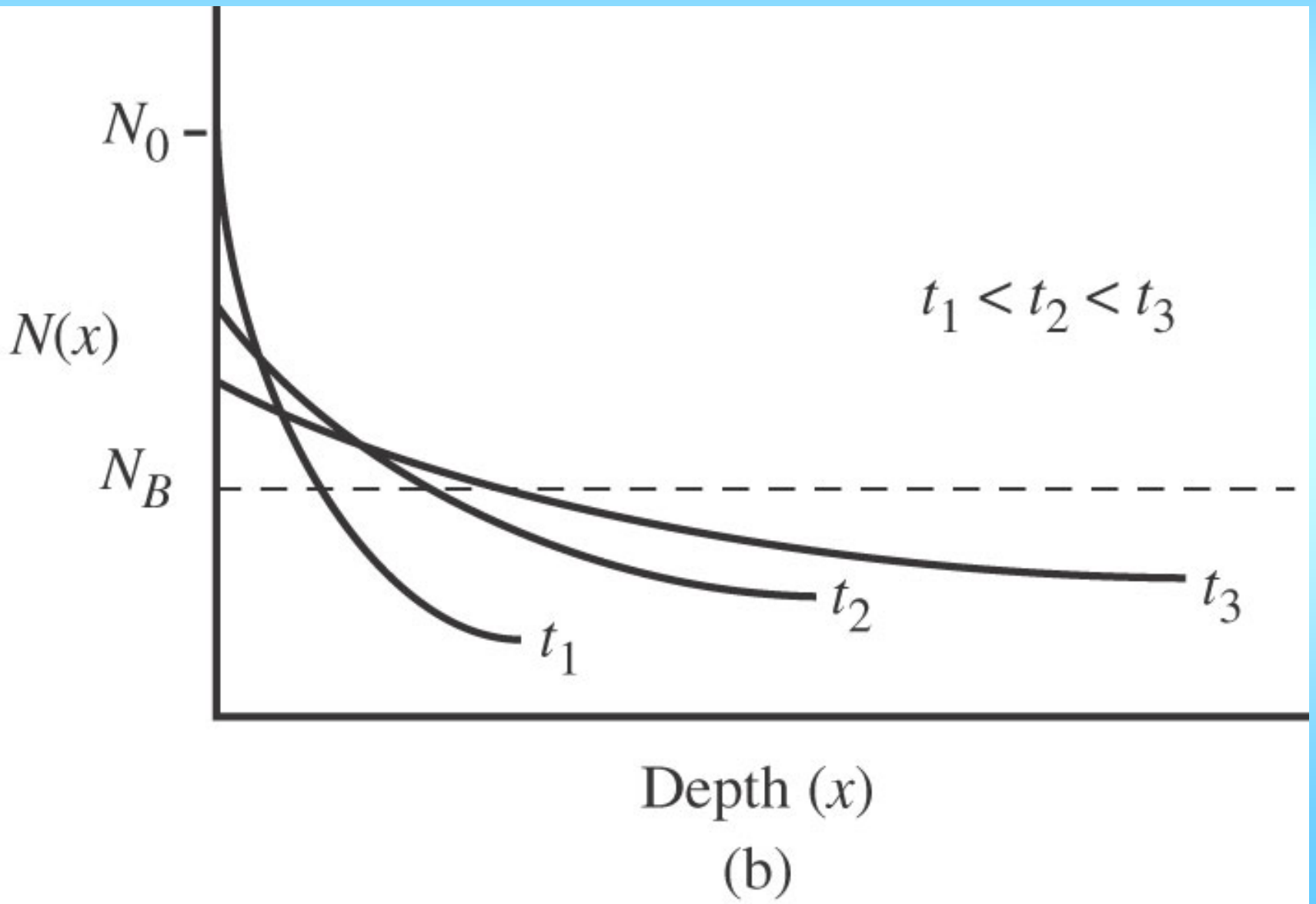



Diffus'on Furnace
N2 - O2
POCl3

Infinite-source diffusion

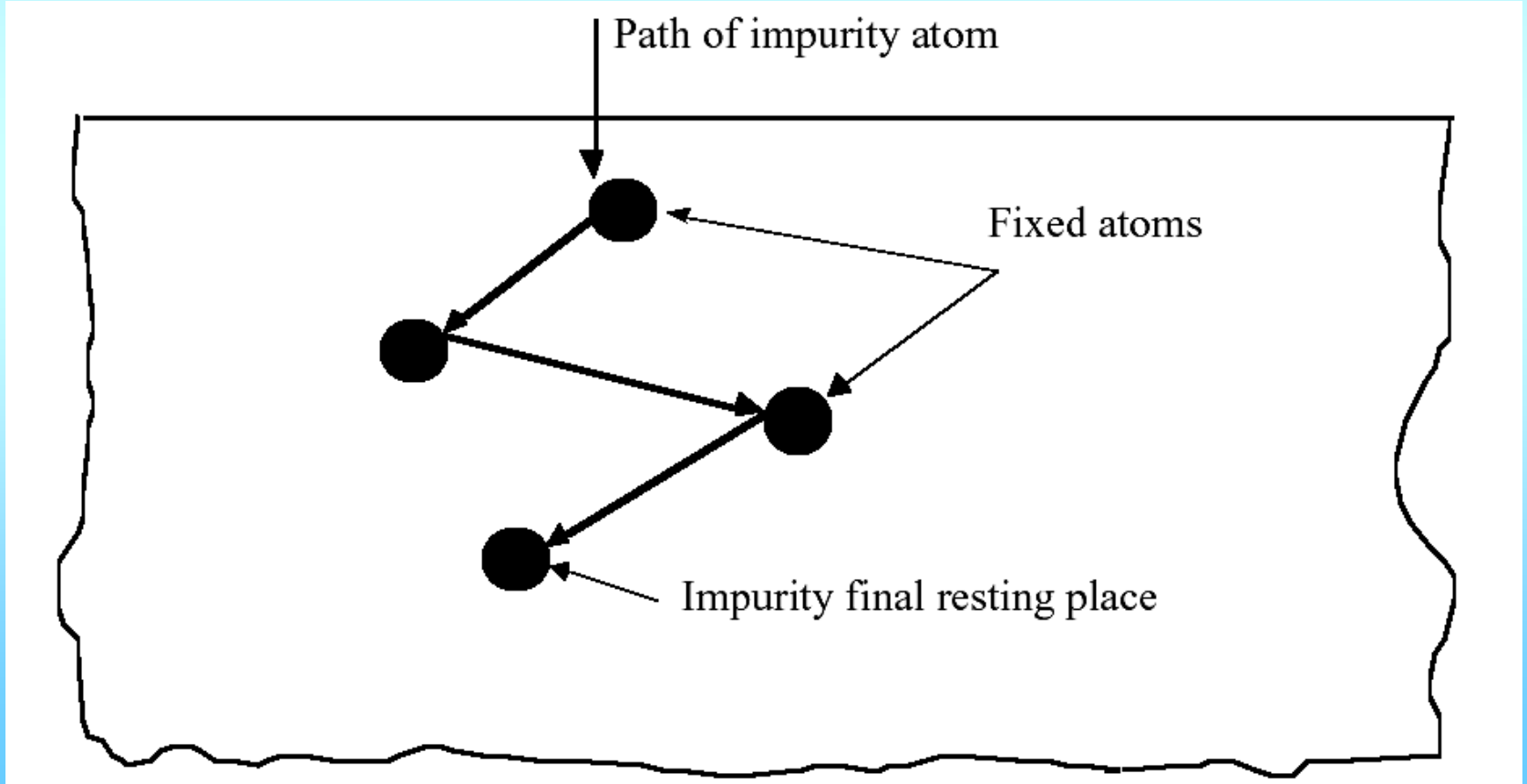


Finite-source diffusion

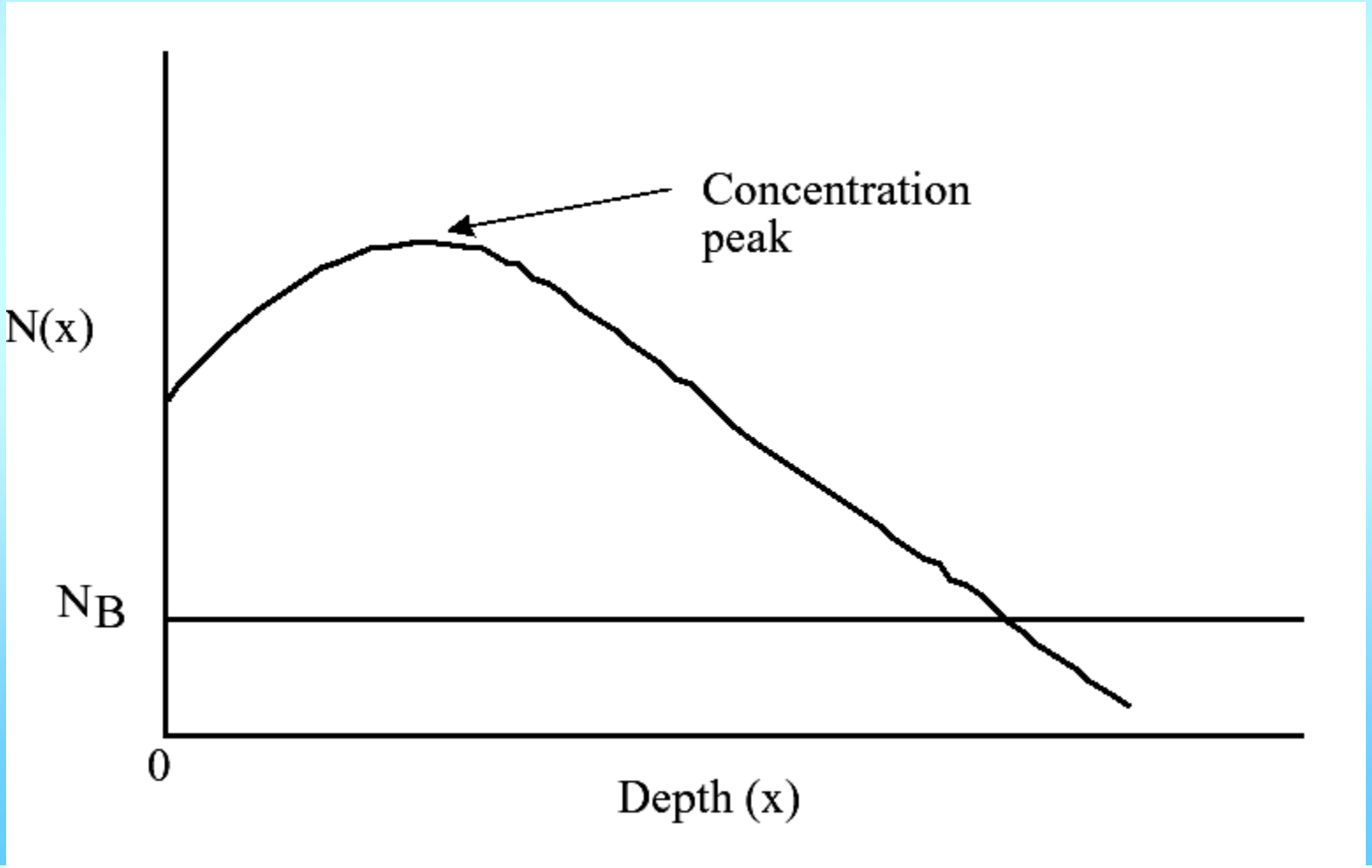


Ion Implantation

The process by which impurity ions are accelerated to a high velocity and physically lodged into the target.



- **Require anneal to repair damage**
- **Can implant through surface layers**
- **Can achieve unique doping profile**



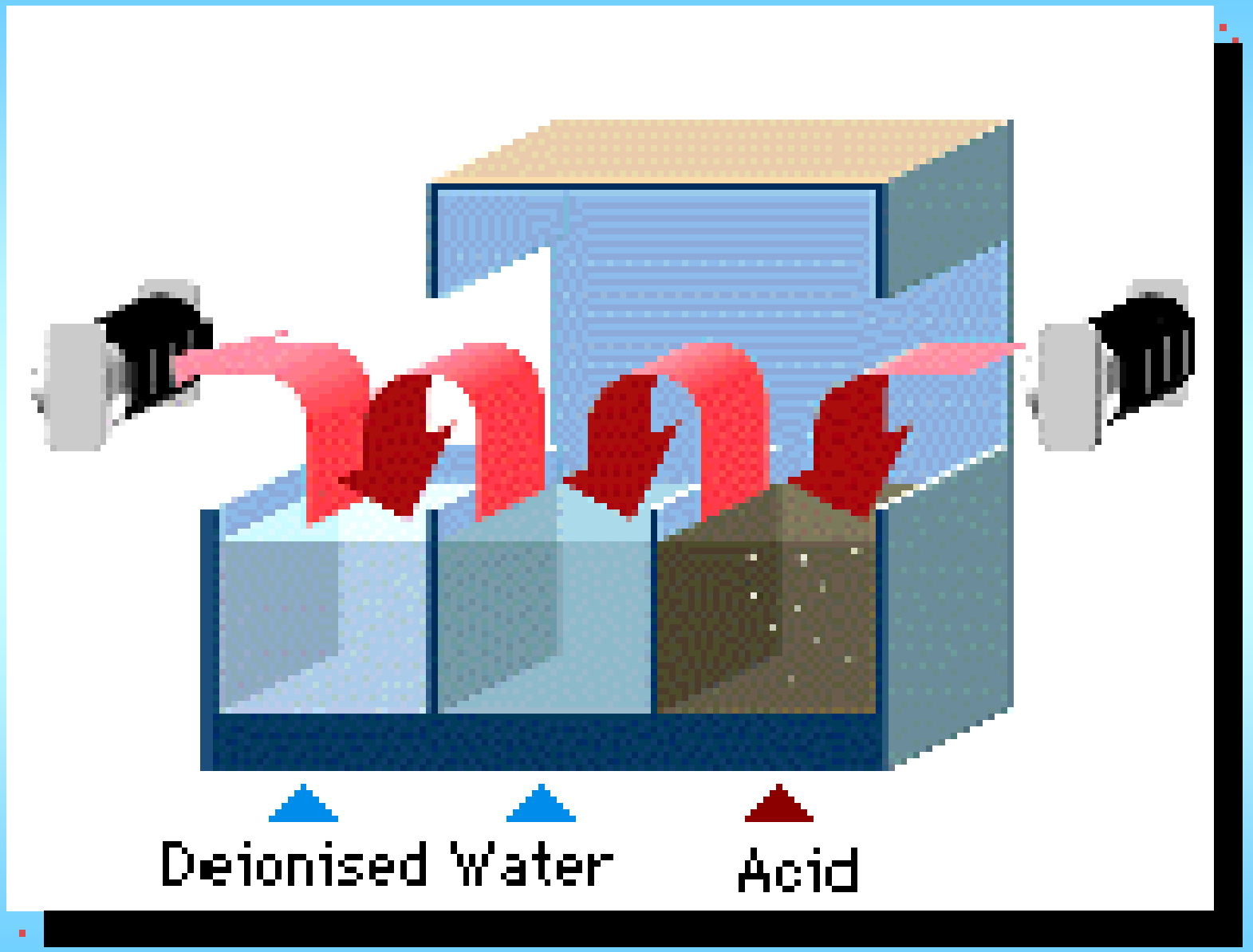
Deposition

- Chemical-vapor deposition (CVD)
- Low-pressure chemical-vapor deposition
- Plasma-assisted chemical-vapor deposition
- Sputter deposition

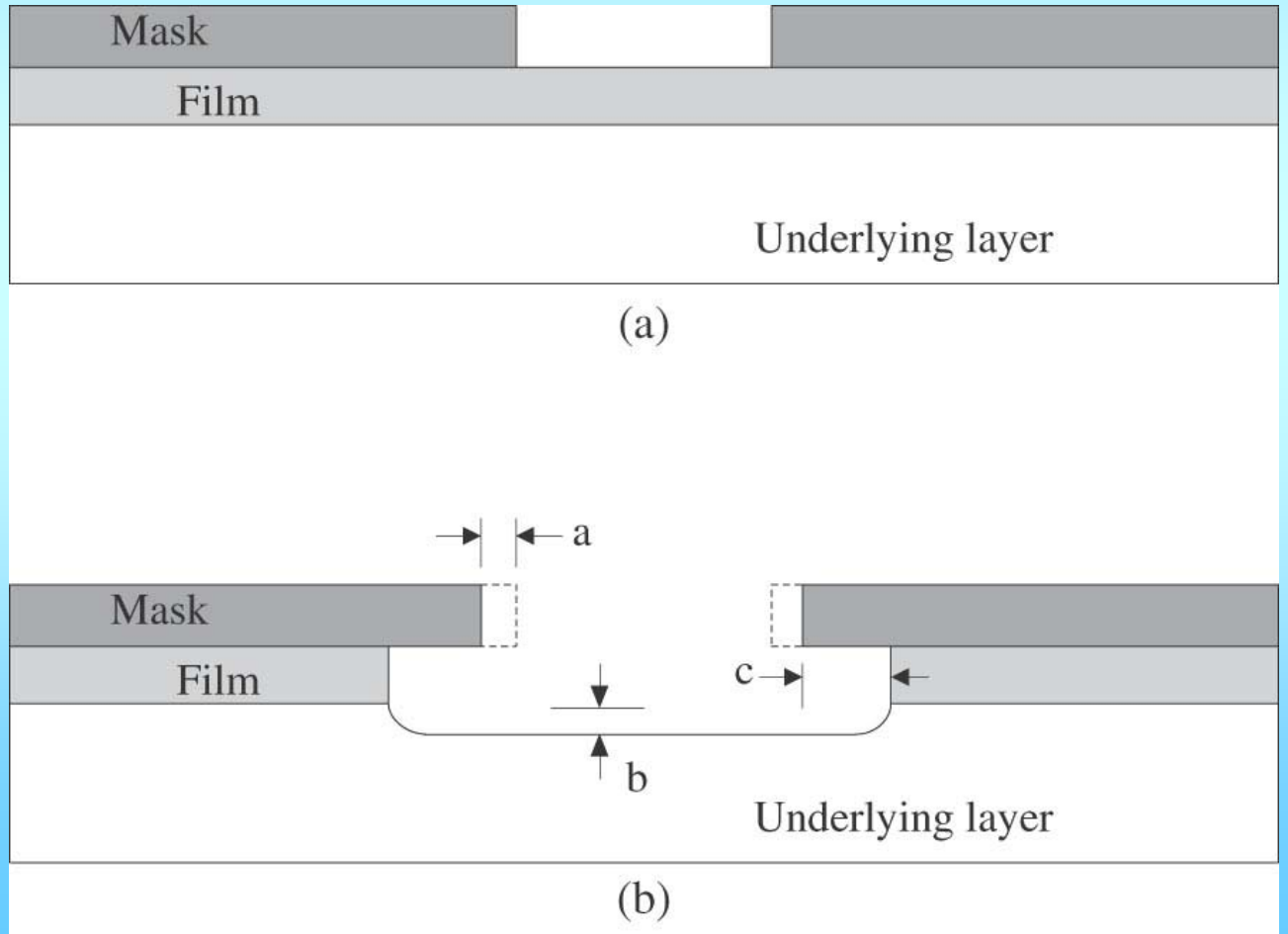
- Materials deposited
  - Silicon nitride (Si_3N_4)
  - Silicon dioxide (SiO_2)
  - Aluminum
  - Polysilicon

Etching

- To selectively remove a layer of material
- But may remove portions or all of
  - The desired material
  - The underlying layer
  - The masking layer
- Two basic types of etches:
  - Wet etch, uses chemicals
  - Dry etch, uses chemically active ionized gasses.


Deionised Water
Acid

- **Selectivity:** $S = \dfrac{\text{Desired layer etch rate}}{\text{Undesired layer etch rate}}$
- **Anisotropy** $A = 1 - \dfrac{\text{lateral etch rate}}{\text{vertical etch rate}}$



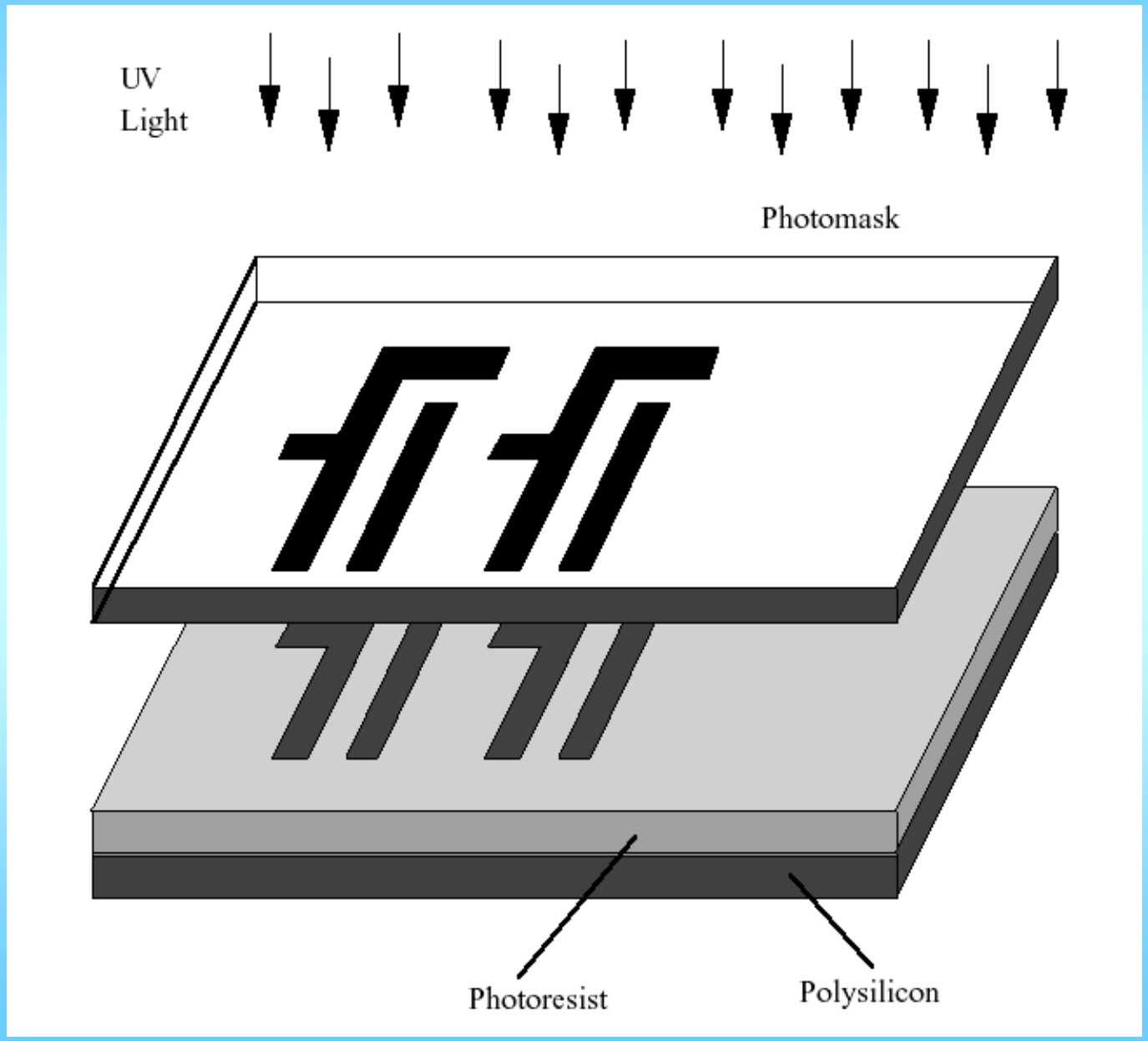
Photolithography

- **Components**
  - **Photoresist material**
  - **Photomask**
  - **Material to be patterned (e.g., SiO2)**
- **Positive photoresist-**
  - **Areas exposed to UV light are soluble in the developer**
- **Negative photoresist-**
  - **Areas not exposed to UV light are soluble in the developer**

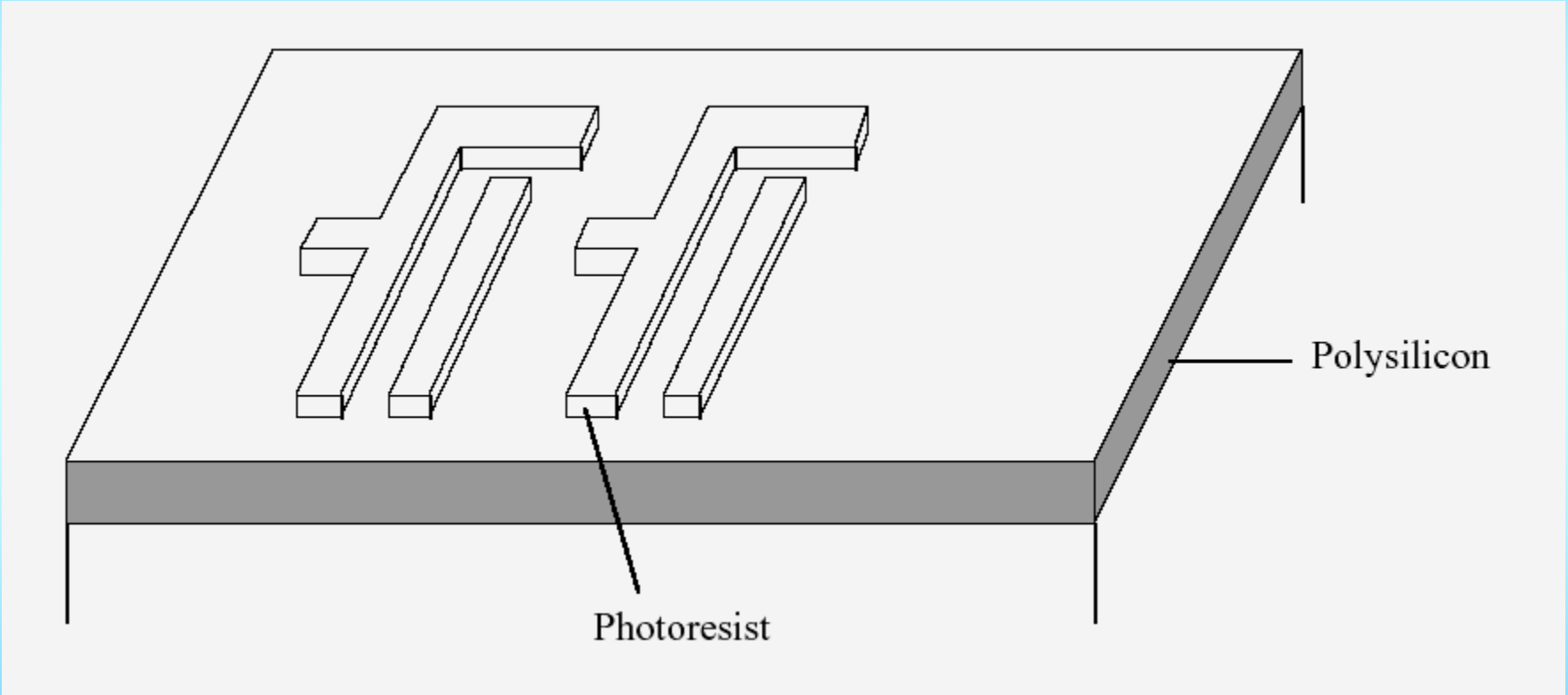
Steps:

1. Apply photoresist
2. Soft bake
3. Expose the photoresist to UV light through photomask
4. Develop (remove unwanted photoresist)
5. Hard bake
6. Etch the exposed layer
7. Remove photoresist

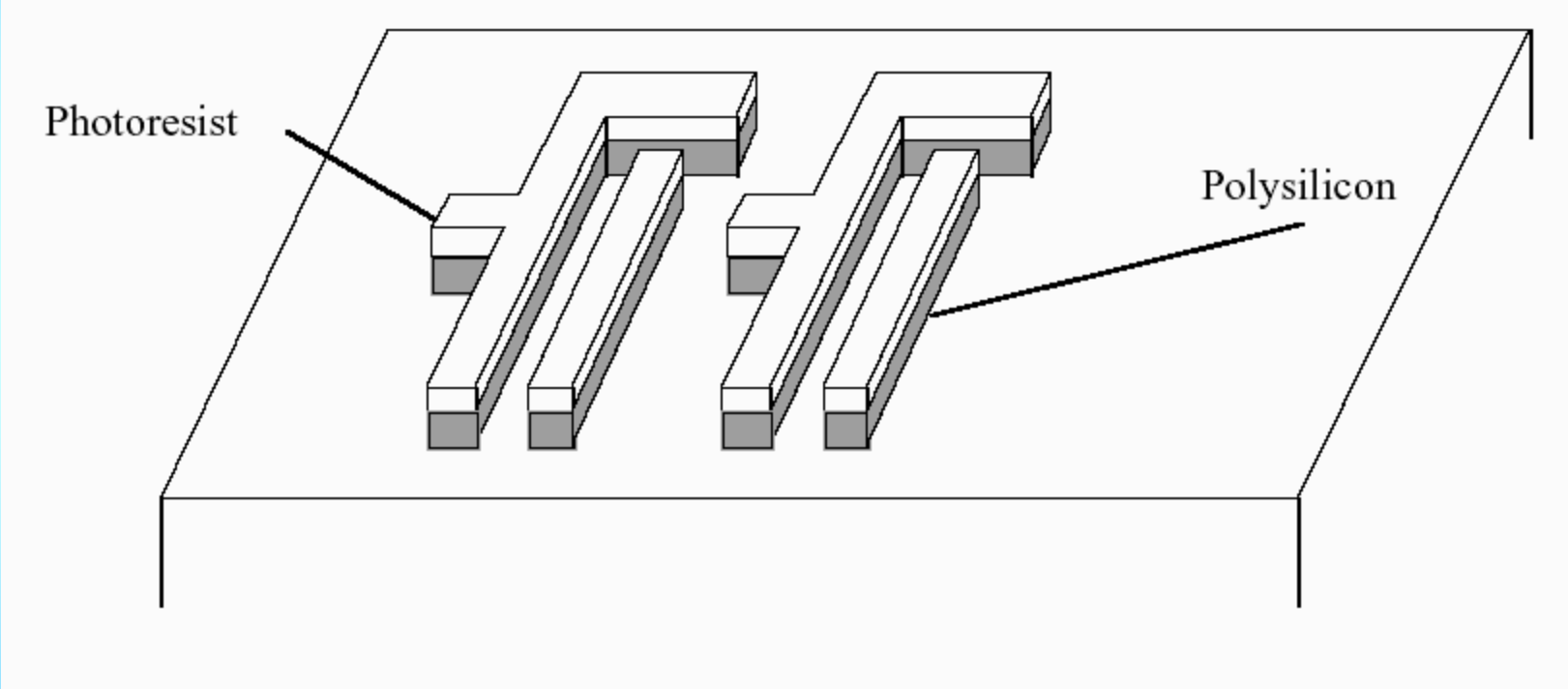
Expose:



After Developing



After Etching



After Removing Photoresist