A Quad CMOS Single-Supply Op Amp with Rail-to-Rail Output Swing

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Abstract—**The realization of a commercially viable, general-purpose quad CMOS amplifier will be presented along with discussions of the trade-offs involved in such a design. The amplifier features an output swing that extends to either supply rail. Together with an input common-mode range that includes ground, the device is especially well suited for single-supply operation and is fully specified for operation from 5 to 15 V over a temperature range of −55 to +125°C. Unlike earlier designs that sacrificed performance in the areas of input offset voltage, offset voltage drift, input noise voltage, voltage gain, and load driving capability, this implementation offers performance that equals or exceeds that of popular general-purpose quads of bipolar or BI-FET[1] construction. On a 5-V supply the typical V_{os} is 1 mV, V_{os} drift is 1.3 μV/°C, 1-kHz noise is 36 nV/√Hz, and gain is one million into a 600-Ω load. This device achieves its performance through both circuit design and layout techniques as opposed to special analog CMOS processing, thus lending itself to use on system chips built with the latest digital CMOS technology.**

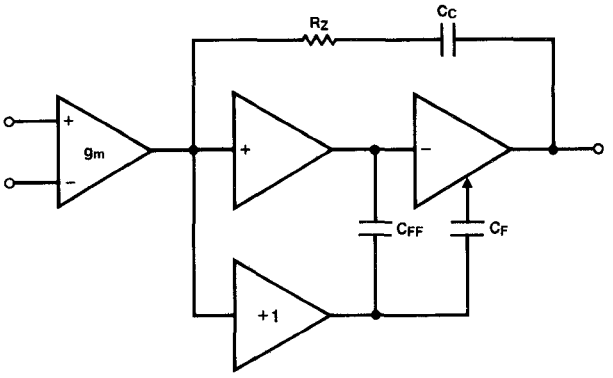

Fig. 1. Circuit topology of the amplifier.

I. Introduction

ALTHOUGH special-purpose CMOS amplifiers are an accepted part of mixed analog/digital chips where their ability to be integrated outweighs their existing weaknesses, penetration into stand-alone applications has been limited to niches such as low voltage, low power, and chopper stabilization. Unfortunately, shortcomings in the input stage relating to input offset voltage, drift and noise, shortcomings in the output stage in driving realistic loads, and latch-up sensitivity have prevented CMOS from making a strong contribution to the mainstream amplifier arena. This paper will describe a new CMOS amplifier design with overall performance on a +5-V supply that is equal to or better than most commercially available bipolar, BI-FET, or CMOS quad amplifiers. It is significant that this has been achieved on a conventional 4-μm, double-polysilicon, P-well process optimized for digital chips. This ability to share a common process with advanced digital CMOS circuits has important ramifications in realizing the large mixed analog/digital chips of the future that are the dream of the system designer.

II. Amplifier Topology

The amplifier topology chosen (Fig. 1) departs somewhat from the convention for general-purpose operational amplifiers in that the traditional unity-gain buffer is absent and the output is taken instead directly from the output of the integrator. Designing the buffer would not have been straightforward due to requirements for a stable stage with a gain of between one and two and an output that swings rail to rail. This remains a viable approach. However, eliminating the buffer has the advantage of simplicity and potential power savings, but places greater demands upon the integrator to deliver power, high gain, and rail-to-rail swing, to withstand shorts to either rail, and to remain stable in the presence of a wide range of loads. As a result of these demands, the integrator is a compound affair with an embedded gain stage that is doubly fed forward (via C_F and C_{FF}) by a dedicated unity-gain compensation driver. In addition, the output portion of the integrator is a robust push–pull configuration. While sinking current the whole amplifier path consists of three gain stages with one stage fed forward, whereas while sourcing the path contains four gain stages with two fed forward.

III. The Input Stage

The input stage (Fig. 2) is a conventional configuration that has been very carefully optimized for best performance. The physical layout of this circuit block has as much to do with good performance as does the actual circuit design. The most critical elements are the input devices $M1$ and $M2$, and considerable thought went into their choice, geometry, and placement on the die.

Noise measurements on test structures revealed that the Native p-channels ($V_T = -1.5$ V) were the quietest of the four MOSFET types available on the process. The second quietest device is the Native n-channel ($V_T = 0.7$ V) followed in order by the implant adjusted p-channel ($V_T =$

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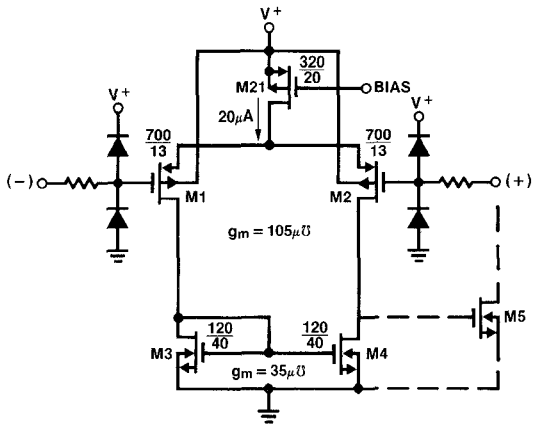


Fig. 2. Input stage with common-mode range that includes ground.

-0.7 V) and the implant adjusted n-channel ($V_T = 1.0$ V). This is in general agreement with the findings of other designers and researchers. It appears that the hole-based devices are indeed quieter than the electron-based devices, but that the overriding factor is whether or not the device receives a threshold adjusting implant.

In order to insure that the input devices dominate the performance of the input stage, they were designed to have a transconductance (105 μmho) that was three times that of the mirror transistors, Native n-channel devices $M3$ and $M4$. That ratio, coupled with the fact that the n-channels have a higher transconductance for equivalent geometry relative to the p-channels, results in the latter having a much higher W/L (700/13) than the mirror devices ($W/L = 120/40$).

The input devices constitute an unusual structure (Fig. 3) that is assembled from a regular array of 16 doughnut-shaped gate regions that are patterned out of a large square of p^+ source/drain implant. This background of p^+ represents the common-source connection of the pair and the interior circles represent the interconnected drain regions. The doughnut structure has minimal associated drain capacitance which helps minimize detrimental phase lag through the mirror. The relatively higher source capacitance manifests primarily as asymmetrical slew behavior. Calculation of the effective width of the doughnut channel region is not straightforward. The width of a single transistor cell as determined by the laterally diffused circumference of the drain region is 80 μm, and as determined by the laterally diffused circumference of the source circle it is 152 μm. Determination of the net effective width of the structure via transconductance measurements put the value at 87 μm, indicating that the effective width of circumference is located much closer to the drain than to the source. This appears logical from the standpoint that the channel near the drain has the highest current density and thus can be expected to dominate the transconductance. The drawn gate area is 1511 μm^2 per doughnut and eight times that or 12088 μm^2 for $M1$ or $M2$.

The mirror devices $M3$ and $M4$ consist of a cross-coupled quad of conventional rectangular construction. Their relatively long channels maximize first-stage gain, minimize output impedance related mismatch error, and set the desired low transconductance of the mirror. The drawn gate area is 4800 μm^2 per transistor.

In order to achieve the best possible V_{os} performance, the use of common-centroid cross-coupling techniques is mandatory for effective rejection of processing gradients. The layout should strive to achieve the highest possible number of cross-coupled elements per unit area consistent with good definition of features and practical interconnect. Nowhere was this carried out to a higher degree than in $M1$ and $M2$ where the 16 doughnuts are packed into a common square of p^+ and interconnected in a checkerboard pattern. The space between the individual doughnuts was efficiently used to connect the poly gates to the second poly which in turn provided the cross-coupled interconnect. Metal was used to cross couple the drains. The web of source material that threads through the structure results in higher source resistance for the interior devices than the outer devices. This means that the connection to the common-source region cannot be freely chosen if systematic offsets are to be avoided. A complex matrix of some 50 resistive elements was created and computer analyzed to study the p^+ pick-up problem. The two-sided pick-up shown in Fig. 3 is one of several schemes that was found to be successful in the study.

Package-induced stress during die attach and molding is a known enemy of the precision match of surface devices like JFET's, MOSFET's, resistors, and to a lesser degree, BJT's. For this reason, the entire input stage is arranged to lie symmetrically about the die centerlines of minimum stress (Fig. 4). The output stage power devices are located directly above the input devices and are also on the centerline for isothermal reasons. The rejection of thermal waves from the other cells on the chip is left to the high degree of cross coupling.

From a circuit point of view the input stage is also well balanced. The second-stage transistor $M5$ is biased such that its V_{GS} is equal to that of $M3$ which eliminates the potential V_{os} error term that would have occurred if $M1$ and $M2$ had been allowed to have unequal drain-to-source voltages. When the needs of small-signal bandwidth, slew, common-mode range, voltage gain, and noise are combined, the input devices end up being biased into their quasi-subthreshold region which lies somewhere between square-law and exponential behavior. This is not at all a poor region in which to be operating. The V_{GS} match is better than the square-law region and the current density is not as low as in the subthreshold region where high-temperature operation is risked to leakage and ac performance suffers from an abundance of capacitance and a lack of current. At first it may appear that second-stage transistor $Q23$ (see Fig. 7) will load the input stage with base current, thus introducing a systematic offset and a drift component. This does not occur to any significant degree, however, due to the high beta (typically 900) of the substrate n-p-n and the temperature coefficient of its quiescent current. The excellent V_{os} performance

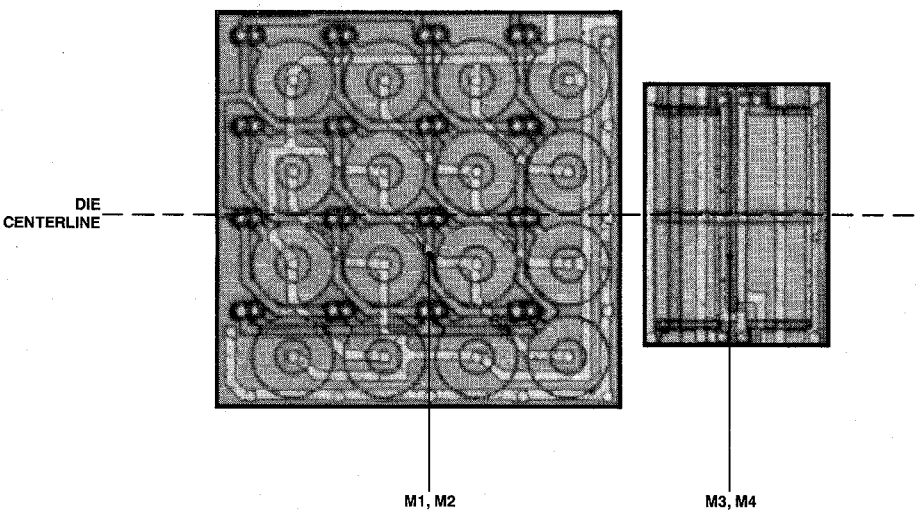


Fig. 3. Geometries of cross-coupled input transistors $M1$ and $M2$ and cross-coupled mirror transistors $M3$ and $M4$. The centerline of minimum package-induced stress passes through the center of these critical devices.

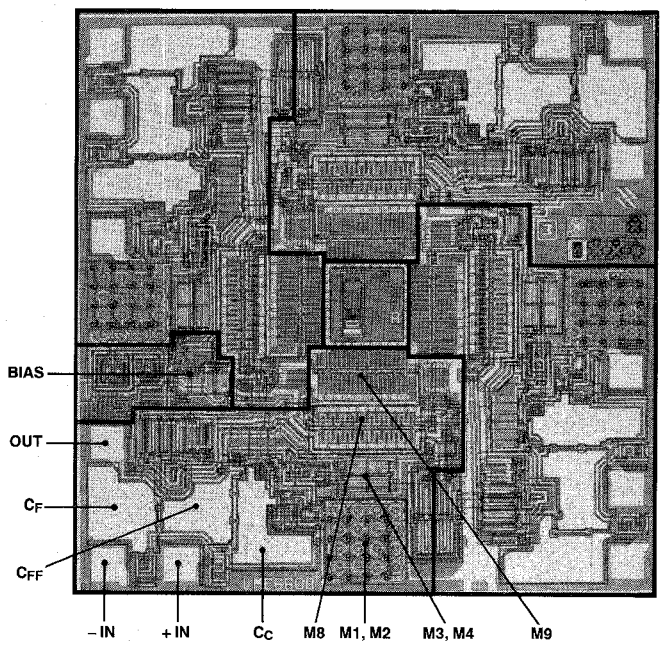
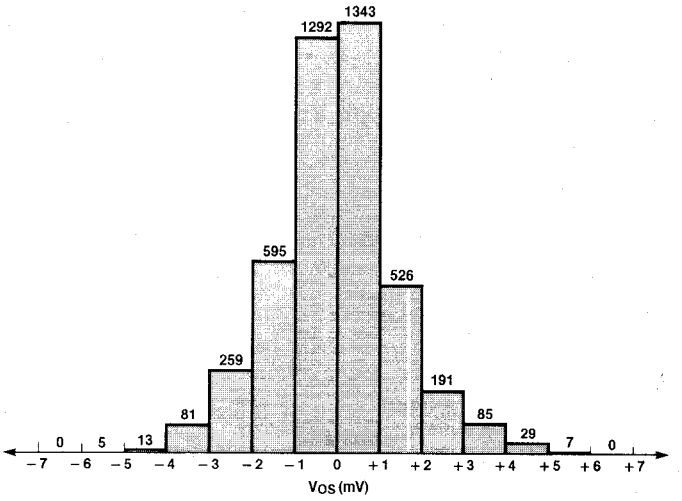
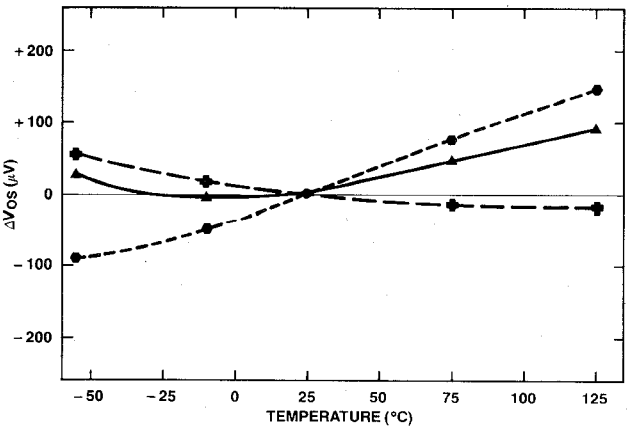


Fig. 4. Photomicrograph of 75×75-mil (3.63-mm^2) die. Each amplifier input stage is located along the die centerline of minimum stress and symmetrically placed behind the thermal sources of the output stage. The capacitors are poly to poly with an overcoat of metal.



(a)

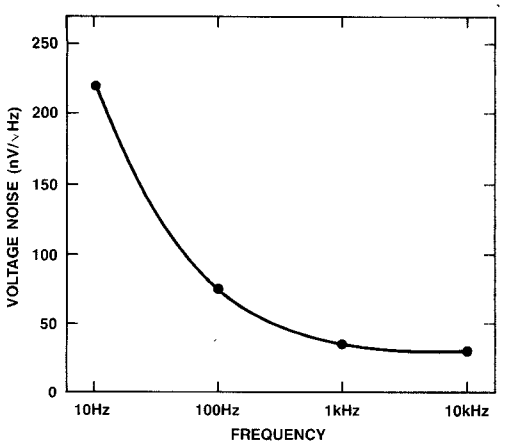


(b)

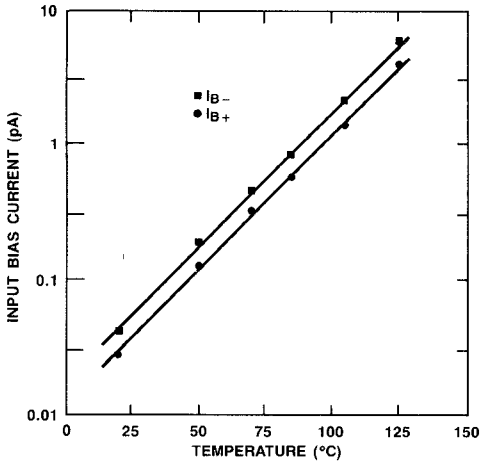
Fig. 5. (a) The distribution of V_{os} on a typical wafer as measured at wafer-sort for all functional op-amp cells on the wafer taken as a group. The mean V_{os} is -0.04 mV and the sigma is 1.37 mV. (b) The V_{os} drift versus temperature for three representative op-amp cells.

(Fig. 5(a)) of the amplifier is better than existing CMOS offerings and compares favorably with the raw offsets of bipolar and BI-FET quads. After die attach and encapsulation in plastic, the offset distribution undergoes minimal degradation. The V_{os} drift performance (Fig. 5(b)) is likewise excellent and again compares very favorably with other general-purpose untrimmed quads. Note the absence of any telltale "hook" in the high-temperature end of the drift curve that would be indicative of an input stage leakage problem.

The voltage gain of the input stage is quite high, typically 54 dB, which easily swamps the noise of the second stage and significantly contributes to the high gain of the



(a)



(b)

Fig. 6. (a) Input-referred voltage noise density versus frequency. (b) Input bias current versus temperature for each input.

overall amplifier. This high gain is achieved because the second-stage loading is very light, the mirror has very high output impedance, and the input devices are operating quasi-subthreshold.

For true single-supply operation the input-stage common-mode range must include ground. Two effects combine to achieve this. One is the higher V_T(1.5 V) of the Native input devices and the other is the unavoidable body effect of those same devices which are built in the substrate. Although the body effect is desirable in that it increases the V_{GS}, the mismatch of the body effects of $M1$ and $M2$ will determine to a large extent the maximum achievable CMRR and positive PSRR. For a CMRR of 85 dB, the mismatch must be less than 0.03 percent. The high degree of cross coupling makes this possible.

CMOS amplifiers are notorious for exhibiting large voltage noise. While this design reveals no cures for the problem, the superiority of the silicon gate processing over metal gate and the choice of Native p-channel devices that are allowed to dominate the noise picture leads to voltage noise performance (Fig. 6(a)) that is quite acceptable for general-purpose applications. With a voltage noise density of typically 36 nV/√Hz at 1 kHz and 30 nV/√Hz at 10 kHz, it compares reasonably well with general-purpose bipolar and BI-FET quads. There is clearly room for improvement at the low-frequency end, however, with 80 and 220 nV/√Hz found at 100 and 10 Hz, respectively. One bright spot is that the wafer-to-wafer and run-to-run variations are minimal. There have been no observed cases of popcorn noise.

In order to protect the inputs from ESD damage, a 200-Ω polysilicon resistor is placed in series with each input and protection diodes are connected from each input gate to either rail. These diodes are actually parasitic transistors and can protect with a low impedance on the rails (i.e., in the circuit board) or with rails floating as occurs during handling. In the former situation the protection is by diode action. In most cases, continuous currents of up to 50 mA can be put through these diodes while the IC is powered up without triggering a destructive latch. In the latter situation the floating supply rails allow the parasitic transistors that the diodes represent to combine and form a desirable, protective, bidirectional SCR differentially across the otherwise vulnerable input pins. The input bias and input offset currents that result from these protection diodes are dominated by the upper diodes which consistently outleak the bottom diodes causing the bias current to always exit the pins. This current is exceptionally low and typically only 50 fA at room temperature (even less in plastic). It is proportional to the voltage across the upper diode and thus varies with common-mode voltage at the rate of about 10 fA/V, which is equivalent to an input resistance of 100 tΩ. The leakage currents from the respective inputs track well with temperature (Fig. 6(b)) and rise to only 5 pA typically at +125°C.

IV. The Integrator

As mentioned earlier, the integrator is a compound stage that is actually two stages in one: a preceding feed-forward noninverting block, and a push–pull inverting output block that drives the load rail to rail. The feed-forward stage (Fig. 7) is a relatively simple circuit that consists of $M5$, $M19$, $M20$, and $M6$. This small, lightly loaded, single-ended stage is able to deliver about 40 dB of gain which is largely responsible for the high overall gain of the amplifier. The output of this interior stage can swing rail to rail which is essential in delivering the large gate overdrive to the big output n-channel $M8$ (Fig. 8). The maximum overdrive is clamped at 6 V by $Z1$ so as to act as a current limit. The stage is fed forward at high frequencies by capacitor C_{FF} at the frequency given by

$$f = g_{m_5}/(2\pi \cdot C_{FF}) = 550 \text{ kHz}. \quad (1)$$

This frequency is about one-third of the unity cross frequency of the amplifier. Although C_{FF} could have been driven from the first stage directly, it is more effective being driven by a high-transconductance driver such as $Q23$. $Q23$ also proves useful in providing feed-forward compensation all the way to the large output p-channel

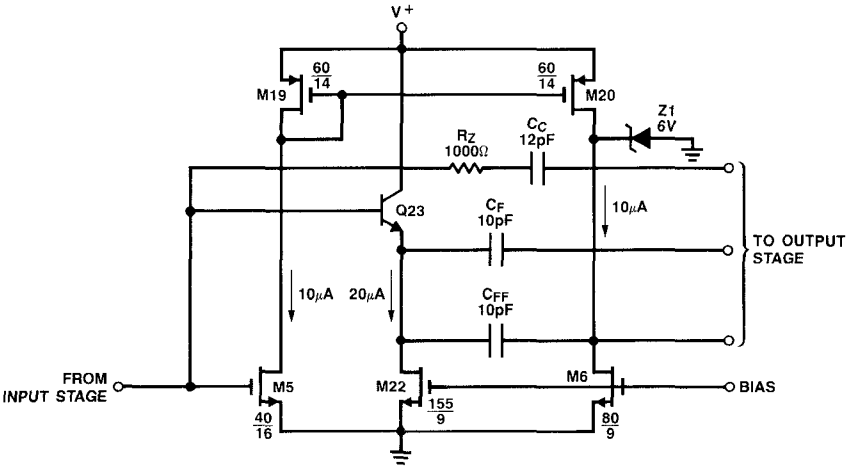


Fig. 7. The feed-forward stage portion of the integrator.

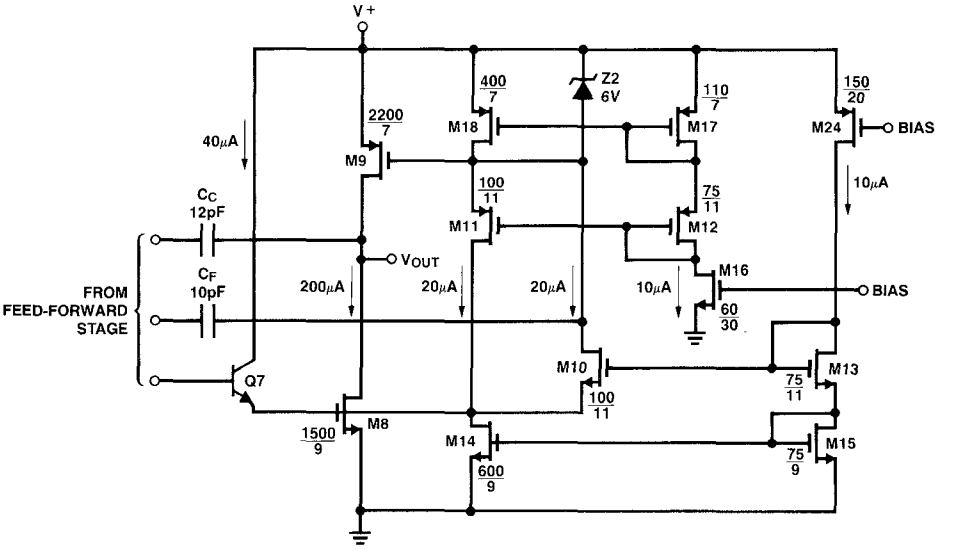


Fig. 8. The output stage with rail-to-rail swing capability.

$M9$. Near the unity cross of the amplifier, the input stage (via $Q23$, C_{FF} and C_F) effectively has control of the gates of the two large output devices lending ac stability to the amplifier.

The output stage (Fig. 8) must solve a level shifting problem that has plagued rail-to-rail designs for some time. Elaborate solutions have been proposed that combine multiple embedded feedback loops that are in effect op amps within op amps. To succeed as a general-purpose quad, a simpler solution had to be found. The signal path of the output stage that resulted consists of just five devices, $Q7$ and $M8$–$M11$. The complementary output devices $M8$ and $M9$ change their conduction in response to the complementary common-gate level shifters $M10$ and $M11$. These common-gate devices alter their relative conduction levels in turn via the voltage drive of the high-transconductance driver $Q7$.

Quiescently, the stage biases as follows. Complementary currents from the bias generator flow into complementary stacks of diode-connected transistors whose $2V_{GS}$ potentials are used to bias the gates of $M10$ and $M11$. Separate but equal area ratioing of the top and bottom clusters of complementary transistors causes $M8$ and $M9$ to carry 200 μA when the level shifters each carry half (20 μA) of the current from current source $M18$. This condition occurs when $Q7$ conducts half (40 μA) of the current from current sink $M14$. The class AB current is stable with supply and processing variations being only dependent upon the bias current generator and device area ratioing.

Under small-signal conditions, $M8$ is directly driven by $Q7$ and $M9$ is driven in like phase via $M10$ feeding the source of $M11$. $M10$ thus acts like a broad-band noninverting stage with a gain of slightly more than one. The total transconductance of the output stage is found by simply adding the transconductances of $M8$ and $M9$ which are roughly equal. This combined transconductance is about 2.5 mmho which is high enough to provide some gain into low-impedance loads even under small-signal conditions, which is worst case. Under large-signal conditions the gain will climb as either the top or bottom device

begins to conduct load current. This behavior is unique to drain-output or collector-output type designs. The high small-signal transconductance is also a help in driving capacitive loads because the pole frequency caused by load capacitance is proportional to this transconductance. Under small-signal conditions, the amplifier will typically handle 100 pF over the military temperature range. Under large-signal conditions the capacitive load handling capability increases.

When the output stage is driven to sink a lot of current, $Q7$ absorbs all the current from $M14$ and pulls the gate of $M8$ up to a V_{BE} less than the supply rail or a V_{BE} less than 6 V, whichever is less. Under these conditions $M10$ is completely shut off and $M11$ must carry the full current of 40 μA from $M18$. The source of $M11$ rises to its maximum point thus cutting back on the conduction of $M9$ but not turning it off. Leaving $M9$ in an idling state is important to keeping large signal distortion at a minimum, because otherwise there would be a crossover gap that would need to be closed by rapid slewing. Under conditions of strong sourcing, $Q7$ shuts off and $M14$ pulls all of its current through $M10$. Inasmuch as this current is twice as much as $M18$ can provide, $M11$ is shut off as the gate of $M9$ is pulled low. This condition results in a high impedance on the drain of $M10$ allowing the device to exhibit substantial voltage gain. While the additional gain from this fourth stage is welcome, the phase shift it adds to the signal path is certainly not. This is why the second feed-forward capacitor C_F is needed to feed around $M10$. In the strong sourcing situation, the opposing output device again does not shut off but instead merely idles back and this is just as important to distortion as the top-side idle. Ultimately the swing on the gate of $M9$ will come to a stop about $2V_{DS}$ from the negative rail or 6 V from the positive rail. The large swing drive to both output devices is very important in driving loads close to the rails.

V. The Bias Circuit

The lack of a good, simple bias circuit has been a damper on analog CMOS performance. Aside from zeners, which do not work on +5-V supplies, it is difficult to obtain an accurate potential in CMOS let alone a repeatable potential with a positive temperature coefficient (TC). The positive TC is useful in moderating the growth in transistor transconductance at cold temperatures and holding it up at high temperatures. The accuracy is needed to hit certain performance targets and the repeatability is needed to guarantee that performance on the data sheet. It is also desirable to be able to guarantee the performance over the entire supply range and this requires that the bias circuit possess high PSRR. Finally, this particular application needs a bias circuit with complementary outputs and the ability to work down to less than 3 V, which is the lower limit of operation for the amplifier. These needs are all met by equipping the substrate n-p-n's with lateral collector elements ($Q26$ and $Q27$) and operating them at

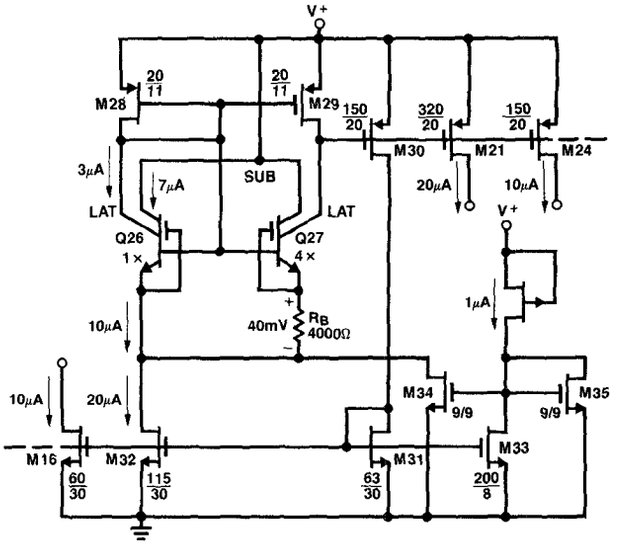


Fig. 9. The bias circuit which features area-ratioed lateral/vertical n-p-n transistors to define a ΔV_{be}-related current.

different current densities to create a ΔV_{BE}-based bias circuit (Fig. 9).

In laying out such a transistor, the lateral collector is made to surround the emitter and is placed as close as feature size permits to that emitter so as to maximize the collection of electrons laterally as opposed to vertically. This lateral base width of 4 μm is defined by polysilicon and the resultant structure looks much like a concentric MOSFET which in fact it actually is. Conduction from emitter to lateral collector due to parasitic MOS action is discouraged by biasing the parasitic gate such that surface inversion is weak or nonexistent. For the case where the gate is tied to the emitter, which is very convenient from both a circuit and layout standpoint, a small amount of subthreshold current will flow that is insignificant for noncritical applications such as bias circuits. Using the transistors in a bandgap voltage reference on the other hand would require that this effect be taken into account. Bandgap designers need also consider the effect due to the onset of large-signal injection. For minimum-size emitters built in a light well background such as these it occurs at 10 μA or more. For maximum accuracy, the multiple-emitter transistor $Q27$ should be built with individual wells for each emitter, though the wells were made common in this application in order to reduce die area consumption.

The split of emitter current between the vertical and lateral paths is not stable with normal variations in processing as it depends upon controlling the ratio between the vertical and lateral base widths, among other things. The performance of a good circuit design using this type of transistor should not be dependent upon the absolute value of the split. For a drawn lateral width of 4 μm and a well depth of about 5 μm, the current flows about one third in the lateral collector and two thirds in the vertical collector. Increases in collector voltage will modulate the split as the Early voltages of the two collec-

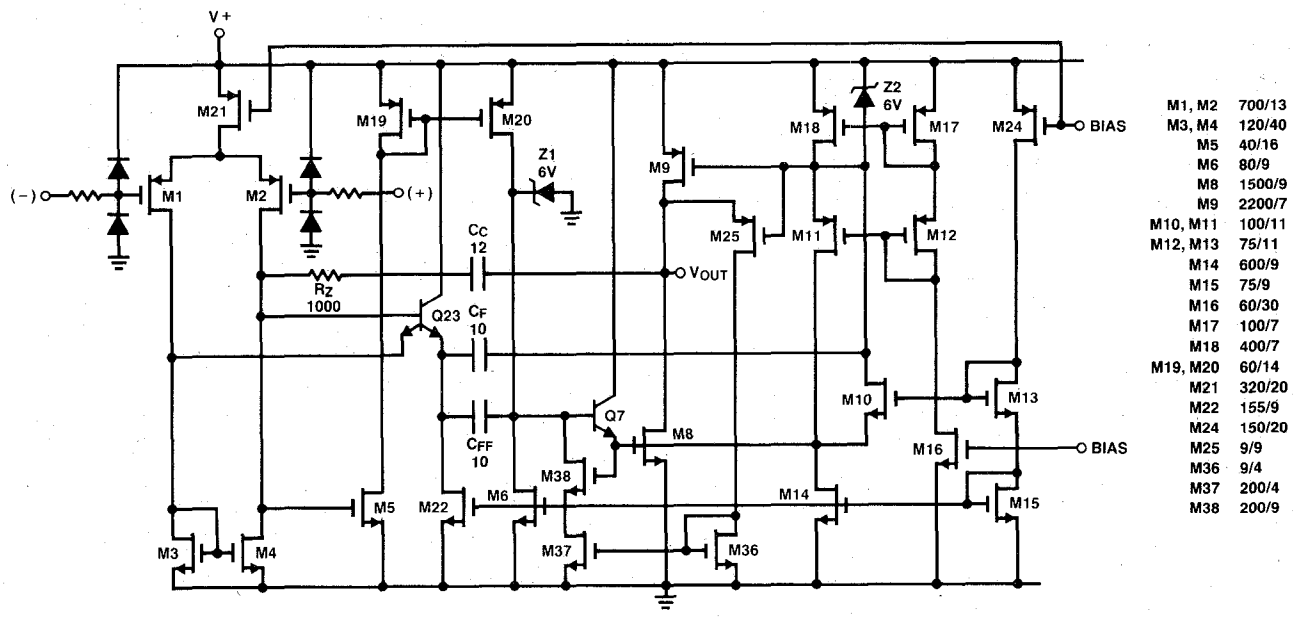


Fig. 10. Circuit for the entire op-amp cell. One such cell consumes approximately 0.71 mm^2 of die area.

tors are not equal. The vertical collector has an Early voltage of 90 V, whereas for the lateral collector it is only 15 V with breakdown occurring at around 8 V.

In the circuit, $Q26$ and $Q27$ are connected in bootstrap fashion such that the collector–base voltage of each collector type on each device is approximately 0 V. The duty of absorbing supply-voltage changes falls upon long-channel devices $M30$ and $M32$ which results in high PSRR. Negative feedback introduced into the "tail" of the bipolar core of the circuit serves to stabilize the operating point of the circuit where ΔV_{BE} is impressed across R_B according to the familiar relation

$$I_{M16} = I_{M24} = (k \cdot T/q \cdot R_B) \cdot \ln(J_{26}/J_{27}). \quad (2)$$

Whereas the calculated ΔV_{BE} is 36 mV for 300 K, the observed value is closer to 38 or 40 mV due to the secondary effects previously mentioned. R_B is constructed out of the material with the best control in the process, the p^+ source/drain implant. In addition to being under good control, it also possesses a relatively mild TC of approximately +500 ppm which when combined with ΔV_{BE} gives the complementary bias current outputs a net TC of +2800 ppm/°C. The start-up needs of the circuit are met by $M33$–$M35$ and by a long 5-μm-wide well resistor that pinches off at about 5 V and draws about 1 μA. Over the 5–15-V supply range of the op amp the bias circuit helps hold the supply current changes down to just 6 percent and the majority of this change is due to output impedances of the transistors in the op-amp cells themselves.

VI. Performance

The complete op-amp cell schematic shown in Fig. 10 has two circuit portions not previously described which are needed to address the situation where the feedback loop is broken and the inputs are overdriven as will occur when the outputs clip against the rails. One is the addition of a second emitter to $Q23$ to limit the overdrive to $M5$ and the other is the inclusion of $M25$ and $M36$–$M38$ to eliminate potential instability as the amplifier output recovers from being collapsed against the upper rail. Small sense transistor $M25$ straddles $M9$ and delivers a current whenever $M9$ collapses into its triode region. This current passes through a gained-up mirror to blend in negative feedback transistor $M38$, which serves to reduce the forward gain and in doing so assists the four-stage amplifier in reestablishing equilibrium cleanly. The rail-to-rail swing and clean clipping behavior of the amplifier is shown in Fig. 11 with a 2-kΩ capacitor coupled load and 1-kHz excitation. The output swings to within 130 mV of the +5-V rail and to within 100 mV of ground. For a 600-Ω load the swings are to within 390 and 300 mV, respectively.

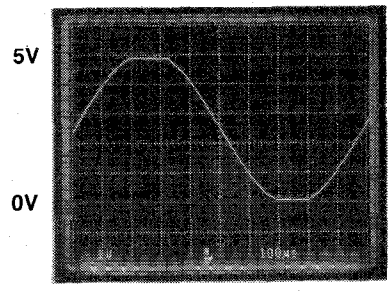
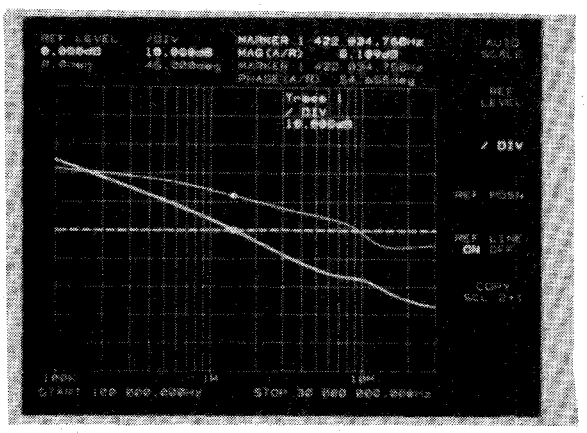


Fig. 11. Output swing at 1 kHz on a +5-V supply into a 2-kΩ capacitor coupled load. The swing extends to 100 mV of the negative rail and 130 mV of the positive rail.

Small-signal gain and phase is best shown on the network analyzer plot in Fig. 12(a) where the unity cross for the particular device measured was 1.4 MHz with a phase margin of 54° and a gain margin of 17 dB. The mild bump in the gain curve (lower trace) is due to the integrator and never presents a threat to the amplifier. Under worst-case



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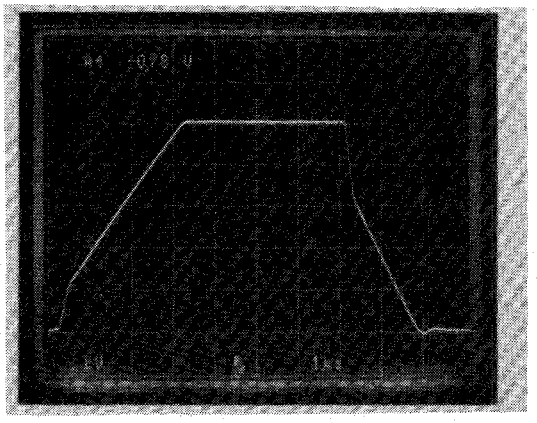

(b)

Fig. 12. (a) The small-signal gain and phase response versus frequency from 100 kHz to 30 MHz. The unity-gain frequency is 1.4 MHz, the phase margin is 54°, and the gain margin is 17 dB. (b) The large-signal step response in the voltage-follower mode in which the amplifier displays the classic slew steps and asymmetry caused by "tail" capacitance. Positive-going slew rate is 1.45 V/μs while negative-going slew is 2.1 V/μs.

conditions of heavy sinking and cold temperatures it only peaks a few decibels. The phase curve (upper trace) shows evidence of phase holdup due to the beneficial effects of the zero setting resistor R_Z in series with the main compensation capacitor C_C.

The large-signal step response is shown in Fig. 12(b) for the voltage-follower configuration. Note the presence of the slew steps and slew asymmetry that one would expect from an input stage that features inverting p-type devices. The slew rate is degraded rising, assisted falling, and typically averages 1.7 V/μs. Despite the use of feed-forward compensation, the settling time is not impaired. While driving 2 kΩ from -5 to $+5$ V with an inverting gain of one, the output settles to within 0.01 percent in 7 μs on the positive-going edge and 6.5 μs on the negative-going edge.

The remainder of the amplifier performance is summarized in Table I. For operation on a 15-V supply, the specifications are nearly identical except for short-circuit current, which doubles, and for output swing, which does not come as close to the rails because of the larger load currents that must be delivered into the rated 2-kΩ and 600-Ω loads. For example, in driving 2 kΩ, the output swings to within 370 mV of the upper rail and 260 mV of the lower rail. The input common-mode range will still extend from ground to within 2 V of the upper rail. Operation over the full military temperature range of -55 to $+125$°C is guaranteed for both 5- and 15-V supplies.

TABLE I
TYPICAL PERFORMANCE (PER OP AMP) AT $V^+ = +5$ V AND $T_A = 25$°C

V_{OS}	1mV
V_{OS} Drift	1.3μV/°C
E_n@1kHz	36nV/$\sqrt{\text{Hz}}$
I_b	50fA
CMRR	85dB
+PSRR	85dB
−PSRR	95dB
Common Mode Range	−0.3V to 3.1V
Differential Range	±5V
Unity Gain Bandwidth	1.5MHz
Slew Rate	1.7V/μs
THD (@10kHz with $A_V = -10$)	0.01%
Voltage Gain into 2kΩ; Source/Sink	2000 / 500 V/mV
Voltage Gain into 600Ω; Source/Sink	1000 / 250 V/mV
Output Swing into 2kΩ; Low/High	0.10V / 4.87V
Output Swing into 600Ω; Low/High	0.30V / 4.61V
Output Current (Short Circuit)	±22mA
Supply Current	350μA
Supply Voltage Range (Guaranteed)	4.75V to 15.5V

No special processing was used to control latch-up sensitivity, yet the quad is not susceptible to latch-up over the entire military temperature range. For example, input excitation from low-impedance sources can be applied to either or both inputs and then the device powered up in any supply sequence without fear of latch. At least ± 30 mA can be accommodated under the worst-case conditions of high supply voltage (15 V) and high ambient temperature (125°C). This was achieved via careful layout throughout the chip and output transistor geometries that embed the drain completely within the surrounding source.

VII. CONCLUSION

A CMOS amplifier design has been presented that is well suited to operation on a single+5-V supply and features rail-to-rail output swing. Performance limitations that have limited CMOS amplifiers in the past are not a problem with this approach. Specifications regarding V_{os}, V_{os} drift, I_B, I_{OS}, broad-band noise, voltage gain, and load driving capability are all equal to or better than most commercially available quad op amps whether constructed with CMOS, BI-FET, or bipolar technology. Because this performance has been achieved via circuit design and layout techniques as opposed to special analog CMOS processing, the design has significance beyond its use in a stand-alone product. Advanced digitally based system chips built on CMOS processes can now realize the benefits of a good on-chip op amp provided that the proper layout considerations are met.

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