A Micropower Chopper-Stabilized Operational Amplifier Using a SC Notch Filter With Synchronous Integration Inside the Continuous-Time Signal Path

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***Abstract*—A micropower chopper stabilized opamp is presented. The new topology incorporates a switched capacitor filter with synchronous integration inside the continuous time signal path virtually eliminating chopping noise. A three-stage amplifier with multipath nested Miller compensation is modified to incorporate chopping of the input stage, sinc filtering to notch any chopping ripple, and a compensation scheme to maintain an undistorted high-speed signal path. Characteristics of the amplifier presented include rail to rail input and output operating on supplies of 1.8 to 5.5 V over −40°C to 125°C. Quiescent supply current is 17 μA, input offset is 3 μV, input offset drift is 0.02 μV/°C, GBW is 350 kHz, and the chopping frequency is 125 kHz. Die area is 0.7 mm^2 using a precision analog mixed-signal CMOS process combining low-noise 0.6-μm analog transistors with 0.3-μm digital CMOS capability.**

***Index Terms*—Choppers, CMOS analog integrated circuits, operational amplifiers.**

I. Introduction

MODERN chopper and autozero opamps have significantly reduced or virtually eliminated switching noise [1]–[5]. Different techniques are used and come with tradeoffs in input-referred noise (en) and quiescent supply current (Iq). The inherent tradeoffs between basic chopper and autozero topologies are known [6]. Basic choppers maintain the broadband noise characteristics of their input stage, but shift their input offset and low-frequency noise up to the chopping frequency (fs) creating large ripple at the output. Basic autozero topologies do not shift their input offset to their autozero frequency (fs) like choppers, but overall input-referred noise is increased due to aliasing or folding back of their broadband noise spectrum sampled during their zeroing cycle. A significantly increase in Iq is required in autozero topologies in order to achieve the desired noise levels after this noise folding [2], [3]. This makes it very desirable to use a chopper in micropower applications and solve the basic limitation of chopper ripple at fs. Previous work has shown some improvement over basic topologies by employing both autozeroing and chopping [4], but is not optimum for micropower applications due to the large overhead in Iq. Another previous low-noise chopper topology has achieved desirable en versus Iq tradeoffs by utilizing a conditionally stable multipath feedforward compensation technique [5]. Although this conditionally stable amplifier is easily frequency compensated in most applications, it does not exhibit the −20 dB/decade frequency roll-off expected from a general purpose operational amplifier (opamp).

This paper will describe a chopper-stabilized opamp using a switched-capacitor (SC) notch filter with synchronous integration inside the continuous-time signal path to reduce chopping noise well below the total rms noise. The opamp maintains the benefits of chopping while notching the ripple at fs. This is done without an increase in Iq, allowing for micropower applications.

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II. Background

A. Input Stage Issues

Low-noise design uses a significant portion of the supply current in the input stage to reduce the noise while the following stages will typically increase the total supply current in proportion to the input stage current. For this reason, it is important to minimize the input stage noise for a given stage current. As a general practice, the noise of any active load should be minimized so that the only significant contributor to noise is the input pair. Then the input pair noise is reduced by increasing the gm of the devices. The limit on gm is reached by increasing W/L to the point where the increased capacitance sets the desired dynamic characteristics or the device enters weak inversion. In both cases further increases in gm become directly proportional to stage current as both W/L and current must be increased by the same factor. This results in en^2 being inversely proportional to increases in W/L and current. With a significant portion of the total supply current allotted to the input stage of low-noise and/or micropower designs an interesting figure of merit is en$^2 \times$ Iq.

B. Autozeroing and the Sampling Process

The inherent tradeoffs between basic chopper and autozero topologies are known [6]. Basic choppers maintain the broadband noise characteristics of their input stage, while basic autozero topologies suffer from aliasing or folding back of their broadband noise spectrum sampled during their zeroing cycle to increase the overall input-referred noise. This is because autozeroing employs a sample-and-hold either directly at the input or at a point in the signal path where a significant amount of the sampled noise is reflected back to dominate the input-referred noise level. Although there are many autozero topologies used, an understanding of the noise folding occurring in a

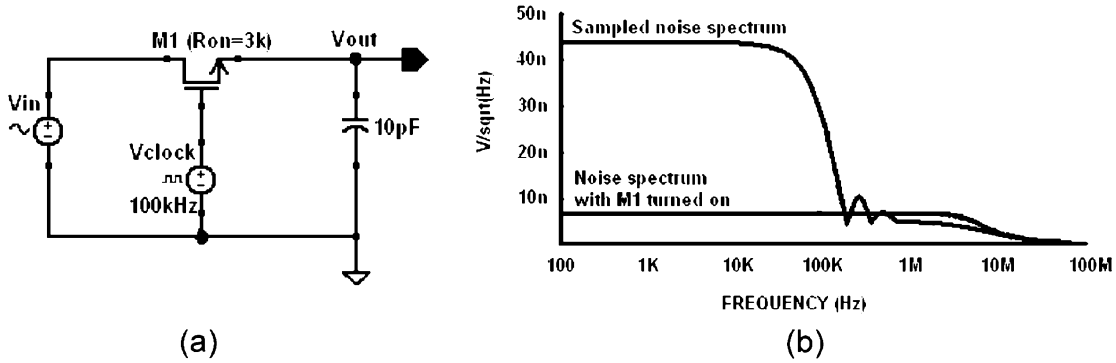

Fig. 1. Sampling process. (a) Simple sample and hold. (b) Noise spectrums for example case.

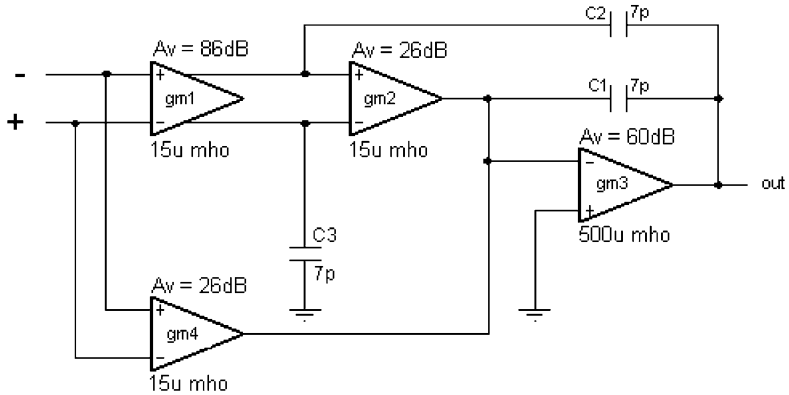

Fig. 2. Basic three-stage amplifier with multipath nested Miller compensation.

simple sample-and-hold is key to working through the many possible design tradeoffs in both autozero and chopper topologies. Fig. 1(a) shows a simple sample-and-hold and Fig. 1(b) plots the noise spectrum for an example case with a 10-pF hold capacitor sampled at 100 kHz and 50% duty cycle. The noise plot shows the original noise spectrum with sampling switch transistor, M1, turned on using a traditional small-signal AC noise analysis in SPICE, and also the sampled noise spectrum obtained with the circuit running with the 100-kHz clock by utilizing periodic steady-state and periodic noise analysis in Spectre RF [7]. Both analyses result in the expected integrated noise of 20 μVrms while demonstrating a factor of 6 increase in the low-frequency noise floor of the sampled spectrum due to noise folding. Autozero circuits typically increase the noise floor 3 to 5 times due to noise folding, requiring an increase in stage current of 9 to 25 times to achieve the required noise floor. Many switching functions can be very complex and it is easy to unintentionally sample a wideband noise signal, completely destroying the noise floor. For this reason, the authors have relied heavily on full-circuit noise simulations for verification using periodic steady-state and periodic noise analysis in Spectre RF for the amplifier presented. More details about this simulation tool and technique can be found in [7].

III. Circuit Implementation

Fig. 2 shows a basic three-stage amplifier with multipath nested Miller compensation [8]. This topology can be thought of as a high-gain three-stage opamp, $\mathrm{gm1}$, $\mathrm{gm2}$, and $\mathrm{gm3}$, in parallel with a wider bandwidth two-stage opamp, $\mathrm{gm4}$ and $\mathrm{gm3}$. DC precision is determined by the input stage $\mathrm{gm1}$ in the high-gain path, while high-frequency response and phase margin are dominated by the two-stage path. Proper selection of gm's and compensation maintains the bandwidth and settling characteristics of a two-stage Miller compensated opamp with minimal Iq increase, achieving a good gain–bandwidth (GBW)/Iq relationship. Fig. 3 plots the overall open-loop gain and the individual frequency responses of both signal paths. The three-stage path of $\mathrm{gm1}$, $\mathrm{gm2}$, and $\mathrm{gm3}$ has a total DC voltage gain of 172 dB, but is not unity-gain stable, while the two-stage path of $\mathrm{gm4}$ and $\mathrm{gm3}$ only has a total DC voltage gain of 86 dB, yet maintains a first-order roll-off at unity-gain crossover for stability. The difference in DC gains for each path results in the DC offsets and low-frequency errors of $\mathrm{gm4}$ and $\mathrm{gm2}$ being divided down by the DC gain of $\mathrm{gm1}$, 86 dB or a factor of 20 000. Typical offsets of less than $\pm$20 mV are reduced to ± 1 μV. However, the offsets and low-frequency noise of $\mathrm{gm1}$ remain referred directly to the input. This is addressed by adding basic chopper stabilization to input stage $\mathrm{gm1}$ in the DC path in Fig. 4. This significantly reduces offset, drift, and flicker noise, but shifts $\mathrm{gm1}$ offset to fs as expected, creating a large output ripple. Fig. 6 shows how a 10-mV offset inserted into the input stage $\mathrm{gm1}$ results in output ripple. The basic chopper shown in Fig. 4 will create 75-mVpp ripple at its chopping frequency of 125 kHz. The elimination of this ripple is achieved in Fig. 5 by integrating the output of $\mathrm{gm1}$ synchronous to the chopping before transferring

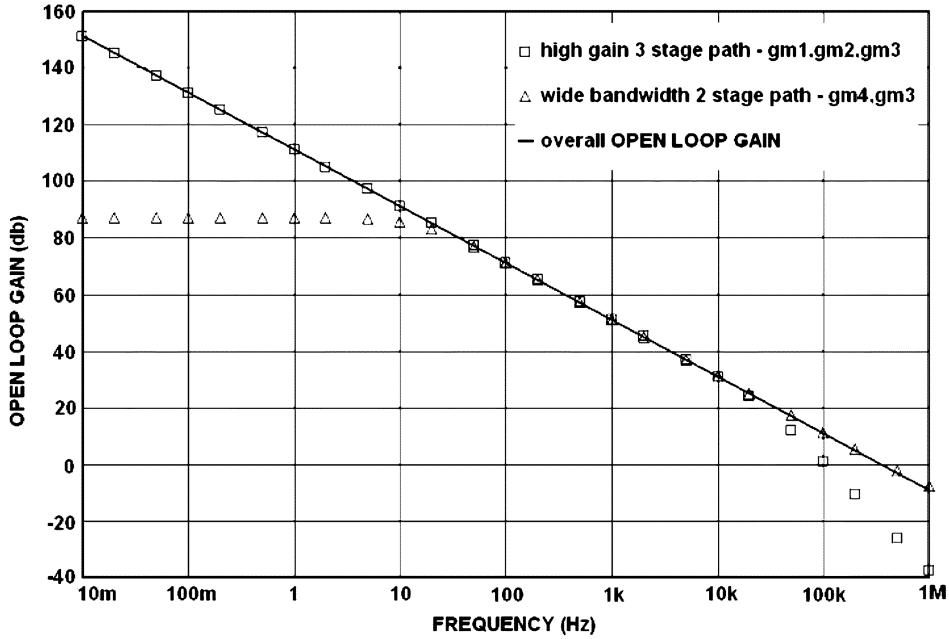

Fig. 3. Frequency responses.

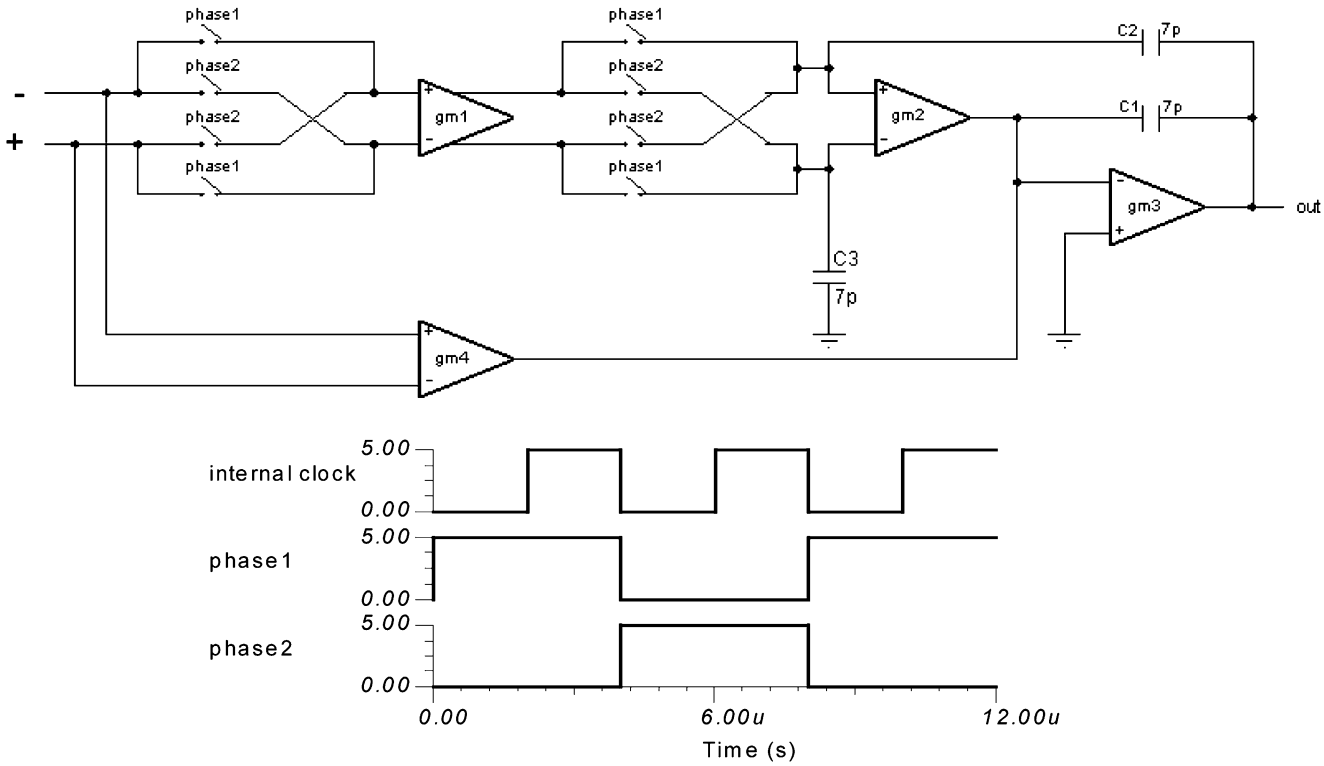

Fig. 4. Chopping added to input stage.

the signal to the next stage $\mathrm{gm2}$. This represents the circuit we have built and will describe in more detail. Consider that a positive offset current flows from $\mathrm{gm1}$ during phase1 and an equal and opposite negative offset current flows during phase2 as a result of chopping its input offset voltage. This offset signal is nulled by integrating half of the positive phase1 offset current and half of the negative phase2 offset current onto C5 during phase3 for a net charge of 0 before transferring it to $\mathrm{gm2}$ during phase4. In phase4, C6 is used to integrate the equal and opposite offset currents from chopping $\mathrm{gm1}$ for a net charge of 0 as well. C5 and C6 work in tandem during phase3 and phase4 to integrate and transfer the chopped offset current from $\mathrm{gm1}$ as shown by the timing diagram. Referring to Fig. 6 again, a 500X reduction in ripple is shown with the use of the notch filter as described. Even though the filter provides a deep notch for the ripple, it also creates a concern for the normal signal

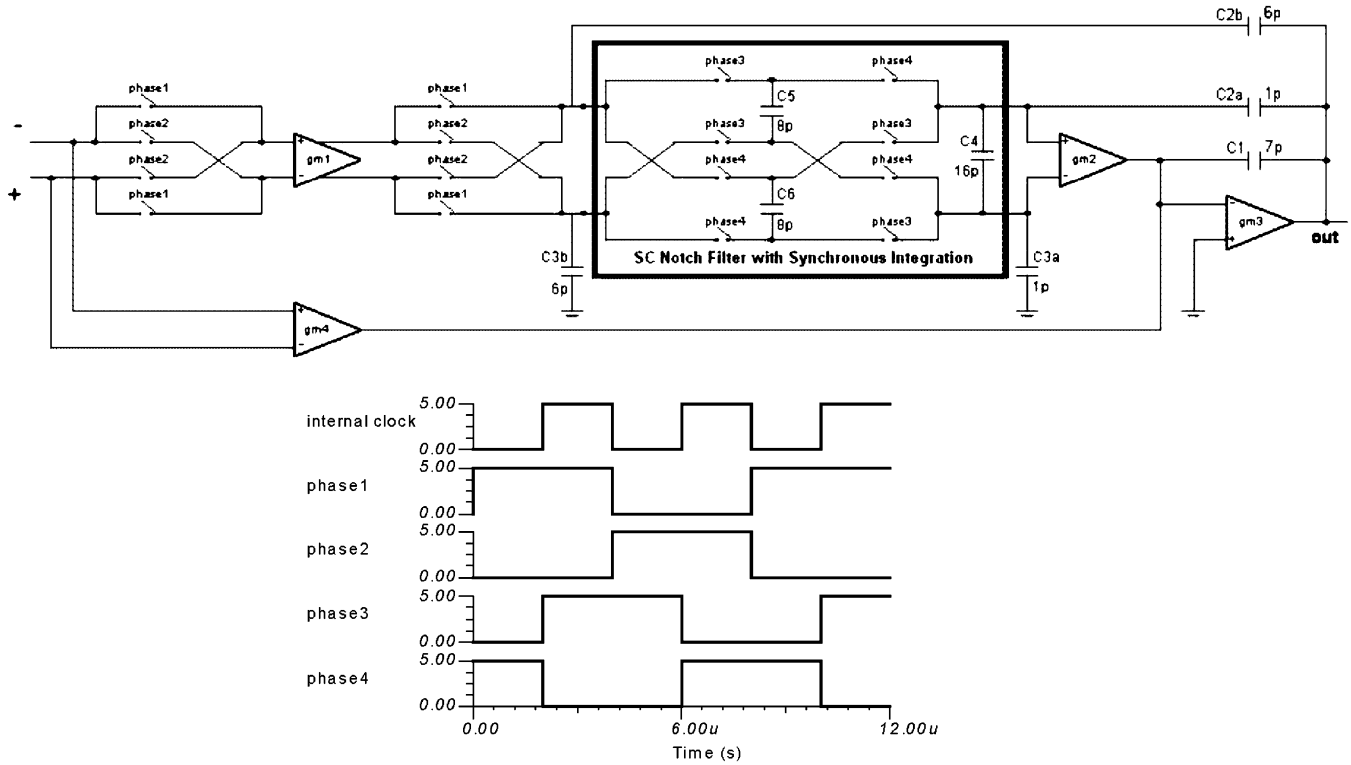

Fig. 5. SC notch filter with synchronous integration included.

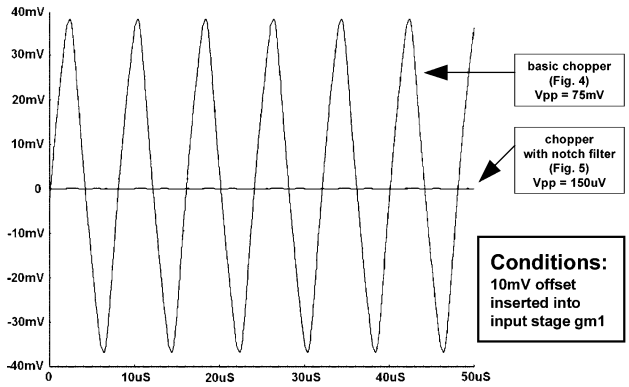

Fig. 6. Transient simulation showing 500X less ripple.

transfer. A delay is created by the integrate and transfer action which will affect the circuit differently depending on how the compensation capacitors are connected. Notice that C2 and C3 have been split into the "b" portion returning to the filter input and the "a" portion returning to the filter output. Returning compensation to the filter input through C2b has the advantage of maintaining a continuous time path for the normal signal, but the potential for local loop instability arises due to the delay of the switched capacitor filter being in the local feedback path through C2b. Returning the compensation to the filter output though C2a provides a direct feedback path for local loop stability, but now the normal signal is delayed by the SC filter and may distort the large-signal response. This design returns most of the compensation, 6 pF, to the filter input, maintaining good continuous-time characteristics, and 1 pF is returned to the filter output for local loop stability. The inclusion of C4 at the filter output also aids stability by rolling off the magnitude of the filter path before the delay creates excess phase shift in the high-gain three-stage path. Stability was tested during the design by injecting a small transient current pulse at each internal node and monitoring the voltage response on the node over many clock cycles. The ringing on the node relates directly to the damping factor and thus the stability of any internal loop affected.

A more detailed circuit diagram of the input stage used for $\mathrm{gm1}$ in the circuit built is shown in Fig. 7. A rail-to-rail input with p-channel inputs MP0 and MP1 and complementary n-channel inputs MN0 and MN1 is used. The input common-mode crossover error created by the inherently different offsets in these two different input pairs is not an issue in this design since these offset errors are chopped out. The input pairs are fed into a folded cascode structure with common-mode feedback devices MN5 and MN6, setting the output common-mode bias voltage. It is important to maximize the output impedance of $\mathrm{gm1}$ and hence the DC gain because as previously discussed any offset from the following gm stages or the errors from the high-speed $\mathrm{gm4}$ path will be divided by $\mathrm{gm1}$'s 86 dB of voltage gain to contribute to input-referred offset voltage. These offset errors are not chopped out. For this reason, additional cascodes MP4 and MP5 are included. The sizes of MP4 and MP5 are minimized to reduce the parasitic capacitance on the output of $\mathrm{gm1}$ because charging of these parasitics at the chopping frequency effectively reduces the DC gain as well.

The complete chip is shown in simplified block form in Fig. 8. A low-current bias generator runs on a 1.8 to 5.5 V supply and consumes 1 μA. A low-dropout voltage regulator

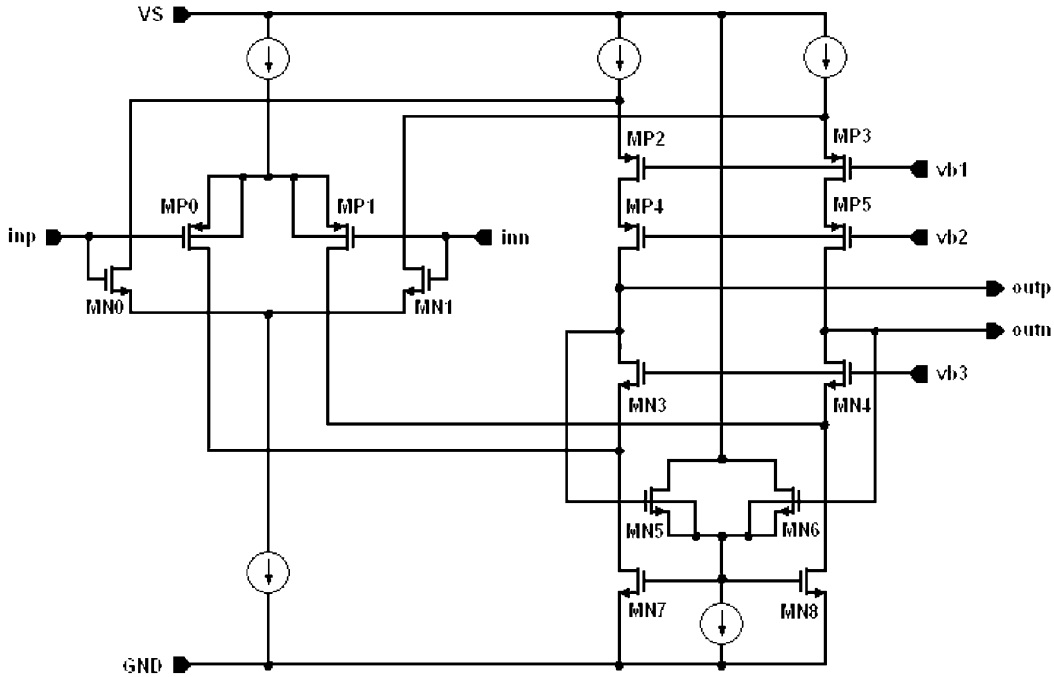

Fig. 7. Input stage used for $\mathrm{gm1}$.

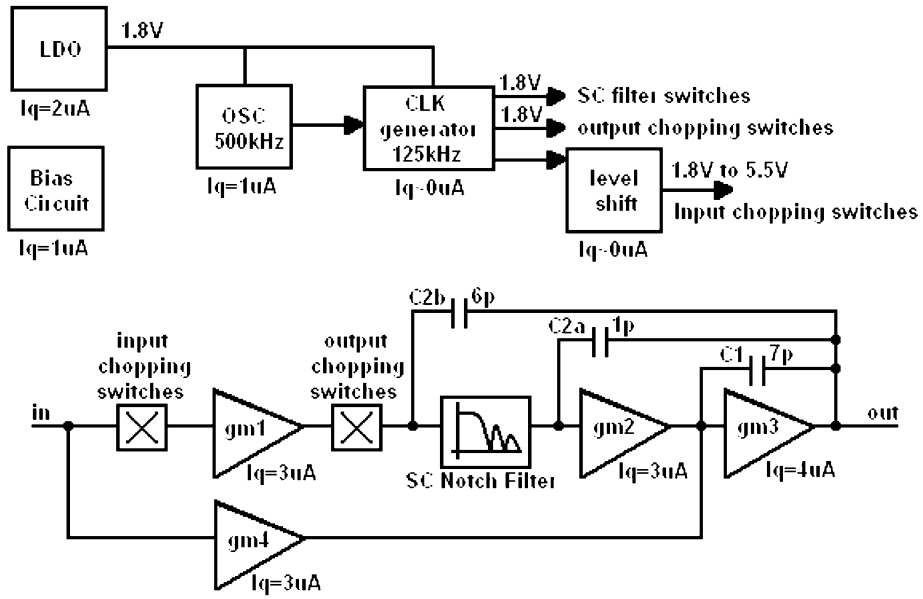

Fig. 8. Simplified block diagram.

(LDO) is used to provide a subregulated 1.8 V independent of supply. The internal 1.8-V rail is used to power the oscillator and logic for the clock generator and switches in the SC notch filter and output chopper. Running these sections on a minimum voltage significantly reduces critical charge injection, power supply sensitivities, and logic glitches. The oscillator is set at 500 kHz and the clock generator includes a divide-by-two stage to create an accurate 50% duty cycle at 250 kHz, which in turn creates the accurate phase relationships of the 125-kHz clock signals used to drive the switches. Complete offset reduction of $\mathrm{gm1}$ requires the chopping signal to have less than a 1-ns timing skew in the 50% duty cycle. The SC notch filter will not be affected by timing skews at this level. This was achieved with careful attention to layout and the use of post-layout parasitic extraction tools. The input switches require full supply swing of 1.8 to 5.5 V, and a logic translator referenced to supply is used to drive these switches. The switches use a standard pass-gate structure with parallel nMOS and pMOS devices, but the 1.8-V operation is aided by the use of a low-threshold nMOS device available on the process. The LDO, oscillator, and clock generator consume 3 μA. Stages $\mathrm{gm1}$ and $\mathrm{gm4}$ use similar folded cascode structures as shown in Fig. 7. The two input stages consume 6 μA. $\mathrm{Gm2}$ also uses a folded cascade structure but requires only pMOS input devices with its fixed

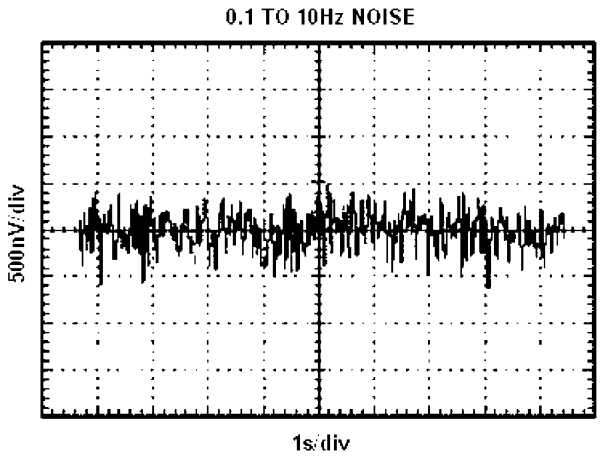

Fig. 9. Low-frequency noise measurements of 1.2 μVpp over 0.1 to 10 Hz.

internal common-mode voltage. This stage consumes 3 μA. The output stage $\mathrm{gm3}$ is a class-AB biased rail-to-rail output stage consuming 4 μA without load. Not shown on the simplified block diagram is that a fully differential signal path from the input through the SC notch filter as shown in Fig. 5 is used. Symmetry of charge injection errors in this differential path is critical to achieving low offset. All devices and capacitors were laid out to match in the differential path as good design practice would dictate, even though precise capacitor matching is not required with this topology.

IV. Measured Results

Silicon noise spectrum measurement of 55 nV/$\sqrt{\text{Hz}}$ was accurately predicted by circuit simulation using SpectreRF's periodic steady-state and periodic noise analysis. Low-frequency measurement of 1.2 μVpp over 0.1 to 10 Hz shown in Fig. 9 demonstrates that the en of 55 nV/$\sqrt{\text{Hz}}$ is essentially flat to DC. Input offset of 3 μV and offset drift of 0.02 μV/°C are shown in production histograms in Fig. 10 [9]. Effective use of multipath nested Miller compensation can be seen by minimal gain and phase anomalies in the measured open-loop gain and phase plot shown in Fig. 11. This plot does not extend to the very low frequencies where the part's simulated DC open-loop gain is 172 dB. Test equipment resolution limits device measurement to the simulated level, but measurements have shown an open-loop gain $\mathrm{A_{ol}}$ in excess of 130 dB. Large-signal transient behavior is shown in Fig. 12. Other general characteristics include rail-to-rail input and output operating on supplies of 1.8 to 5.5 V over -40°C to 125°C. Iq is 17 μA and GBW is 350 kHz. The device maintains all the characteristics of general-purpose operational amplifiers without chopper stabilization, making it applicable for a broad range of applications. Table I compares this work to other chopper and autozero opamps with favorable figure of merits for both $\mathrm{en}^2 \times \mathrm{Iq}$ and $\mathrm{GBW/Iq}$, demonstrating its application to micropower and/or low noise. This precision amplifier fits in the SC-70, an industry standard "miniature" transistor package. Die area is 0.7 mm^2 on a precision analog mixed-signal CMOS process combining low-noise 0.6-μm analog transistors with 0.3-μm digital CMOS capability. A chip photograph is shown in Fig. 13. Only about one third of the die area is used for the signal path, making this design very attractive for use in larger mixed-signal or system-on-chip designs.

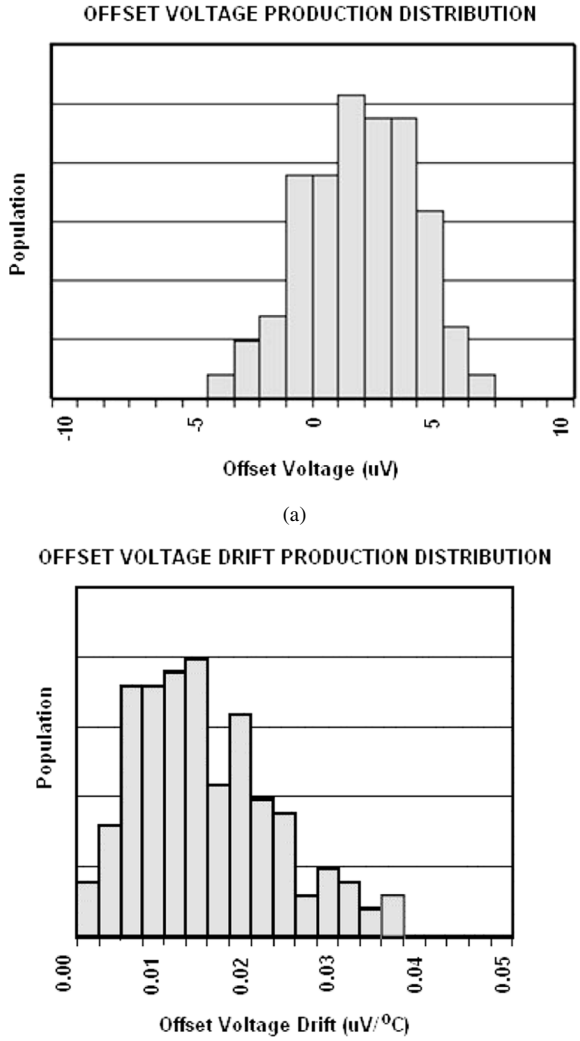

Fig. 10. Production histograms of offset and offset drift.

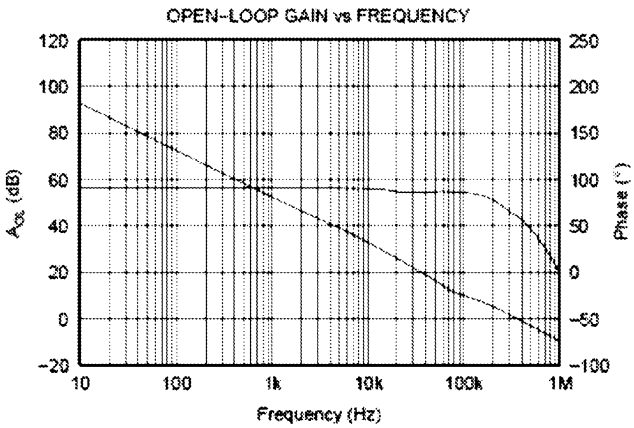

Fig. 11. Open-loop gain and phase.

Silicon measurements of the ripple proved difficult as the low-level ripple is buried well below the total rms noise and not found on an oscilloscope. Spectrum analyzer measurements also

TABLE I
COMPARISION OF CHOPPER AND AUTOZERO OPAMPS

	This work	(2)	(3)	(4)	(5)
Year published / released	2006	2004	2002	2002	2002
Chopping frequency	125kHz			15kHz	200kHz
Autozero frequency		1kHz	10kHz	7.5kHz	
Offset voltage (mean + std)	3uV	1uV	1uV	3uV	4uV
Input bias current	70pA	1pA	70pA	40pA	450pA
Gain Bandwidth, GBW	350kHz	500kHz	2MHz	2.5MHz	5MHz
Input noise, en	55nV/√Hz	85nV/√Hz	55nV/√Hz	20nV/√Hz	6.5nV/√Hz
Supply current, Iq	17uA	140uA	285uA	800uA	1.8mA
en^2 x Iq (nV^2 x mA) Figure of merit	51	1011	862	320	76
GBW/Iq (kHz/uA) Figure of merit	21	4	7	3	3

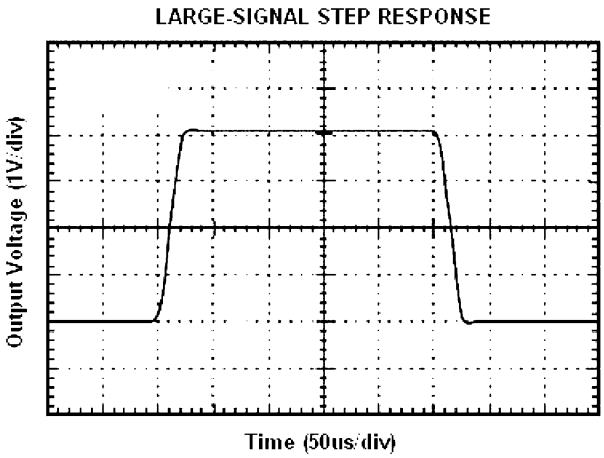

Fig. 12. Large-signal transient response.

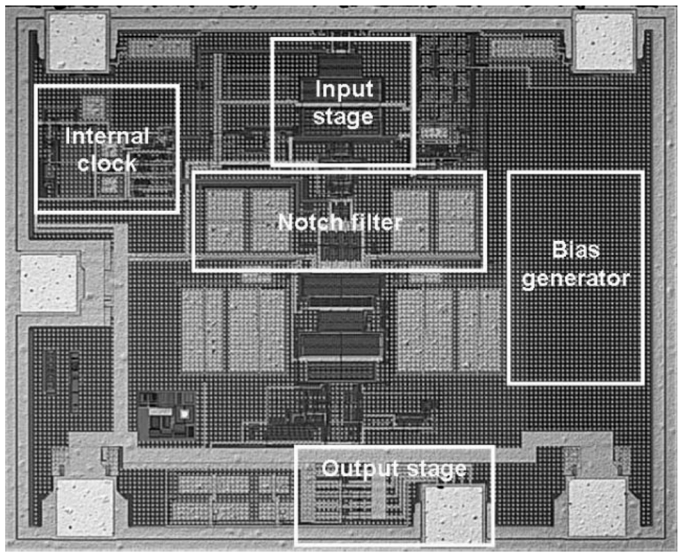

Fig. 13. Chip photograph.

proved to be difficult as readings at the chopping frequency were not visible above the noise floor on units with typical internal offsets. Simulation of ripple such as shown in Fig. 6 was done by inserting internal offsets much higher than those existing in real silicon.

V. CONCLUSION

A micropower chopper-stabilized opamp has been presented. The use of a three-stage amplifier with multipath nested Miller compensation allows modification to incorporate chopping of the input stage, SC filtering to notch out chopping ripple, and a compensation scheme to maintain an undistorted high-speed signal path. The elimination of offset and flicker noise by chopping allows the use of much smaller input devices than practical with a continuous-time amplifier. The die area required makes this design very attractive for use in larger mixed-signal or system-on-chip designs. The topology has application to lower noise and/or larger GBW requirements. The figure of merits for Iq relationships presented for this design are achievable for a wide range of requirements. GBW of up to 5 MHz on similar technology nodes is readily achievable.

The design finds use in many applications requiring amplification of low-level signals from a variety of real-world sensors. These applications often benefit from the elimination of offset, offset temperature drift, flicker noise, and the long-term offset stability provided by chopping.

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