Understanding MOSFET Mismatch for Analog Design

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***Abstract*—Despite the significance of matched devices in analog circuit design, mismatch modeling for design application has been lacking. This paper addresses misconceptions about MOSFET mismatch for analog design. $V_{\rm t}$ mismatch does not follow a simplistic $1/(\sqrt{\rm area})$ law, especially for wide/short and narrow/long devices, which are common geometries in analog circuits. Further, $V_{\rm t}$ and gain factor are not appropriate parameters for modeling mismatch. A physically based mismatch model can be used to obtain dramatic improvements in prediction of mismatch. This model is applied to MOSFET current mirrors to show some nonobvious effects over bias, geometry, and multiple-unit devices.**

***Index Terms*—Analog circuits, mismatch, semiconductor device modeling, SPICE.**

I. Introduction

MISMATCH is the differential performance of two or more devices on a single integrated circuit (IC). It is widely recognized that mismatch is key to precision analog IC design. Historically, mismatch has been treated as an "art" rather than a science, relying on past experience and unproven or uncharacterized effects. Exacerbating the situation is a fundamental lack of modeling and understanding of mismatch over bias and geometry. In an *EE Times* article discussing intradie parameter variations (i.e., mismatch), Nassif stated, "The problem isn't the amount of variability. It's that we tend to turn variability into uncertainty by not modeling it." [1]. Without an accurate mismatch model, designers are forced to include substantial design margin or risk yield loss [2], both of which cost money and time.

Most approaches to mismatch modeling are based on hand analysis of the simple MOSFET drain–current relationship in the saturated region (i.e., $I_d = 0.5\beta(V_{\rm gs} - V_{\rm t})^2$). These models (e.g., [3]–[7]) are based on parametric extensions of [8], but they lack the same fundamental basis. None of these models are applicable in all bias regions. This is a critical requirement of a mismatch model, since matched MOSFETs are used in weak (i.e., low-current low-power design) and strong inversion, in linear and saturated regions, across body bias.

Although these methods are perceived as simple approaches, it has been our experience that the practical implementation is complex. Model inadequacies across geometry and bias create characterization dilemmas, which lead to thick, difficult-to-understand mismatch reports and partitioning of the bias and geometry space into multiple bins or categories. Design application of $V_{\rm t}$, g_m, and $I_{d\rm sat}$ mismatch is not obvious. Additional publications [9]–[11] have focused on the underlying fabrication contributions to mismatch variation, which is useful for technology development, but none of these have satisfactorily described mismatch in a manner relevant to design.

This paper describes a mismatch model that is conducive to design and has been used exclusively at Motorola for the past several years. A key aspect of this model is that the mismatch is characterized in same domain (e.g., I_d) using the same tools (i.e., SPICE) and models (e.g., BSIM) that are used for design. Since SPICE models provide the most accurate and complete description of device electrical behavior as it relates to design, this approach assures that the most appropriate, accurate mismatch prediction is obtained, limited only by the SPICE model and the nature of the collected data.

This paper highlights the physical basis for mismatch. A model is described that is applicable across all bias and geometry conditions, including phenomena such as source/drain series resistance, body bias effects, short-channel/reverse-short-channel effects, narrow-width/inverse-narrow-width effects, mobility degradation, and graded-channel effects. Equally important, this approach is directly intended for design. This model is used in several current-mirror examples to demonstrate some nonobvious effects.

II. Mismatch Model

The basis for mismatch modeling was proposed in [12] and [13]. Here, the notion of local variation was introduced, as Fig. 1 shows. For local variation, the fluctuations in the observed length L depend on the width of the device

$$\sigma_L^2 \propto \frac{1}{W} \tag{1}$$

and likewise for observed width

$$\sigma_W^2 \propto \frac{1}{L}. \tag{2}$$

The local variation of parameters such as sheet resistance, channel dopant concentration, mobility, and gate oxide thickness have an area dependency

$$\sigma_p^2 \propto \frac{1}{LW} \tag{3}$$

where the subscript p represents the process parameter of interest. Physically, the edge variation in (1) and (2) and area dependent variation in (3) result from polysilicon/metal edge grains, photoresist edge roughness, dopant clustering, gate-oxide thickness/permittivity variations, etc. Qualitatively, local variations decrease as the device size increases since the

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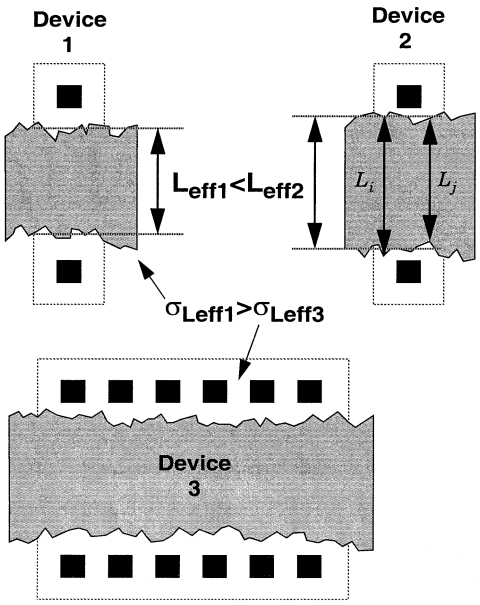

Fig. 1. Global variation and local variation. For local variation, the variance in length depends on the width.

parameters "average" over a greater distance or area. This is contrasted with global process parameter variation which is independent of length L and width W. As per [14], mismatch (i.e., intradie parameter variation) is comprised of local variation but traditional interdie (die-to-die) variation, used for best case and worst case models and statistical simulation, contains both global and local components. In fact, in many instances of technology, device-type, geometry, and bias, the local variation component dominates the interdie variation [15]. This implies an additional geometric dependence that is rarely accounted for in interdie statistical models [16].

The model in (1) was derived by evaluating the local length (e.g., L_i and L_j in Fig. 1) across the entire width and finding the second moment (i.e., the standard deviation) of the effective length. An alternative derivation [8] has been used to describe mismatch behavior over geometry. This model assumes that the observed variation for a given parameter is the convolution of the small-signal parameter spatial variation over the device area. This model is identical to (3). Perimeter contributions to mismatch were not addressed in [8], but a similar derivation results in (1).

Although the model in [8] was derived correctly, it is incorrectly applied to threshold voltage $V_{\rm t}$ and gain factor β. These two parameters are combined to produce the I_d mismatch

$$\sigma^2_{I_d} = \frac{\sigma^2_\beta + 4\sigma^2_{Vt}}{(V_{\rm gs} - V_{\rm t})^2}. \tag{4}$$

One immediately apparent problem is the physical basis for these parameters. As pointed out in [17] and later in [18], if the underlying cause for mismatch variation is the gate-oxide thickness $t_{\rm ox}$, it will be accounted for in both $V_{\rm t}$ and β, thus, σ_{I_d} will be overestimated by a factor as large as two.

For mismatch modeling, one can consider two types of parameters: process and electrical (see Table I). Process parameters are those physically independent parameters that control the electrical behavior of a device. Electrical parameters are those parameters that are of interest to the designer. $V_{\rm t}$ mismatch does not belong in either category.

TABLE I
RELEVANT PROCESS AND ELECTRICAL PARAMETERS

Process Parameters	Electrical Parameters
Flatband Voltage (V_{fb})	Drain current (I_d)
Mobility (μ)	Input voltage (V_{gs})
Substrate Dopant Conc. (N_{sub})	Trans-conductance (g_m)
Length Offset (ΔL)	Output Conductance (g_o)
Width Offset (ΔW)	
Short Channel Effect (V_{tl})	
Narrow Width Effect (V_{tw})	
Gate Oxide Thickness (t_{ox})	
Source/Drain Sheet Resistance (ρ_{sh})	

$V_{\rm t}$ is not a process parameter. $V_{\rm t}$ depends on $V_{\rm fb}$, $t_{\rm ox}$ and $N_{\rm sub}$ (the effective value of which depends on body bias), L through the "short-channel effect" and "reverse-short-channel effect," and W through the "narrow-width" and "inverse-narrow-width effect." In addition, 0.18-μm and smaller technologies use halo or pocket ion implantations which introduce new length and width dependencies. This means that the relationship

$$\sigma_{V_{\rm t}} = \frac{A_{V_{\rm t}}}{\sqrt{LW}} \tag{5}$$

is physically incorrect, and measured data from many technologies confirm this. In [4], the attempt was made to accommodate the otherwise anomalous scaling behavior by using the effective length and width (i.e., $L_{\rm eff} = L - \Delta L$), but this is not appropriate for the same reason that short and narrow channel effects are not modeled with just with ΔL and ΔW. In practice, the geometric scaling inadequacies of (5) are often circumvented by creating local models for geometric subsets of the overall designable geometry space. This approach introduces practical complexities and discontinuities in the model.

$V_{\rm t}$ mismatch is often assumed to be the input offset voltage mismatch $\sigma_{V_{\rm gs}}$ which is an electrical parameter, but

$$\sigma_{V_{\rm gs}} = \frac{\sigma_{I_d}}{g_m}. \tag{6}$$

Even using the simplistic mismatch relationship in (4), it is apparent that $\sigma_{V_{\rm t}}$ is not the input offset voltage, because neither σ_{I_d} nor g_m is constant over bias, especially for graded-channel devices such as the halo-implanted device, yet $\sigma_{V_{\rm t}}$ is. The consequences of this distinction will be made apparent in Section III.

Inadequate geometry selection in the mismatch test structure design of experiments hides the shortcomings of (5). Several different gate areas are used to extract the $A_{V_{\rm t}}$. Barring any other considerations, often these geometries are selected about $L = W$. This establishes a self-fulfilling situation in which an erroneous model appears to fit the data well. Departures in the true mismatch behavior from the assumed model cannot be detected and evaluated. Large model prediction errors result for wide/short and narrow/long MOSFETs. These geometries are critical to analog design.

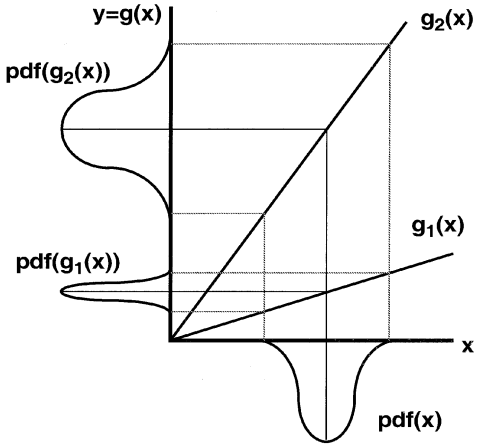

Fig. 2. Graphical depiction of the propagation of variance.

A physically complete and accurate mismatch model is given in [18] for MOSFETs and [19] for bipolar junction transistors (BJTs). All mismatch models are based on the propagation of variance (POV) relationship depicted in Fig. 2. For a given independent variable x and a dependent variable $y = g(x)$

$$\Delta y = \frac{\partial y}{\partial x}(\Delta x). \tag{7}$$

Considering the range of possible values of Δx as described by the probability density function (pdf) of x and building a pdf(y) yields the POV relationship

$$\sigma_e^2 = \sum_i \left(\frac{\partial e}{\partial p_i}\right)^2 \sigma_{p_i}^2 \tag{8}$$

where e is any electrical parameter and p_i is the ith independent process parameter, listed in Table I. In the case of MOSFETs, normal distributions are assumed. For BJT mismatch models, log-normal distributions are required for some parameters, but that is outside the scope of this paper. For MOS mismatch models other than [18], the partial derivatives in (8) are based on the simplistic I_d model

$$I_d = 0.5\beta\,(V_{\rm gs} - V_{\rm t})^2 \tag{9}$$

or extensions of (9), with $V_{\rm t}$ and β as process parameters, and I_d as the electrical parameter. Combining (9) and (8) yields (4).

The mismatch model in [18] is more complete since it uses BSIM3 (or another SPICE MOSFET model) to evaluate the partial derivative in (8), which is substantially more accurate than using a simple analytic model like (9). Unlike the mismatch model in (4), [18] is valid in the linear and saturation regions, for subthreshold, weak inversion, and strong inversion conditions, and for all geometries, as shown in the plots of measured and simulated data for nMOS transistors in Fig. 3. A partial comparison of the modeling approaches is given across bias in Fig. 4 and across geometry in Fig. 5, for a nMOS device in a 0.25-μm CMOS technology. It is worth noting that the comparison of models in Figs. 4 and 5 are given for large gate voltages (1.8 and 2.5 V). As the gate voltage decreases, the departure in modeling approaches increases. Clearly, there is a significant improvement of the model [18] over the standard approach, (4) and (5). A detailed discussion of the characteristics of these plots is given in [18].

Applying (8) to MOSFET mismatch produces

$$\sigma_e^2 = \sum_i \left(\frac{\partial e}{\partial p_i}\right)^2 \sigma_{p_i}^2(\text{geometry}) \tag{10}$$

where the geometric dependency of the process parameter variation is given in (1)–(3). Expanding (10) gives

$$\begin{bmatrix} \sigma^2_{\tilde{I}_{d1}} \\ \sigma^2_{\tilde{I}_{d2}} \\ \sigma^2_{\tilde{I}_{d3}} \\ \cdots \\ \sigma^2_{\tilde{I}_{dn}} \end{bmatrix} = \begin{bmatrix} \left(\frac{d\tilde{I}_{d1}}{d\Delta_W}\right)^2 & \left(\frac{d\tilde{I}_{d1}}{d\tilde{t}_{\rm ox}}\right)^2 & \left(\frac{d\tilde{I}_{d1}}{dV_{\rm fb}}\right)^2 & \left(\frac{d\tilde{I}_{d1}}{d\tilde{\mu}_o}\right)^2 & \left(\frac{d\tilde{I}_{d1}}{d\Delta_L}\right)^2 & \left(\frac{d\tilde{I}_{d1}}{dV_{\rm tL}}\right)^2 & \left(\frac{d\tilde{I}_{d1}}{d\tilde{\rho}_{\rm sh}}\right)^2 & \left(\frac{d\tilde{I}_{d1}}{d\tilde{N}_{\rm sub}}\right)^2 \\ \left(\frac{d\tilde{I}_{d2}}{d\Delta_W}\right)^2 & \left(\frac{d\tilde{I}_{d2}}{d\tilde{t}_{\rm ox}}\right)^2 & \left(\frac{d\tilde{I}_{d2}}{dV_{\rm fb}}\right)^2 & \left(\frac{d\tilde{I}_{d2}}{d\tilde{\mu}_o}\right)^2 & \left(\frac{d\tilde{I}_{d2}}{d\Delta_L}\right)^2 & \left(\frac{d\tilde{I}_{d2}}{dV_{\rm tL}}\right)^2 & \left(\frac{d\tilde{I}_{d1}}{d\tilde{\rho}_{\rm sh}}\right)^2 & \left(\frac{d\tilde{I}_{d1}}{d\tilde{N}_{\rm sub}}\right)^2 \\ \left(\frac{d\tilde{I}_{d3}}{d\Delta_W}\right)^2 & \left(\frac{d\tilde{I}_{d3}}{d\tilde{t}_{\rm ox}}\right)^2 & \left(\frac{d\tilde{I}_{d3}}{dV_{\rm fb}}\right)^2 & \left(\frac{d\tilde{I}_{d3}}{d\tilde{\mu}_o}\right)^2 & \left(\frac{d\tilde{I}_{d3}}{d\Delta_L}\right)^2 & \left(\frac{d\tilde{I}_{d3}}{dV_{\rm tL}}\right)^2 & \left(\frac{d\tilde{I}_{d1}}{d\tilde{\rho}_{\rm sh}}\right)^2 & \left(\frac{d\tilde{I}_{d1}}{d\tilde{N}_{\rm sub}}\right)^2 \\ \cdots & \cdots & \cdots & \cdots & \cdots & \cdots & \cdots & \cdots \\ \left(\frac{d\tilde{I}_{dn}}{d\Delta_W}\right)^2 & \left(\frac{d\tilde{I}_{dn}}{d\tilde{t}_{\rm ox}}\right)^2 & \left(\frac{d\tilde{I}_{dn}}{dV_{\rm fb}}\right)^2 & \left(\frac{d\tilde{I}_{dn}}{d\tilde{\mu}_o}\right)^2 & \left(\frac{d\tilde{I}_{dn}}{d\Delta_L}\right)^2 & \left(\frac{d\tilde{I}_{dn}}{dV_{\rm tL}}\right)^2 & \left(\frac{d\tilde{I}_{dn}}{d\tilde{\rho}_{\rm sh}}\right)^2 & \left(\frac{d\tilde{I}_{dn}}{d\tilde{N}_{\rm sub}}\right)^2 \end{bmatrix} \begin{bmatrix} \sigma^2_{\Delta_W}/L \\ \sigma^2_{\tilde{t}_{\rm ox}}/(LW) \\ \sigma^2_{V_{\rm fb}}/(LW) \\ \sigma^2_{\tilde{\mu}_o}/(LW) \\ \sigma^2_{\Delta_L}/W \\ \sigma^2_{V_{\rm tL}}/W \\ \sigma^2_{\tilde{\rho}_{\rm sh}}/(LW) \\ \sigma^2_{\tilde{N}_{\rm sub}}/(LW) \end{bmatrix}. \tag{11}$$

The tilde $(\sim)$ above a variable indicates a normalized parameter. For characterization, the vector on the left side of (11) is a set of n I_d mismatch standard deviations collected across many dies for many biases and geometries, typically hundreds of combinations. The combinations are chosen so that the process parameter mismatch variances are observable in the I_d mismatch data, with a unique and unconfounded solution. For instance, $\rho_{\rm sh}$ only significantly affects I_d for short devices in the linear region for high $V_{\rm gs}$, so we measure mismatch under these conditions. Conversely, $\rho_{\rm sh}$ cannot be considered in mismatch characterization schemes that contain $V_{\rm t}$, β, and/or $I_{d\rm sat}$ mismatch measurements, because it is not reflected in those parameters. This is a likely explanation of the results obtained in [22].

The large middle matrix in (11) contains the squares of the sensitivities of I_d with respect to each of the process parameters. Each row of sensitivities is numerically evaluated using SPICE at the bias and geometry conditions at which the corresponding σ_{I_d} is measured. Hence, the bias conditions and geometries for the measured devices must be chosen to ensure that each process parameter can be uniquely observed above the measurement error.

Given the first two matrices in (11), the rightmost vector of process parameters can be calculated using analytic simple linear regression. This method is called back propagation of variance (BPV). Essentially, process parameter variations are extracted that best explain the measured σ_{I_d} over bias and geometry. Each process parameter is assumed to be independent. If a correlation exists between process parameters, that is an indication that a wrong or incomplete set of process parameters has been selected. Correlations can always be addressed with the inclusion of the appropriate set of independent process parameters. For instance, $V_{\rm t}$ and β (or g_m) mismatch are partially correlated, depending on the relative contribution of

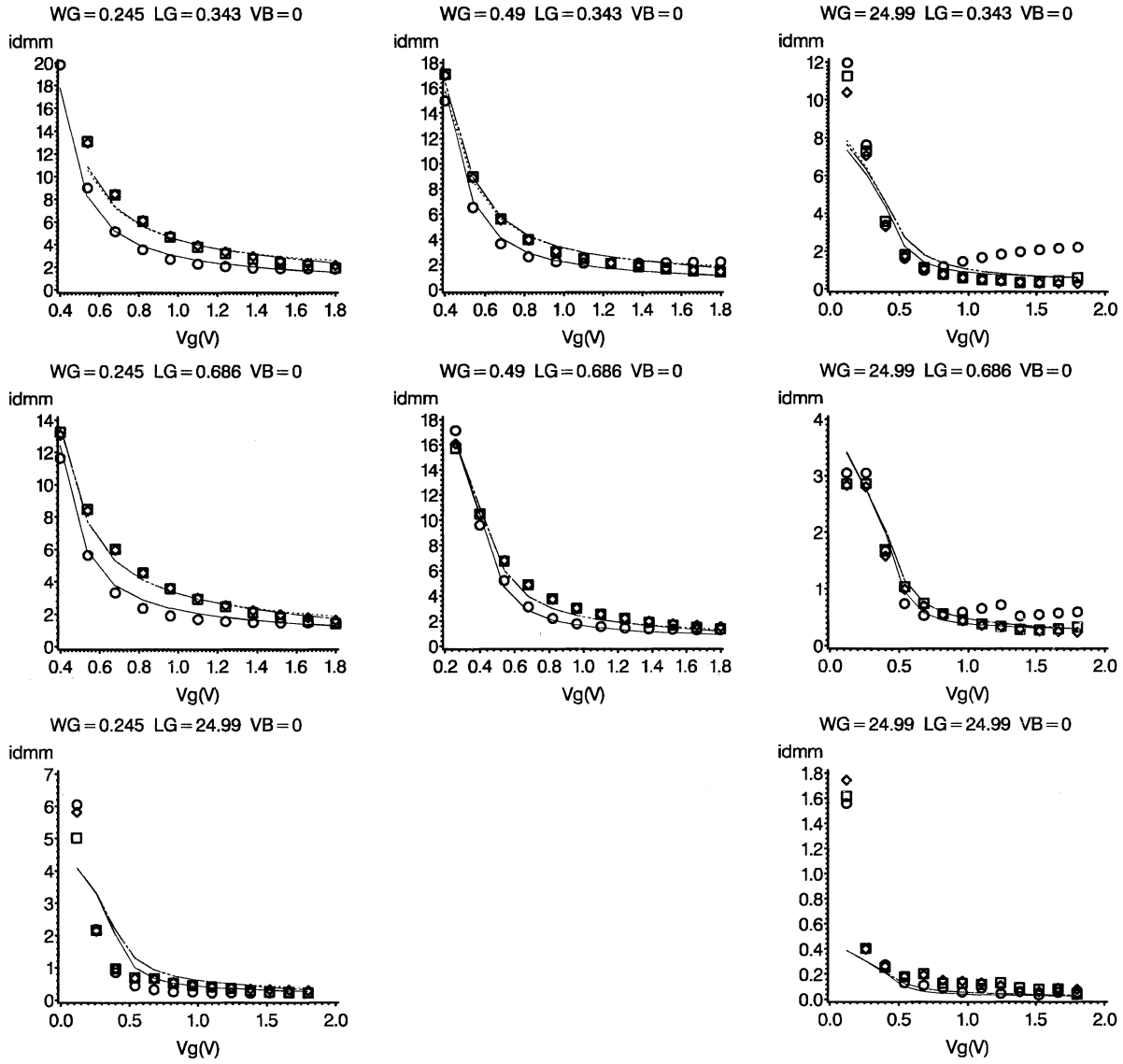

Fig. 3. Array of plots of measured and simulated mismatch data for an nMOS device on a 0.18-μm technology [20]. The geometry selection is based upon the design of experiments in [21]. Circle, square, and diamond symbols are measured data at $V_d = 0.1$ V, 0.9 V, and 1.8 V, respectively. Lines are model at the same conditions.

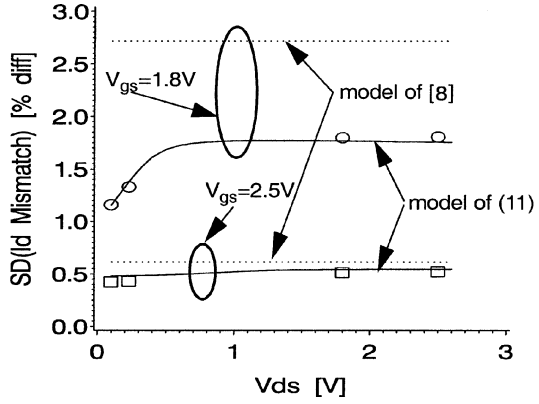

Fig. 4. NMOS I_d mismatch over bias, 0.25-μm CMOS technology, $W/L = 7/0.56$ μm $= -2.5$ V. Symbols are data.

t_{ox}. An appropriate reparameterization of V_t and β mismatch would use V_{fb}, N_{sub}, μ, and t_{ox}. BPV should not be confused with principle component analysis (PCA), which is strictly empirical with no physical basis or interpretation.

Note that the process parameters in the right-side vector of (11) contain the local variation geometric scaling as prescribed by (1)–(3). This means that geometric scaling is applied to both the variance and the sensitivity components on the right side of (8). The geometric scaling affects the sensitivities through the underlying SPICE MOSFET model.

III. Mismatch Application

An accurate mismatch model is not useful unless it can be practically used for design. The specific intention of the characterization approach described here is its application in SPICE through Monte Carlo or sensitivity analysis. We use MOSFET current mirrors to illustrate some nonobvious mismatch phenomena. Similar analysis can be used for other applications such as differential pairs and much larger circuit blocks.

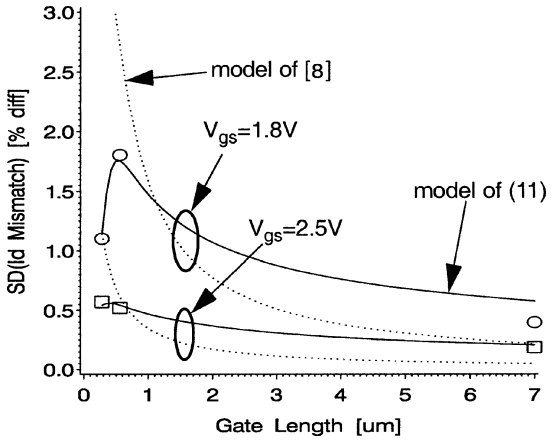

Fig. 5. NMOS I_d mismatch versus L, 0.25-μm CMOS technology, W=7 μm, $V_{\rm ds} = 2.5$, V $= -2.5$ V. Symbols are data.

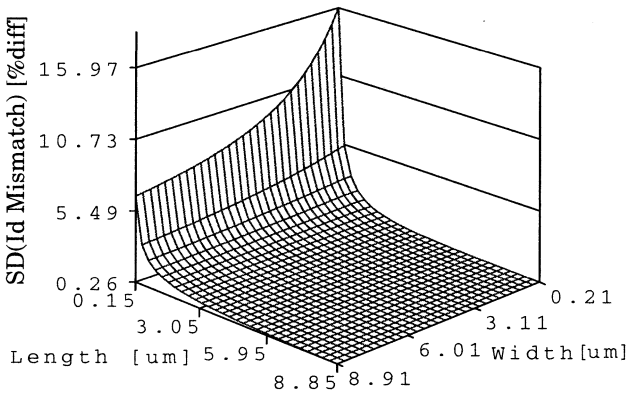

Fig. 6. Three-dimensional (3-D) plot of I_d mismatch versus L and W for an nMOS current mirror, $I_{\rm ref} = 10\ \mu$A, 0.13-μm CMOS technology.

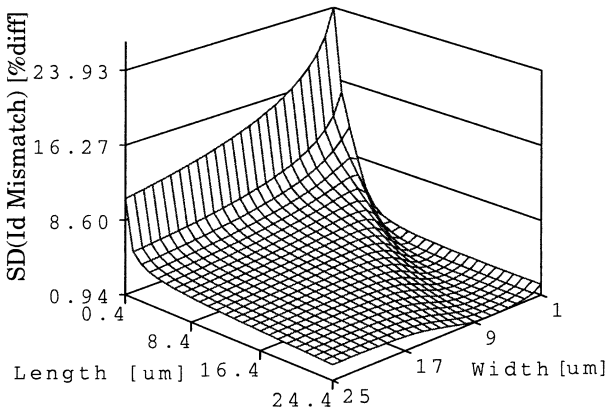

Fig. 7. 3-D plot of I_d mismatch versus geometry, graded-channel nMOS, at $I_{\rm ref} = 10\ \mu$A, 0.25-μm BiCMOS technology.

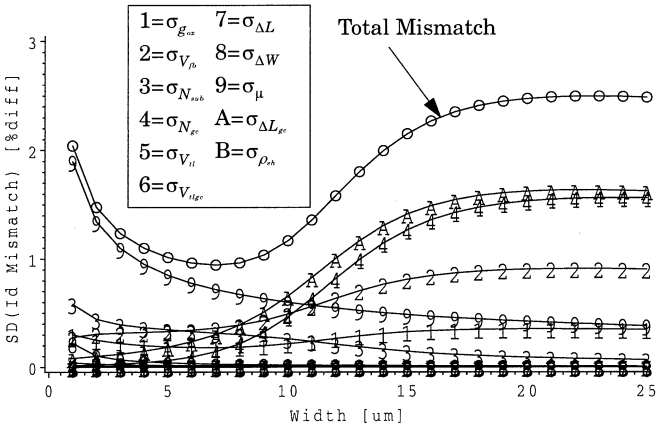

Fig. 8. I_d mismatch and the underlying process parameter contributions for $L = 25\ \mu$m in Fig. 7. "gc" subscript indicates parameters specific to the graded channel.

A. Geometry and Bias Interrelationship

What is the best way to size devices in a current mirror to meet matching requirements? A MOSFET current mirror is biased with a current, so the gate voltage depends on geometry. Intuitively, as the gate overdrive voltage $V_{\rm od} = V_{\rm gs} - V_{\rm t}$ increases, those parameters that effect $V_{\rm t}$ have less impact on the I_d mismatch. This is even apparent in (4).

As L increases, the intrinsic mismatch decreases as per (1)–(3). At the same time, $V_{\rm od}$ increases to supply the same reference current. Both the sensitivity local parameter components in (8) also decrease, constructively combining to decrease σ_{I_d}.

However, as W increases, the intrinsic mismatch component decreases, but $V_{\rm od}$ decreases. These two effects offset each other, and as Fig. 6 shows, can give rise to little or no improvement in mismatch with increasing W. Depending on the underlying dominant mismatch process parameters, better matching can be obtained without consuming additional area, simply by changing the W/L aspect ratio. This improvement comes at the expense of reduced dynamic range since $V_{\rm od}$ increases and, hence, the linear/saturation transition point for $V_{\rm ds}$ (i.e., $V_{d\rm sat}$) increases.

For graded-channel MOSFETs [23] (and halo-implanted devices), the geometry and bias tradeoff can have a much more profound impact, as Fig. 7 shows. Here, a dramatic improvement in mismatch is obtained with small W/L ratios. To further explore this, a cut along $L = 25\ \mu$m in Fig. 7 is given in Fig. 8. For wider devices, the mismatch is dominated by the dopant concentration and the length of the graded-channel region. Since the channel dopant concentration is highest in the graded-channel region (versus the bulk dopant concentration), this region effectively sets the threshold voltage of the device. As the device narrows, $V_{\rm od}$ increases, thereby reducing the sensitivity of I_d to the graded-channel components. Of particular interest is that the geometric dependency of μ is determined by the local process parameter definition, but the geometric dependency of the graded-channel regions is determined by the sensitivity component of (10) and (11). Mismatch does not blindly depend on area alone. The impact of $V_{\rm od}$ on mismatch also means that mismatch is not constant if the reference current is not constant, such as in an active load (see Fig. 9).

Thus, current mirror mismatch depends strongly on L and not W. Proper sizing of MOSFETs in current mirrors requires a mismatch model that is accurate over both bias and geometry.

B. NMOS or PMOS?

A common question is, "Which matches better, nMOS or pMOS?" The answer depends on how a device is biased. With voltage bias, there is no consistent trend across technologies. With current bias, the lower mobility for pMOS means that

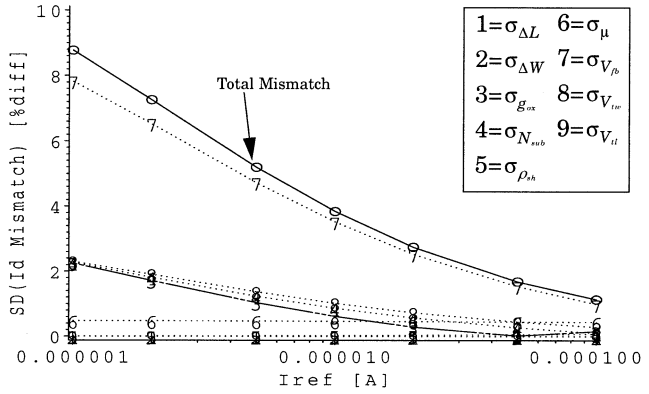

Fig. 9. Current mirror I_d mismatch versus $I_{\rm ref}$, $W/L = 2/2$ μm, 0.13-μm CMOS technology.

TABLE II
MISMATCH FOR 2×2 μm^2 nMOS AND pMOS DEVICES ON A 0.4-μm-POWER BiCMOS PROCESS

Bias Condition	Device	V_{gs} [V]	SD(Id Mismatch) [%diff]
Current Mirror Iref=10μA	nMOS	1.09	1.22%
	pMOS	1.70	1.09%
Voltage Driven Vgs=1.70V	nMOS		0.589%
	pMOS		1.09%

a larger $V_{\rm od}$ is required to supply the same reference or tail current, thereby improving the mismatch as compared with an nMOS device. Table II shows this effect for complementary standard-logic nMOS and pMOS devices in a 0.4-μm-power BiCMOS process. In almost all cases, complementary pMOS devices will appear to have better matching than nMOS when biased with current. More generally, mismatch tradeoffs appear differently to characterization and device engineers (who typically bias devices with voltages) than to design engineers (who often bias devices with current). Metrics such as $V_{\rm t}$ mismatch may not be particularly meaningful. Device-type, geometry, and bias comparisons for mismatch must be performed in the design application.

C. Multiple-Unit Devices

Wide/short MOSFETs are often used in design, particularly in differential pair applications where a high g_m is needed. These devices are broken up into smaller unit MOSFETs and combined to compact the layout and to reduce parasitic source and drain junction capacitances. When multiple-unit devices are placed in parallel, the process parameter variance component in (10) increases by a factor of n, because each MOSFET contains its own local parameter variation. On the other hand, the squared sensitivities decrease by a factor of n^2, because each device has less impact of the current. Thus, overall σ_{I_d} decreases by a factor of $\sqrt{n}$, per (10). This is consistent with the definition of local parameter variation. For example, an 80-μm-wide device can be broken up into 4×20-μm-wide devices. Neglecting width effects, the mismatch variability for a single 20-μm-wide device will be twice the variability of the 80-μm-wide device per (1) and (3), which is the same as dividing the 20-μm device mismatch by $\sqrt{4}$. This consistency is an important consideration when selecting the geometric dependency in the rightmost vector in (11).

TABLE III
IMPACT OF MULTIPLE UNIT DEVICES ON CURRENT MIRROR MISMATCH FOR A 2×2 μm^2 nMOS DEVICE ON A 0.13-μm CMOS PROCESS. $I_{\rm REF}$ IS SCALED FOR THE REFERENCE DEVICE TO MAINTAIN CONSTANT VOLTAGE BIAS

# in parallel reference device	# in parallel output device	SD(Id Mismatch) [%diff]
1	1	3.86
1	4	1.52%
4	1	3.05%
4	4	1.41%

Where integer current scaling is desired, the matching of a $1:n$ ratio differs from an $n:1$ ratio. If n devices are placed in parallel, each device contributes additional mismatch variance. The situation for current mirrors is slightly different, because multiple-unit devices in the reference transistor are mapped through the gate voltage. As Table III shows, the majority of the improvement from using multiple parallel devices is gained by using them for the output, not the reference device.

IV. CONCLUSION

Accurate mismatch modeling is needed to avoid parametric yield loss and overdesign. The common approach to MOSFET mismatch modeling, based on $V_{\rm t}$ and β, leads to inaccurate predictions over geometry and bias. Mismatch modeling based on physical process parameters is significantly more accurate.

In addition, because the approach is based on physical uncorrelated process parameters, the characterization procedure identifies the parameters that have the greatest contribution to mismatch. This helps process technologists identify key areas to work on when trying to optimize a process for best mismatch.

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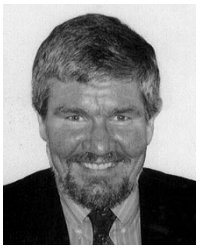

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