## 10.6 A 10μs Fast Switching PLL Synthesizer for a GSM/EDGE Base-Station

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GSM & EDGE base-stations require synthesizers that can frequency hop over the full 75MHz TX or RX band in < 10us and also have very low phase noise and spurious. To date, these conflicting requirements can only be accomplished using a costly "ping-pong" architecture where one synthesizer is locking to the next desired frequency while the other is active as the LO. The proposed fast switching synthesizer can meet all these requirements with a single PLL.

A common approach to reducing PLL lock time is to increase the charge pump current ($I_{CP}$) by a factor of N, while reducing the loop filter zero-resistor by sqrt(N). This increases the BW by sqrt(N) while leaving the phase margin unchanged [1]. The disadvantage of this approach is that the loop settles slowly from the phase disturbance that inevitably results when switching back to the narrow BW mode. In this paper, we describe several techniques that ensure this disturbance is no greater than the +/- 5 degree limits that are acceptable for EDGE, thus allowing us to fully take advantage of the wide BW mode.

During fast lock, 64 identical 0.25mA charge pump cells are enabled for an 8x increase in the loop BW. The NMOS switches of Fig. 10.6.1 are also closed to effect an 8x reduction in the loop filter zero-resistor. After 10us, the frequency has settled to the new value. The TX power amplifier in the base-station can begin to ramp up and has an additional 10us to reach the desired TX power level for EDGE before the start of the TX data burst. This additional 10us is utilized in the chip to reduce the loop BW back to 40kHz before the start of the TX data burst.

Any change in the up-to-down current mismatch between the 64x and 1x modes of the charge pump will provoke a step change in the phase response of the PLL. A mismatch change of just 0.35%, with a 2ns minimum PFD pulse, will cause a 7ps phase step at the PFD inputs [2], which represents 5 degrees at a 2GHz RF output. Timing mismatch between the up and down signal paths from the PFD to the charge pump has a similar effect [2].

The strategy used here is to minimize the actual mismatch at both 64x and 1x $I_{CP}$, and hence, by definition, the change in mismatch will be minimised. For best matching, a fully differential charge pump architecture is used [2]. In addition, the complete up-to-down paths from the PFD inputs to the charge pump outputs are chopped at $f_{REF}/2$ to dynamically remove any residual mismatch due to process variations and timing mismatch.

Fig. 10.6.2 shows a simplified diagram of the charge pump cell, which is replicated 64 times on the layout. During wide BW mode, all 64 cells are active. Under the control of the PFD, only one cell is active in narrow BW mode; the currents of the other 63 are steered to a ~2V low impedance bias.

After the 10us it takes to lock the PLL in wide BW mode, gating logic between the UP and DN signals from the PFD and the 64 charge pump cells is used to reduce $I_{CP}$ from 64x to 1x in 6 binary steps with 4 reference cycles between each step. The zero-resistor switches are then opened. A ref cycle ahead of each binary step, the state of the digital sigma-delta modulator (SDM) is scaled to "trick" the PFD into producing a 2x wider than normal output pulse, which compensates to a first order for the binary step reduction in $I_{CP}$. This scaling involves doubling the contents of the 2nd and 3rd integrators in the 3rd order SDM. The SDM responds to this quickly, resulting in a 2x larger than normal output code on the next ref cycle.

The charge pump cell is similar to other differential charge pump architectures using the current steering technique [3]. Switches are used to steer the PMOS as well as NMOS currents to ensure that the outputs are truly switched off during the tri-state period. During the pump-up period, current is sourced out to the loop filter connected to CPO and sinks from the loop filter on CPOB, causing the (CPO, CPOB) differential voltage to increase. Similarly an active pump-down signal will cause the differential output voltage to decrease.

Symmetrical layout is used in the cell and critical current source transistor pairs mp1, mp2 and also mn1, mn2 are each inter-digitated to minimize up-to-down current mismatch. Chopping the outputs is implemented in the gating logic to control the appropriate charge pump switches of Fig. 10.6.2. The transmission gates at the PFD inputs in Fig. 10.6.1 are activated with the indicated chopping phase. Cascode devices are used on the switches of Fig. 10.6.2 to minimise variation in response time and charge injection versus charge pump output voltage [4]. Additional cascode devices are used on the current sources to increase their output impedance for minimal up or down current variation over the desired charge pump output range.

The VCO and passive loop filter, shown in Fig. 10.6.1, are external to the chip for maximum flexibility. The chip will accept RF input signals from 500MHz to 3GHz which more than adequately spans the range of TX and RX VCO frequencies required from GSM850 up to PCS1900, taking into account possible IF frequencies. For a given VCO gain, $K_V$, and $I_{CP}$ = 0.25mA, the zero-resistor value, $R_2$ is chosen using the loop BW formula, $R_2K_VI_{CP}f_{REF}/(2\pi RF) = 40kHz$. The values of $C_1$ and $C_2$ are then chosen to set the pole and zero frequencies at approximately 2.5x and 0.4x of the 40kHz loop bandwidth.

A low noise differential amplifier is used to convert the differential charge pump output into a single-ended control signal for an external low noise VCO, as shown in Fig. 10.6.1. The input buffers comprise a PMOS source follower for zero input current and are sized for low 1/f noise, followed by an NPN emitter follower for level shift and low output impedance. The op-amp is an NPN input, single stage folded cascode design for low noise and fast settling.

A common-mode feedback (CMFB) loop, Fig. 10.6.3, senses the charge pump output common-mode voltage compared to a desired ~2V common-mode reference and adjusts the width of both UP and DN pulses to the PMOS current switches relative to the widths to the NMOS current switches. Since both UP and DN pulse widths are adjusted together by the same amount, the CMFB loop acts independently of the PFD. Noise from the CMFB circuitry is common mode to the PFD and has little impact on the output phase noise.

Figure 10.6.4 shows the tuning voltage and phase settling response for a 75MHz jump across the DCS1800 TX band. Figure 10.6.5 is a plot of the synthesizer's phase noise at 1860MHz with a 26MHz reference and chopping at 13MHz. Figure 10.6.6 summarizes measured performance.

*References:*

[1] Crowley, "Phase Locked Loop with Variable Gain and Bandwidth," US Patent 4,156,855.
[2] Rhee, "Design of High Performance CMOS Charge Pumps in Phase-Locked Loops," *IEEE International Symposium on Circuits and Systems*, 1999.
[3] Y. M. Greshishchev and P. Schvan, "SiGe Clock and Data Recovery IC with Linear-Type PLL for 10-Gb/s SONET Application," *IEEE J. Solid-State Circuits*, vol. 35, no. 9, pp. 1353-1359, Sept. 2000.
[4] J. Bastos et al., "A 12-Bit Intrinsic Accuracy High-Speed CMOS DAC," *IEEE J. Solid-State Circuits*, vol. 33, no. 12, pp. 1959-1969, Dec. 1998.

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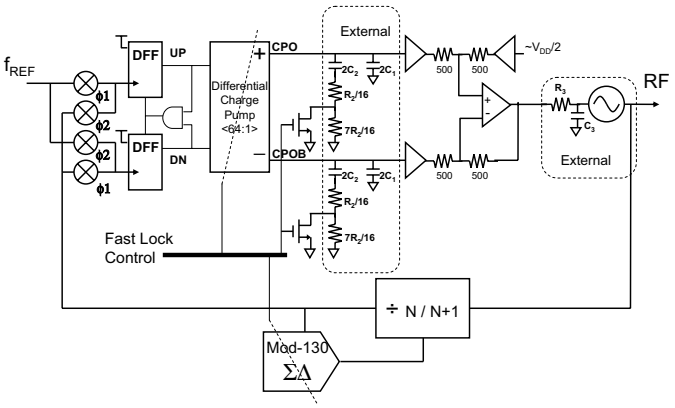



Figure 10.6.1: Fast lock PLL with PFD inputs chopped.

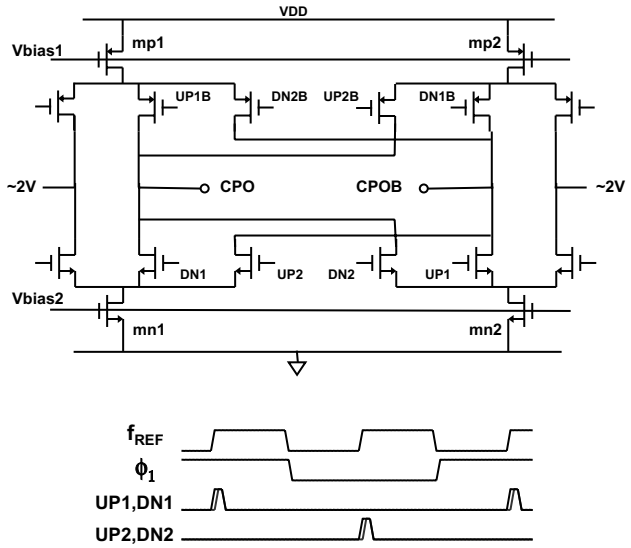



Figure 10.6.2: Differential charge pump cell with chopped outputs.

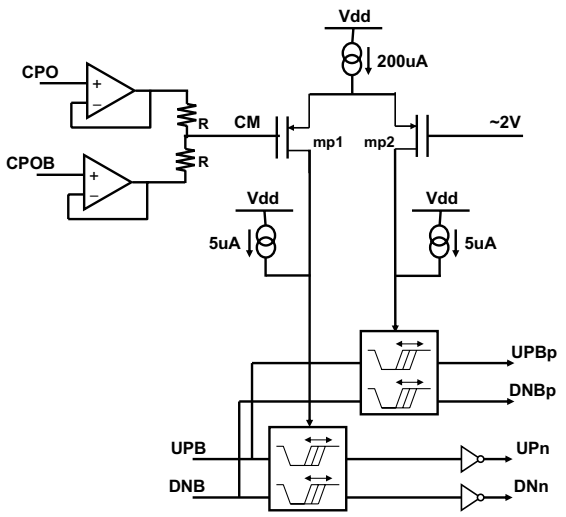



Figure 10.6.3: Pulse stretching common-mode feedback loop.

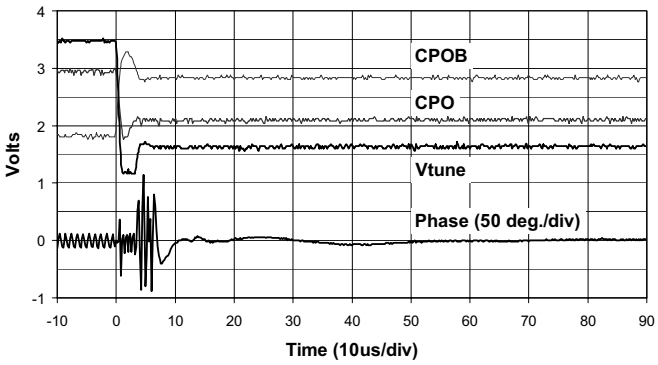



Figure 10.6.4: Settling time plot for a 75MHz jump from 1880 to 1805MHz.

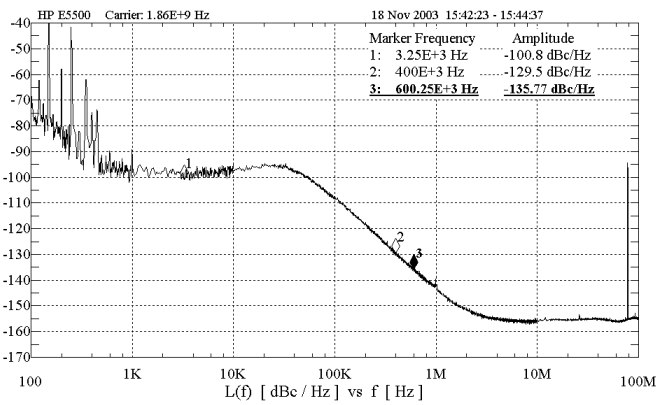



Figure 10.6.5: SSB phase noise plot at 1860MHz with chipping active.

| | |
|---|---|
| Settling Time | 10 us |
| RMS Phase Error | 0.22 deg. |
| RF Input Range (-15 to 0dBm) | 0.5 – 3 GHz |
| Idd: Charge Pump (5V) | 33mA |
| Diff-amp (5V) | 30mA |
| Remainder of chip (3V) | 20mA |
| Worse Case Spurs (with 26MHz Fref and chopping at Fref/2) | -65 dBc @ 200kHz<br>-75 dBc @ 400kHz<br>-85 dBc @ 600kHz<br>-95 dBc @ 13MHz<br>-95 dBc @ 26MHz |
| Chip Size | 2.29 x 2.32 mm |
| Technology | 0.35u BiCMOS with 5V options |
| Package | 5x5mm 32 lead LFCSP |

Figure 10.6.6: Performance summary.

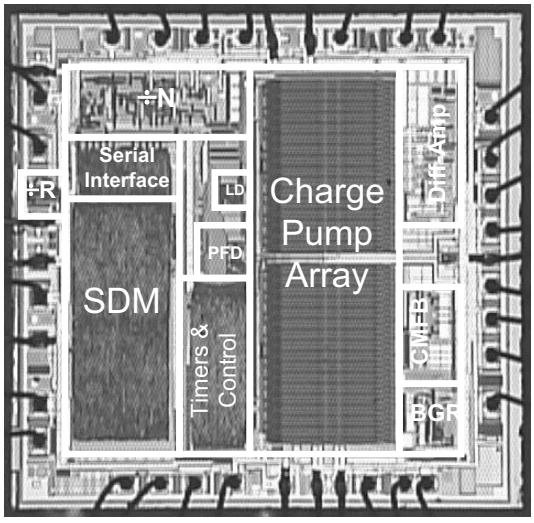



**Figure 10.6.7: Die photo.**

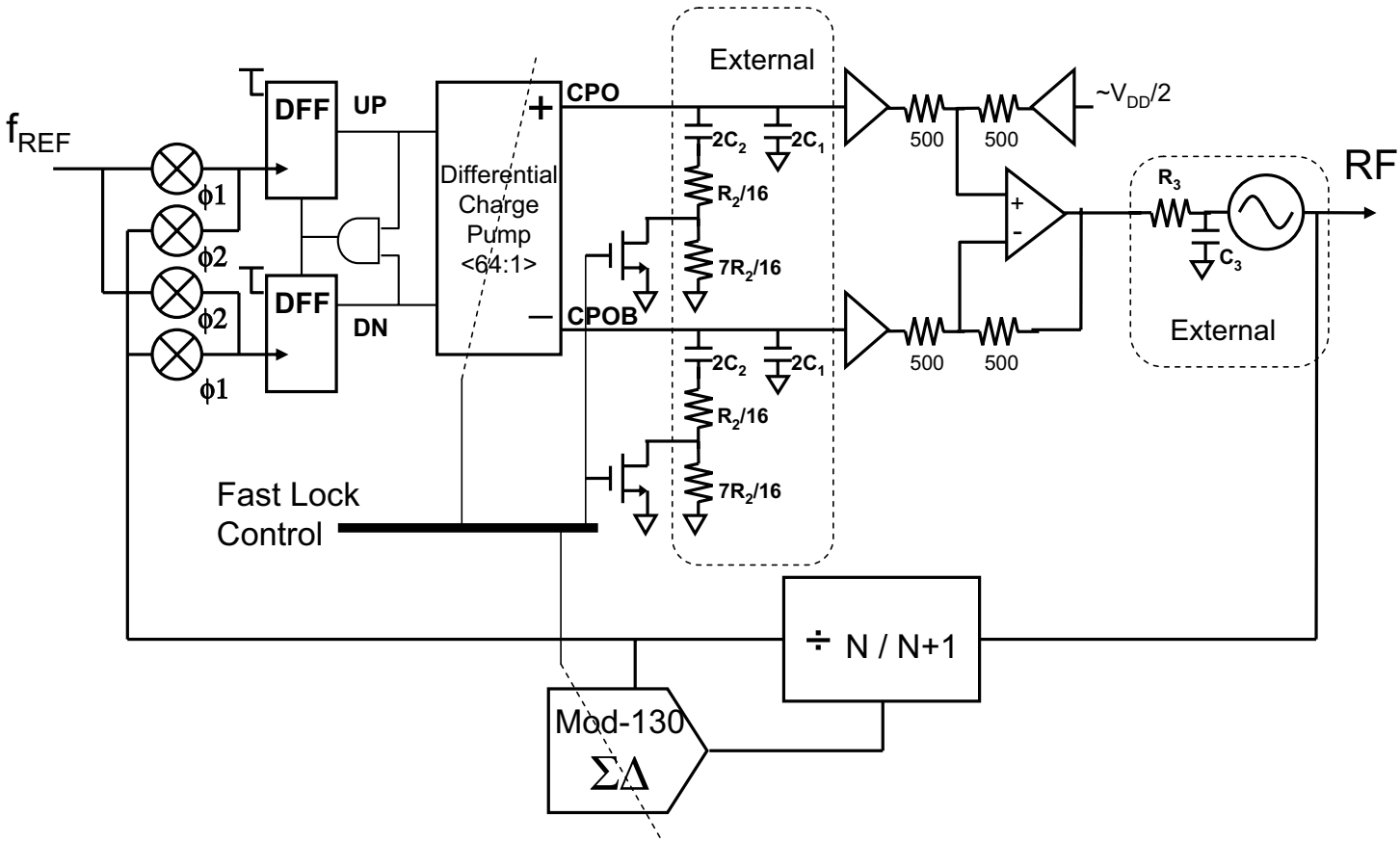
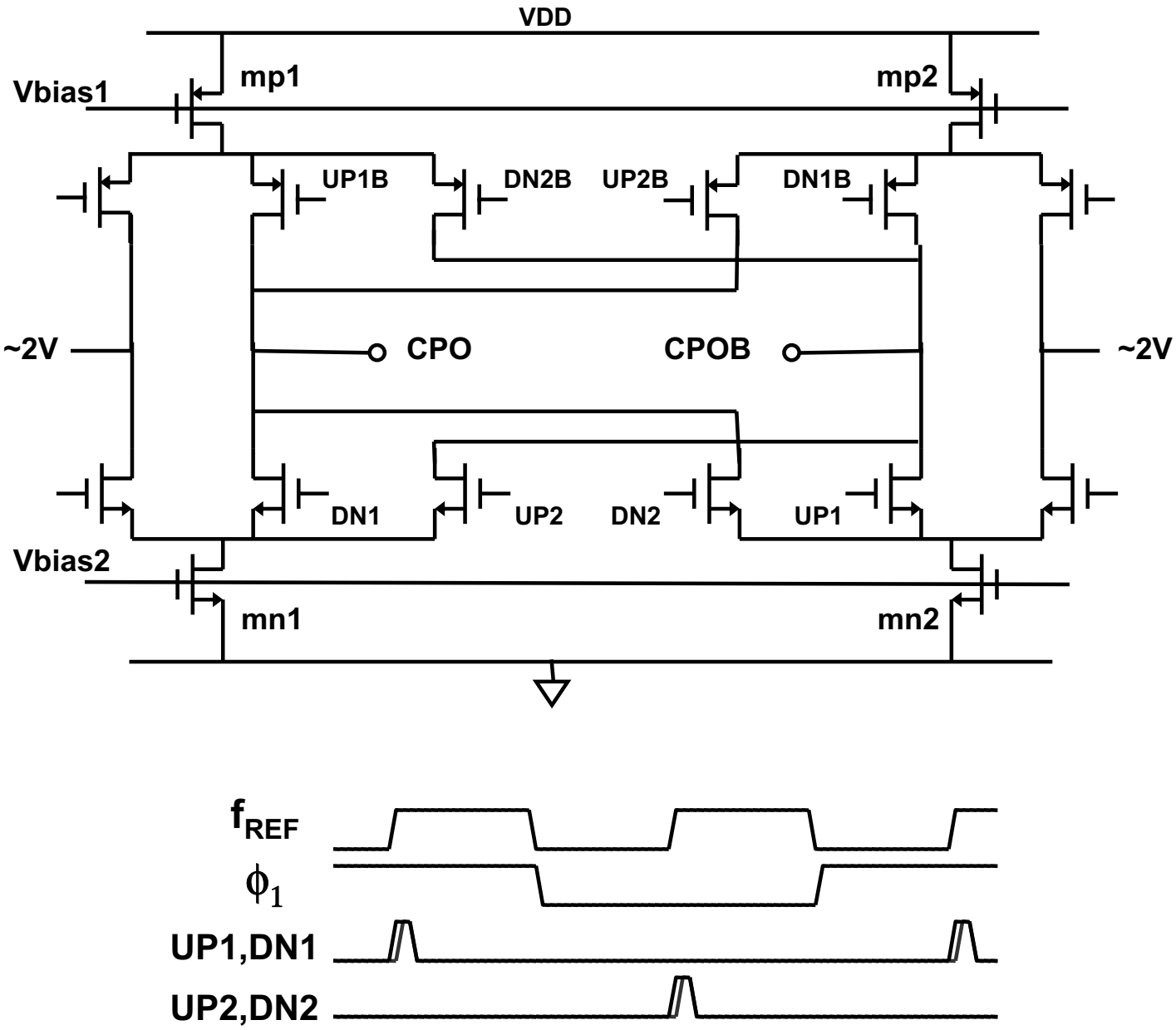



**Figure 10.6.1: Fast lock PLL with PFD inputs chopped.**

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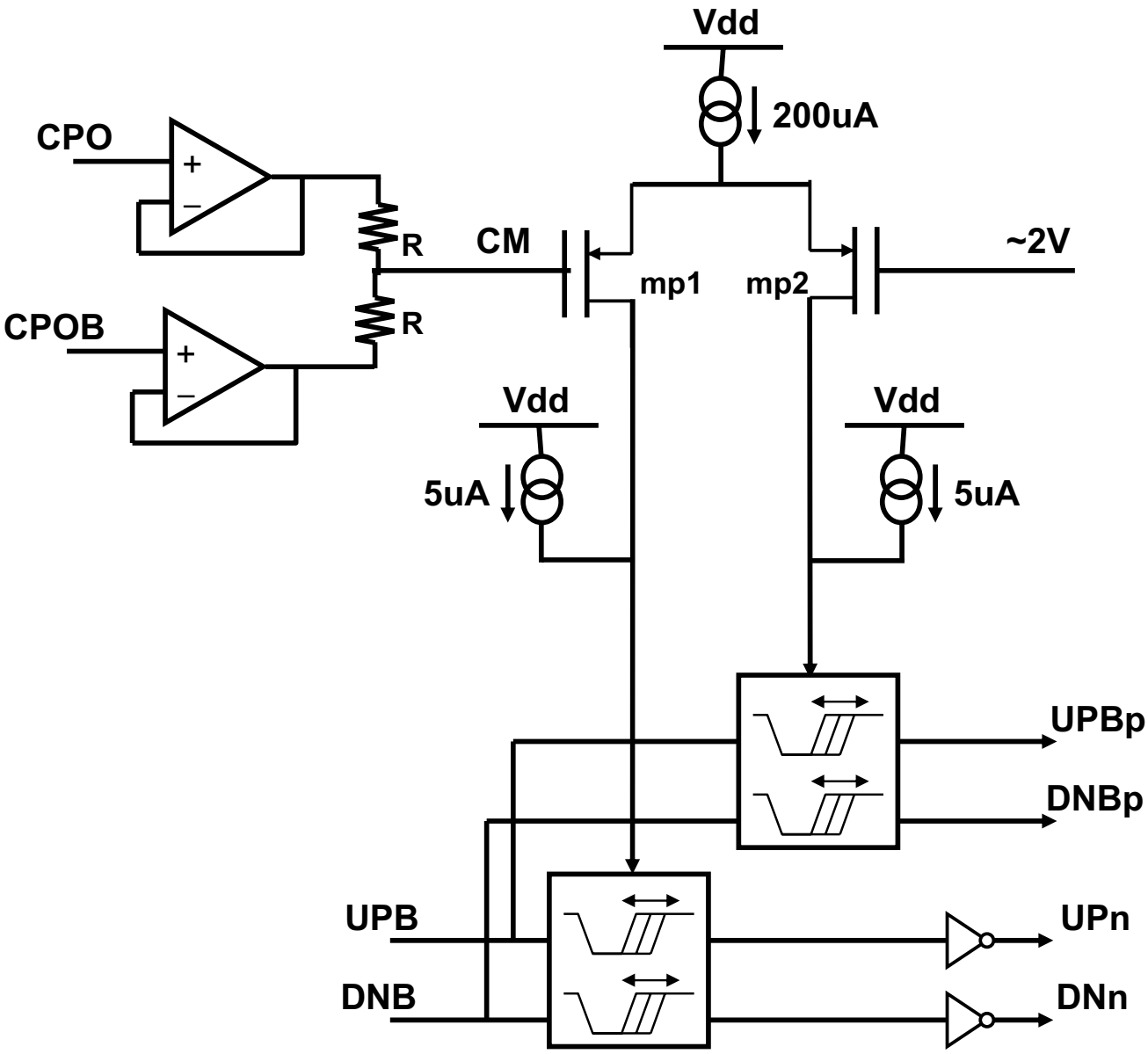


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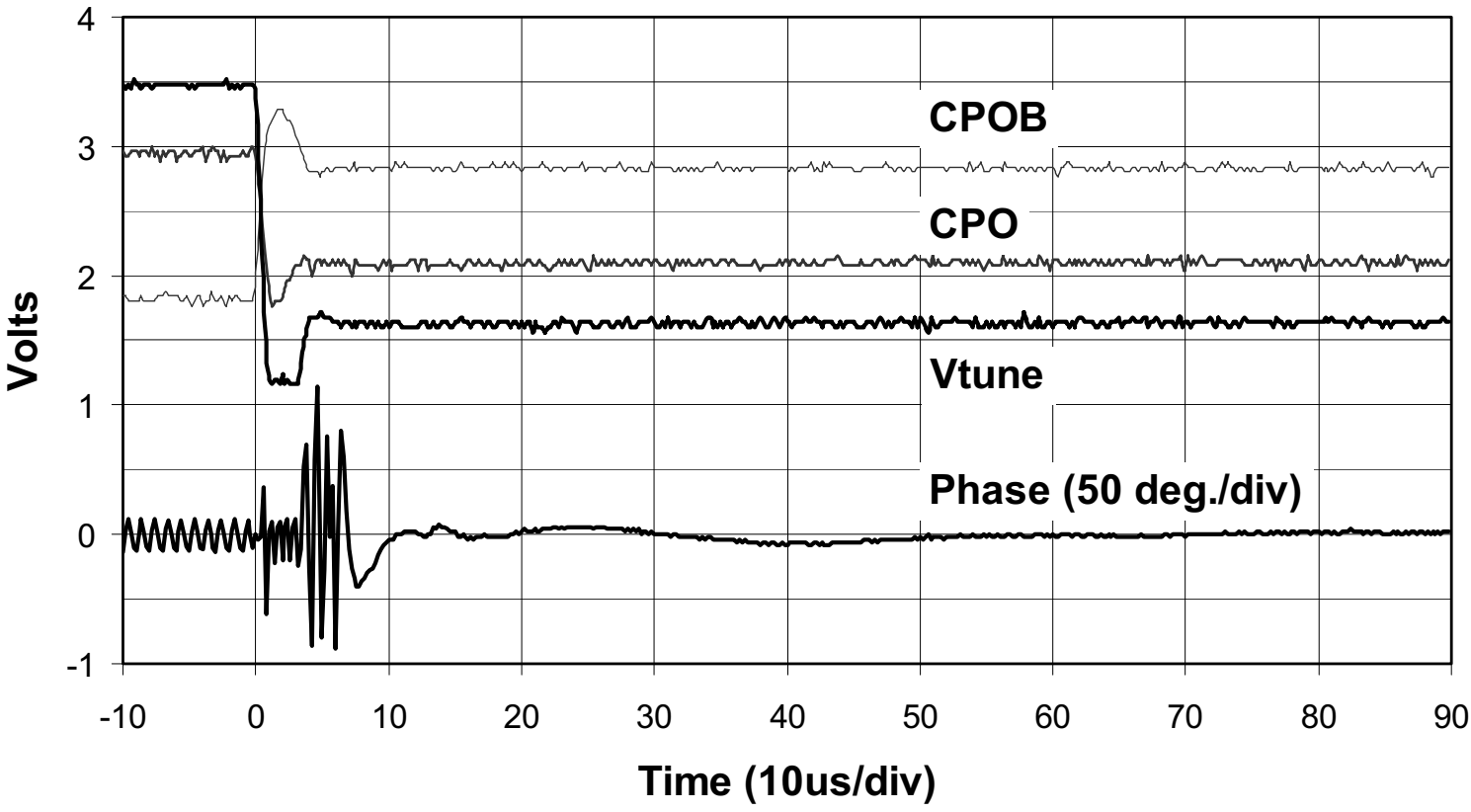


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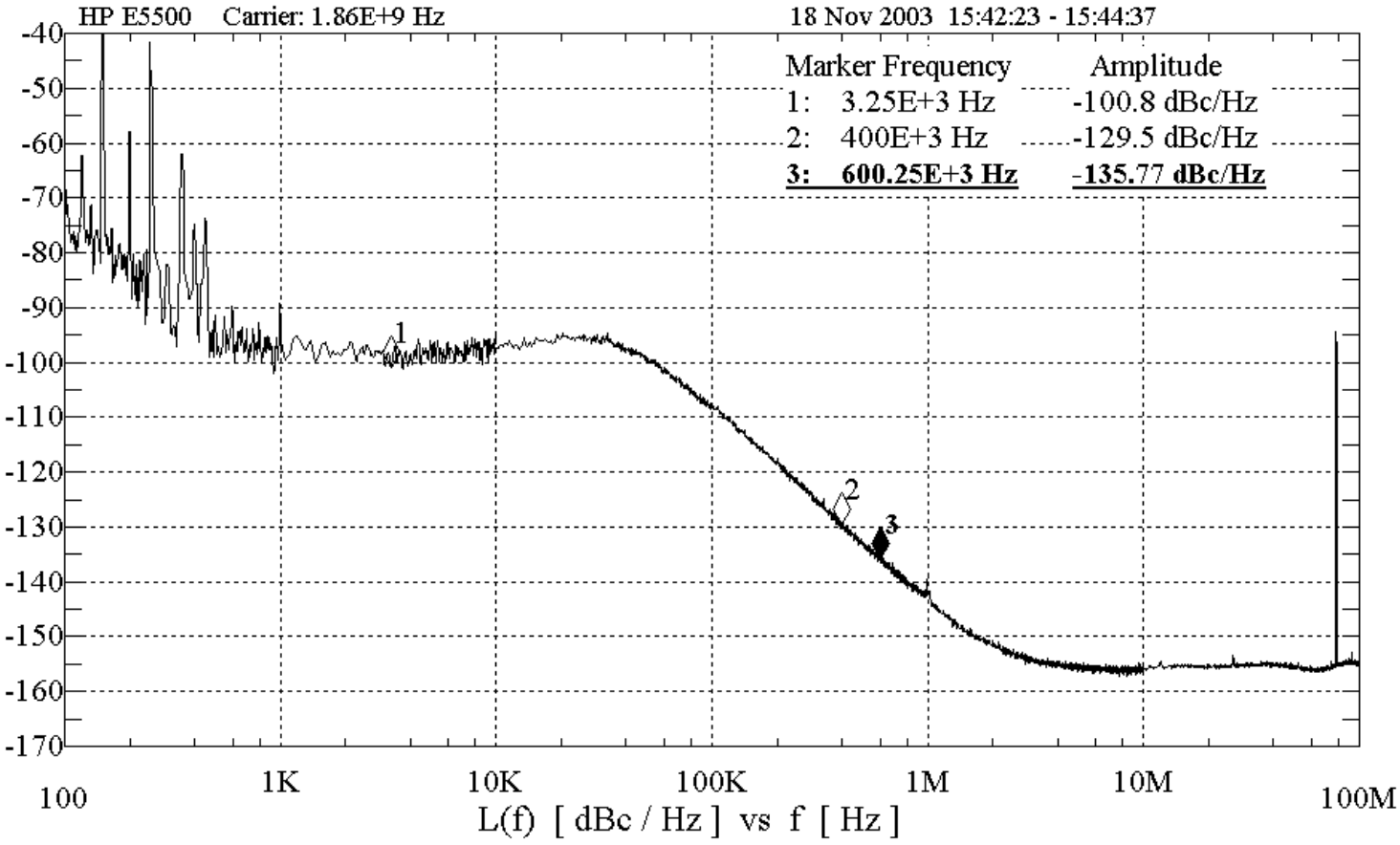


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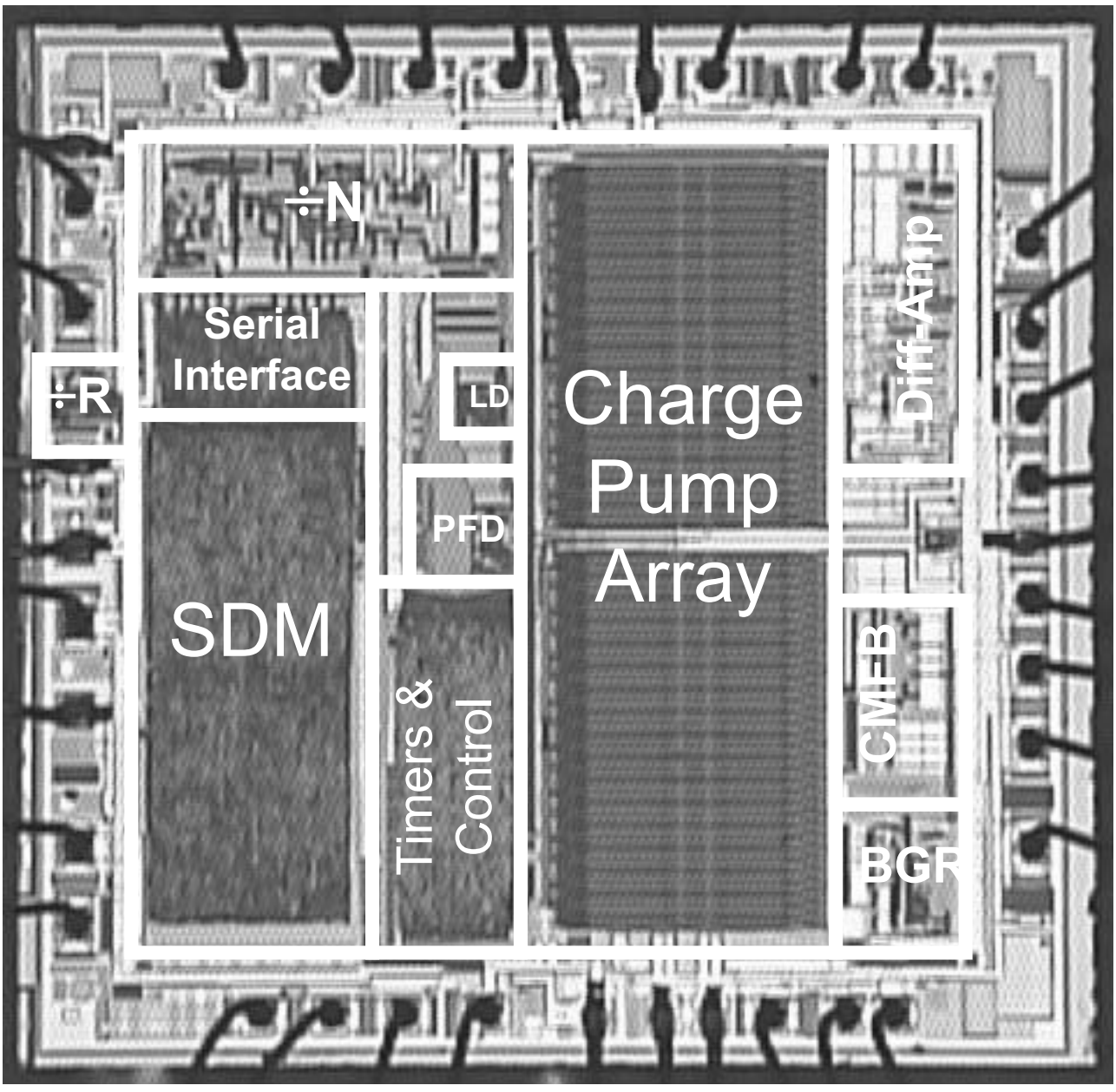


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