A 2.7-V 900-MHz CMOS LNA and Mixer

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***Abstract*— A CMOS low-noise amplifier (LNA) and a mixer for RF front-end applications are described. A current reuse technique will be described that increases amplifier transconductance for the LNA and mixer without increasing power dissipation, compared to standard topologies. At 900 MHz, the LNA minimum noise figure (NF) is 1.9 dB, input third-order intercept point (IIP3) is −3.2 dBm and forward gain is 15.6 dB. With a 1-GHz local oscillator (LO) and a 900-MHz RF input, the mixer minimum double sideband noise figure (DSB NF) is 5.8 dB, IIP3 is −4.1 dBm, and power conversion gain is 8.8 dB. The LNA and mixer, respectively, consume 20 mW and 7 mW from a 2.7 V power supply. The active areas of the LNA and mixer are 0.7 mm × 0.4 mm and 0.7 mm × 0.2 mm, respectively. The prototypes were fabricated in a 0.5-μm CMOS process.**

I. Introduction

THE demand for portable wireless communications systems is driven by the expansion of personal and commercial wireless services. As a result, the design of portable handsets follows trends that include lower cost, longer battery life, smaller size, and lower weight. These trends increase the focus on RF IC implementations that traditionally rely on bipolar or GaAs technologies for 1–2 GHz RF realms. At the same time, fine-line CMOS technologies continue to evolve as the demand for higher speed and more complex digital systems grows. The high-speed attribute of fine-line CMOS technology offers opportunity for RF IC implementation. Monolithic RF IC system integration is an important factor in meeting the design needs of portable communications applications [1]. Integration of RF building blocks into a CMOS monolithic system has the advantage of leveraging efforts in CMOS frequency synthesizer, IF, and baseband processing functions. This paper presents the design of a 2.7-V 900-MHz CMOS low-noise amplifier (LNA) and mixer. A current reuse technique will be described that achieves the same amplifier transconductance for the LNA and mixer but at a decreased power dissipation compared to standard topologies.

II. Design Objectives

The overall specifications for the LNA and mixer were derived from the front-end requirements of a North American Digital Cellular (NADC) handset. The primary design goal for the LNA and mixer is a total current consumption of 10 mA at a 2.7 V power supply. Fig. 1 shows the intended application of the LNA and mixer in a superheterodyne receiver front-end. As an external image-reject filter is employed, the LNA output must be capable of driving a 50 Ω load. The mixer IF output is an open-drain design to provide the option of driving either an impedance matching network for a high impedance IF filter or a buffer that in turn drives an IF filter. The primary CMOS process attributes are: drawn channel length of 0.5 μm, 90 Å gate-oxide thickness, three-level metal, and two-level nonsilicided polysilicon. Attention to layout is needed to minimize parasitic interconnect resistance and overlap capacitance that can degrade circuit performance.

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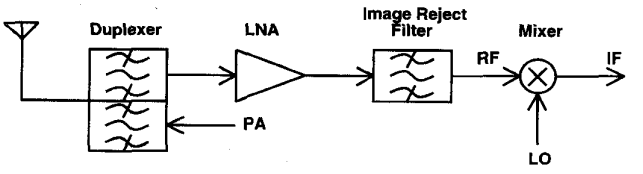

Fig. 1. Superheterodyne receiver front-end application of LNA and mixer.

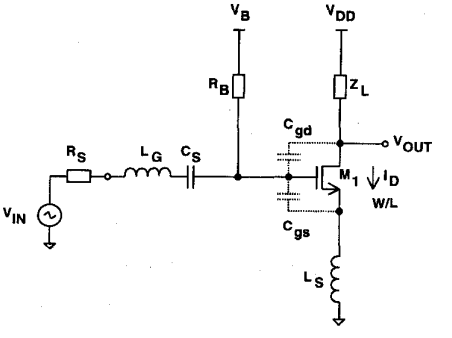

Fig. 2. Basic NMOS LNA design.

III. LNA Design

Fig. 2 shows a schematic of a basic NMOS LNA. For simplicity, the bias network is composed of V_B and R_B to set the desired gate bias voltage for M_1. The input is coupled to the gate of M_1 with coupling capacitor C_S. The input is matched to $R_S = 50\ \Omega$ by using inductors L_G and L_S. The matching condition can be shown to occur when

$$\omega^2 C_{gs}(L_G + L_S) \approx 1 \tag{1}$$

$$L_S \approx R_S C_{gs}/g_{m1} \tag{2}$$

where C_{gs} is the gate-source capacitance and g_{m1} is the transconductance of device M_1. With these conditions, the LNA noise factor F can be shown to be

$$F \approx 1 + (8\omega^2 C_{gs}^2 R_S)/(3g_{m1}). \tag{3}$$

The effect of the gate-drain capacitance C_{gd} is neglected in these first-order approximations. Since g_{m1} appears in the

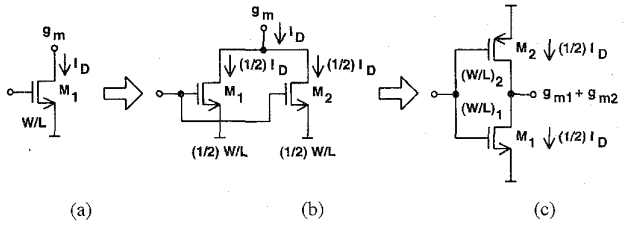

Fig. 3. Illustration of current reuse method.

denominator of (3), a large g_{m1} is typically needed to reduce the noise figure NF, where $NF = 10\log_{10}(F)$. The LNA in Fig. 2 is capable of achieving the desired NF specification, on the order of 2 dB. However, a large drain current I_D may be necessary. To relax this design tradeoff, a current reuse technique will be described.

Fig. 3 illustrates the current reuse method. The goal is to achieve the g_m and $\omega_T = g_m/C_{gs}$ of a single device with less current. Fig. 3(a) shows a single NMOS device that has aspect ratio W/L with drain current I_D. Fig. 3(b) shows two NMOS devices in parallel. Each of these devices has aspect ratio $(1/2)W/L$ and drain current $(1/2)I_D$. Thus, the transconductance of the compound device in Fig. 3(b) is the same as the transconductance of the device in Fig. 3(a). In Fig. 3(c), a PMOS device is substituted for device M_2 in Fig. 3(b). The total transconductance in Fig. 3(c) is $g_{mt} = g_{m1} + g_{m2}$. With $(W/L)_1 = (W/L)_2 = (1/2)W/L$, the input capacitance of Fig. 3(c) is $C_{gs1} + C_{gs2}$ which is nearly equal to C_{gs} in Fig. 3(a). Since the mobility of the PMOS device is lower, g_{mt} will be lower than g_m. For example, if $\mu_p \approx 0.5\mu_n$, then $g_{mt} \approx 0.85g_m$. This reduction in g_{mt} for this design results in 0.2 dB increase in NF, which is tolerable considering that the corresponding drain current is reduced by a factor of two.

The desired LNA design approach employs a cascade connection of two transconductance amplifier stages. A two-stage LNA design is motivated by the desire to relax the design requirements imposed by a one-stage design. A primary design consideration is driving a 50 Ω load while achieving high forward gain and low reverse gain. Low reverse gain is desired to provide sufficient isolation and to simplify input and output port matching.

Fig. 4 shows a schematic of the two-stage LNA design. In this design, stage 1 is used to achieve the overall LNA forward gain while stage 2 is used as a unity-gain buffer. The output of stage 1 is directly coupled to the input of stage 2. Bias amplifiers are used for each stage to establish the operating points for the respective stages. External networks N_S and N_L match the LNA input and output ports to 50 Ω, respectively. The RF input is applied at V_{RF}, thus driving the gates of M_1 and M_2 in the first stage. Since an external image reject filter is intended for use between the LNA output and the mixer RF input, the LNA output is capable of driving a load resistance R_L of 50 Ω. The operation of a single stage is described, as the stage topologies are identical. Focusing on the first stage in Fig. 4, devices M_1 and M_2 are configured such that the transconductance of the stage is $g_{mt} = g_{m1} + g_{m2}$, where g_{m1} and g_{m2} are the transconductances of devices M_1 and M_2, respectively. Capacitor C_B bypasses the source of M_1 to ground at high frequencies.

In the first stage shown in Fig. 4, a bias feedback amplifier is used to set the dc output voltage V_{OUT1} of the stage to the bias reference V_{B1} [2]. Devices M_{3-7} are used to steer bias current into devices M_1 and M_2. The bias reference I_{REF} and the current mirror composed of devices M_8 and M_2 are used to establish the desired bias current in devices M_1 and M_2. The bias feedback loop is completed with a low-pass filter, composed of R_X and C_X, that provides the dc output voltage V_{X1} from V_{OUT1}. The low-frequency pole contributed by the filter dominates the bias feedback amplifier loop transmission to achieve a high phase margin for the loop. Direct coupling is utilized between the output of the first stage and the input of the second stage. The bias reference V_{B1} sets the dc output voltage V_{OUT1} for the first stage and thus sets the dc input voltage of the second stage. The second stage bias current is thus determined. The second stage bias feedback amplifier is used to set the dc output voltage V_{OUT2} to bias reference V_{B2}. In this design, $V_{B1} = V_{B2} = V_A$, where V_A is the dc input voltage of the first stage determined by I_{REF}.

IV. Mixer Design

Fig. 5 shows a basic NMOS mixer design. A single device M_1 is used as a transconductance amplifier and a mixing cell composed of devices M_{2-3} is used to perform the chopping function. The mixer in Fig. 5 is capable of achieving the desired double sideband noise figure (DSB NF) specification, on the order of 8 dB, however, a large drain current I_D may be necessary. To relax this design tradeoff, the current reuse technique is employed.

Fig. 6 shows the desired mixer transconductance amplifier design. The design is similar to a single stage of an LNA. For simplicity, the bias network is composed of V_{B1-2} and R_{B1-2} to set the desired gate bias voltage for M_{1-2}. The input is coupled to the gates of M_{1-2} with coupling capacitor C_{S1-2}. The input is matched to $R_S = 50\ \Omega$ by using inductors L_G and L_{S1-2}. A matching condition similar to that of the LNA in Fig. 2 can be derived for the mixer. Fig. 6 shows a mixer cell interposed between the drains of devices M_1 and M_2. The drain current is thus reused among M_2, the mixer cell and M_1. The mixer cell design is shown in Fig. 7. Devices M_{1-4} compose the main mixer cell driven by the differential local oscillator (LO) inputs V_{LO1} and V_{LO2}. The drain currents I_{D1-2} are steered through devices M_1 and M_3 as shown in Fig. 7(a), or through devices M_2 and M_4 as shown in Fig. 7(b), as a function of the LO phase.

Fig. 8 shows a schematic of the mixer. An external network N_S matches the mixer RF port to 50 Ω. The RF input is applied at V_{RF}, driving V_{RF1} and V_{RF2}, and thus the gates of M_5 and M_6, in phase. Devices M_5 and M_6 are configured as a transconductance amplifier with $g_{mt} = g_{m5} + g_{m6}$, where g_{m5} and g_{m6} are the transconductances of devices M_5 and M_6, respectively. With an input V_{RF} applied, the drain currents of M_5 and M_6 differ by $g_{mt}V_{\mathrm{RF}}$. This difference current is then chopped by the mixer cell resulting in the desired intermediate frequency (IF) current at the mixer output ports, V_{OUT1} and

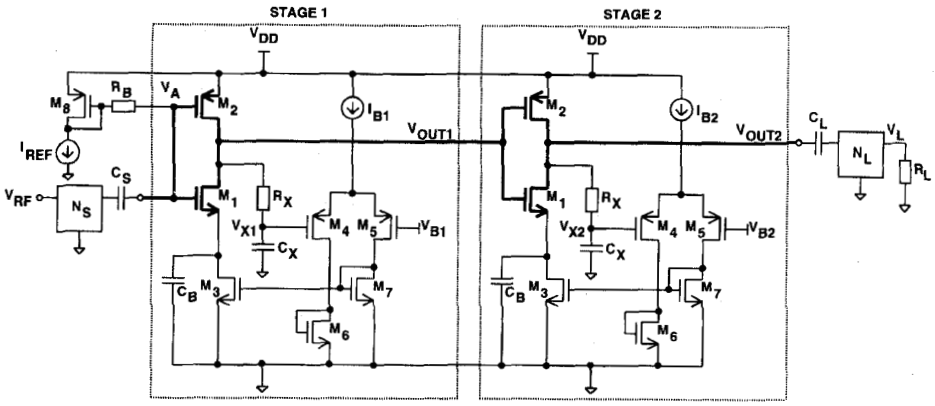

Fig. 4. Schematic diagram of the CMOS LNA.

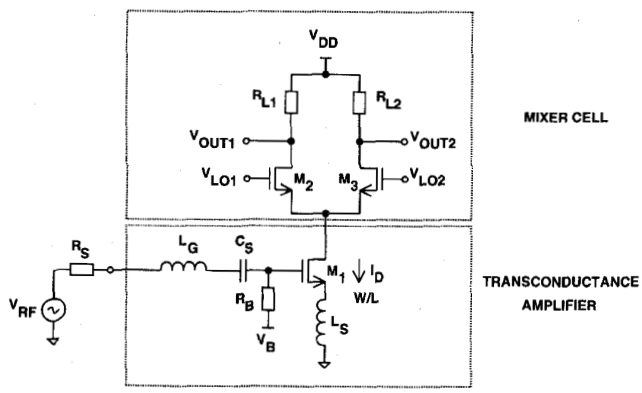

Fig. 5. Basic NMOS mixer design.

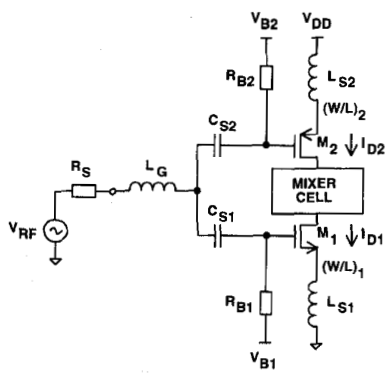

Fig. 6. CMOS mixer transconductance amplifier design.

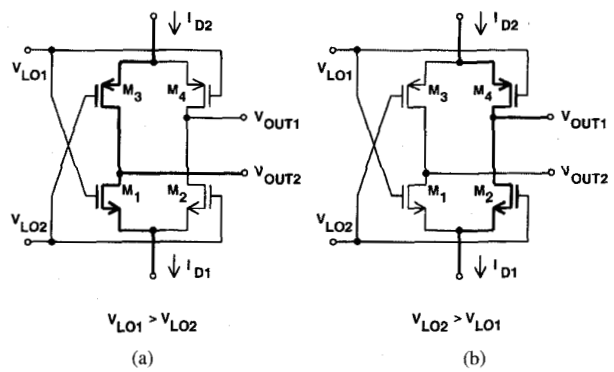

Fig. 7. CMOS mixer cell design.

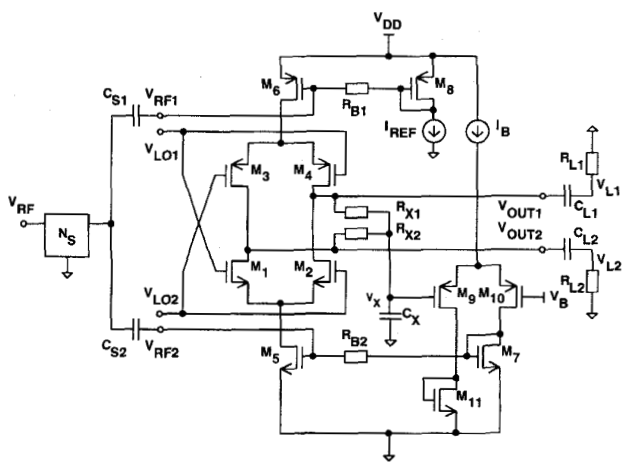

Fig. 8. Schematic diagram of the CMOS mixer.

V_{OUT2}. The high impedance mixer outputs are intended to drive an external high impedance load.

The mixer biasing approach is similar to the technique used for the LNA stages. A common mode feedback amplifier is used to set the dc common mode output level of the mixer, V_X, to the bias reference, V_B. A differential pair and current mirror composed of devices M_5, M_7, M_{9-11} are used to steer bias current into the mixer cell. Bias reference I_{REF} and the current mirror composed of devices M_8 and M_6 are used to establish the desired bias current in the mixer cell. The feedback loop is completed with a low-pass filter, composed of R_{X1}, R_{X2}, and C_X, that provides the dc common mode level V_X from the outputs V_{OUT1} and V_{OUT2}.

V. Experimental Results

The LNA and mixer IC's are individually packaged and tested. The measured performance of the LNA is summarized in Table I. The measured performance of the mixer is summarized in Table II. The LNA and mixer NF measurements are

TABLE I
SUMMARY OF LNA MEASUREMENTS

LNA	Measured Parameters
Supply voltage	2.7V
Power dissipation	20mW
Frequency	900MHz
NF (50 Ω)	2.2dB
Min. NF	1.9dB
Forward gain $\|S_{21}\|$	15.6dB
Reverse gain $\|S_{12}\|$	−32.4dB
Input IP3	−3.2dBm
Input 1dB compression level	−15.2dBm

TABLE II
SUMMARY OF MIXER MEASUREMENTS

Mixer	Measured Parameters
Supply voltage	2.7V
Power dissipation	7mW
RF frequency	900MHz
LO frequency (0 dBm)	1GHz
DSB NF (50 Ω)	6.7dB
Min. DSB NF	5.8dB
Power conversion gain	8.8dB
Input IP3	−4.1dBm
Input 1dB compression level	−16.1dBm
LO-RF feedthrough	−59.6dB
LO-IF feedthrough	−34.4dB

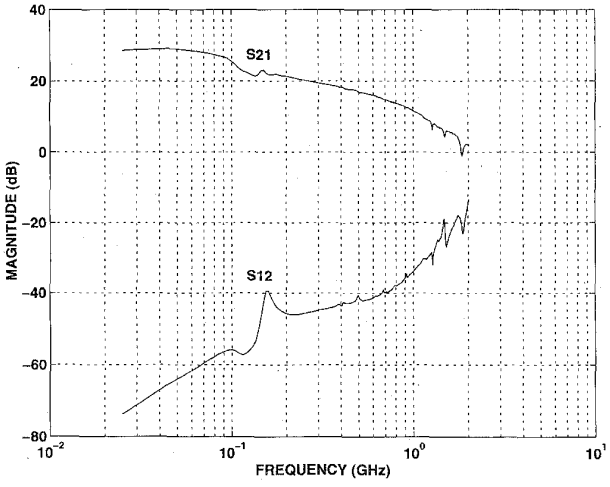

Fig. 9. Measured LNA gain magnitudes $|S_{21}|$ and $|S_{12}|$, swept from 25 MHz to 2 GHz, without external matching networks.

referred to 50 Ω at a frequency of 900 MHz. The DSB NF measurements are reported for the mixer. The single sideband (SSB) NF of the mixer can be estimated to be 3 dB higher than the DSB NF if the mixer conversion gain at frequencies LO−IF and LO+IF are similar [3], as in the mixer presented in this work.

The wideband frequency response measurements in Figs. 9 and 10 are performed without matching networks. Fig. 9 shows the measured LNA forward and reverse gain magnitudes, $|S_{21}|$ and $|S_{12}|$, respectively, swept from 25 MHz to 2 GHz. Fig. 10 shows a zoomed-in measurement of Fig. 9 from 800 MHz to 1 GHz.

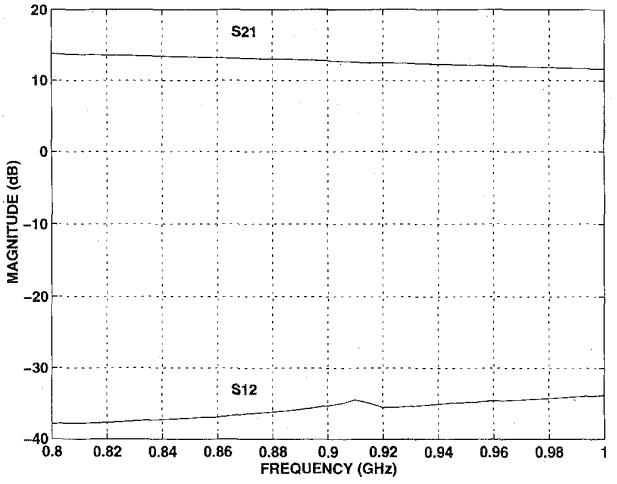

Fig. 10. Measured LNA gain magnitudes $|S_{21}|$ and $|S_{12}|$, swept from 800 MHz to 1 GHz, without external matching networks.

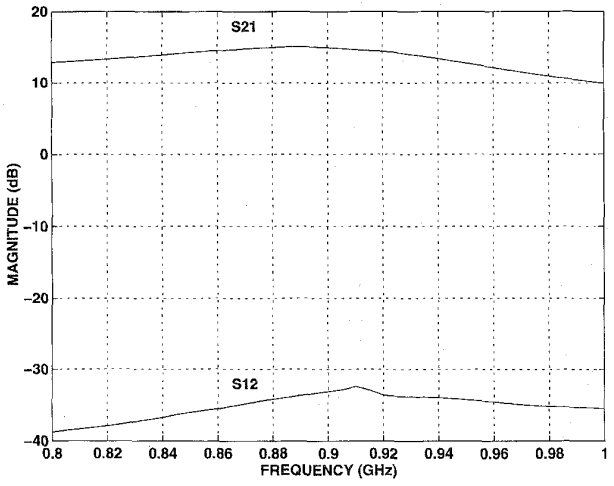

Fig. 11. Measured LNA gain magnitudes $|S_{21}|$ and $|S_{12}|$, swept from 800 MHz to 1 GHz, with external matching networks.

Figs. 11 and 12 show measurements performed with matching networks for the LNA input and output ports. Fig. 11 shows the measured LNA $|S_{21}|$ and $|S_{12}|$, swept from 800 MHz to 1 GHz. Fig. 12 shows the measured LNA output spectrum when a two-tone RF input at 899.5 MHz and 900.5 MHz is applied. The RF input power level is −31 dBm for each tone.

Fig. 13 shows measurements performed with a matching network for the mixer RF port. Fig. 13 shows the measured mixer IF output spectrum when a two-tone RF input at 899.5 MHz and 900.5 MHz is mixed with a LO frequency at 1 GHz. The RF input power level is −29 dBm for each tone and the LO power level is 0 dBm.

The external matching networks are implemented with manual slide-screw tuners that feature locking verniers and

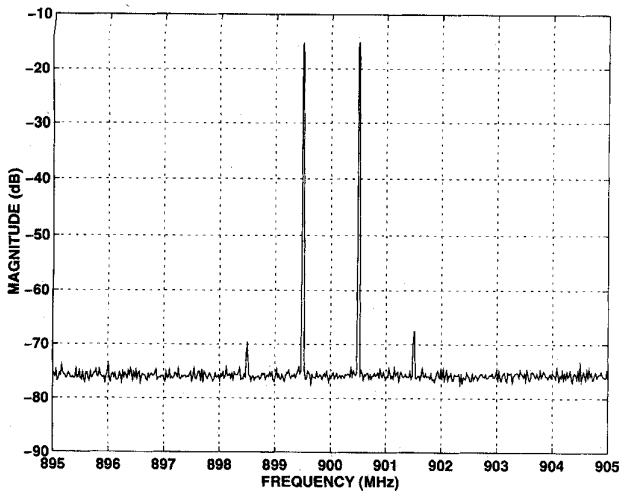

Fig. 12. Measured LNA output spectrum, RF input power level −31 dBm at 899.5 MHz and 900.5 MHz, with external matching networks.

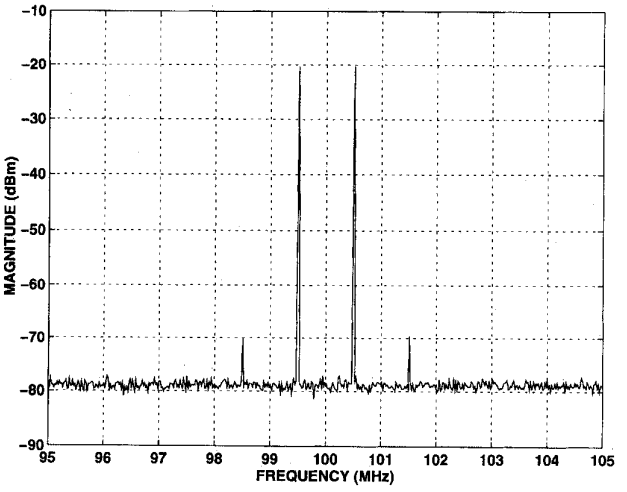

Fig. 13. Measured mixer IF output spectrum, RF input power level −29 dBm at 899.5 MHz and 900.5 MHz, LO input power level 0 dBm at 1 GHz, with external matching network at the RF port.

micrometers for repeatability. The bondwires that are used for the V_{DD} and V_{SS} power supply connections provide real-part contribution to the LNA input impedance and the mixer RF port input impedance [2]. The measurements for Figs. 12 and 13 are repeated for different input power levels, below the respective input referred 1 dB compression levels, in order to predict the input IP3 extrapolation.

Fig. 14 shows a Smith chart for the measured LNA S_{11} and S_{22}, swept from 800 MHz to 1 GHz. Fig. 15 shows a Smith chart for the measured mixer RF port S_{11}, swept from 800 MHz to 1 GHz. Referring to Figs. 14 and 15, when the input reflection coefficient is set to point "G," $\Gamma_S = \Gamma_G$, maximum gain occurs. When the input reflection coefficient is set to point "NF," $\Gamma_S = \Gamma_{NF}$, minimum noise figure occurs [4]. When $\Gamma_S = \Gamma_{NF}$, the input return loss, or reflection

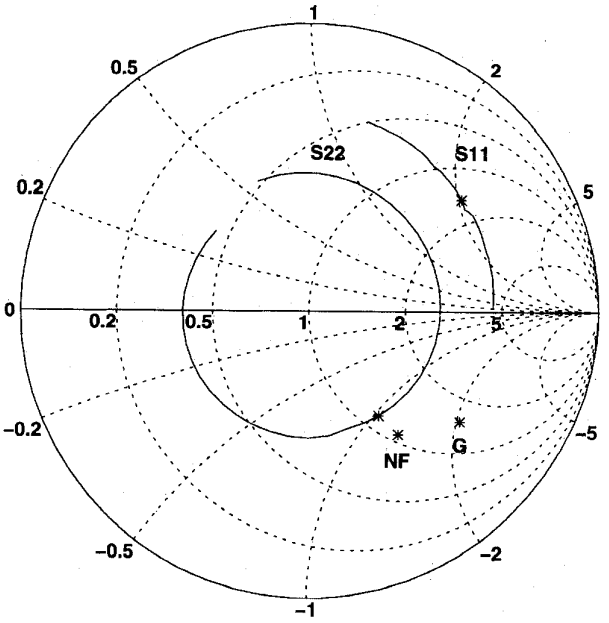

Fig. 14. Measured LNA Smith chart for S_{11} and S_{22}, swept from 800 MHz to 1 GHz. Source reflection coefficient measured at 900 MHz for maximum gain, $\Gamma_S = \Gamma_G$, and for minimum $NF, \Gamma_S = \Gamma_{NF}$.

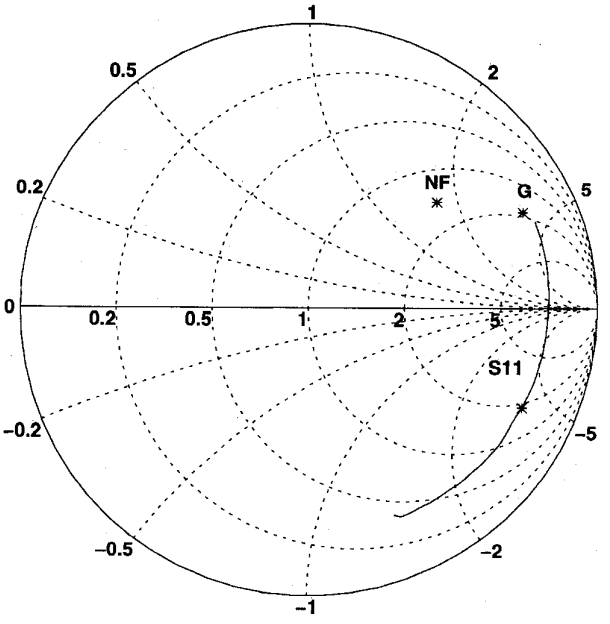

Fig. 15. Measured mixer Smith chart for the RF port S_{11}, swept from 800 MHz to 1 GHz. Source reflection coefficient measured at 900 MHz for maximum gain, $\Gamma_S = \Gamma_G$, and for minimum $NF, \Gamma_S = \Gamma_{NF}$.

coefficient magnitude, for the LNA is $RL = -11$ dB and for the mixer RF port is $RL = -7$ dB.

The LNA and mixer designs utilize external coupling capacitors at the input and output ports. The prototypes are measured in thin quad flat pack (TQFP) packages. Fig. 16 shows a micrograph of the LNA and Fig. 17 shows a micrograph of the mixer. The active areas of the LNA and mixer are 0.7 mm × 0.4 mm and 0.7 mm × 0.2 mm, respectively.

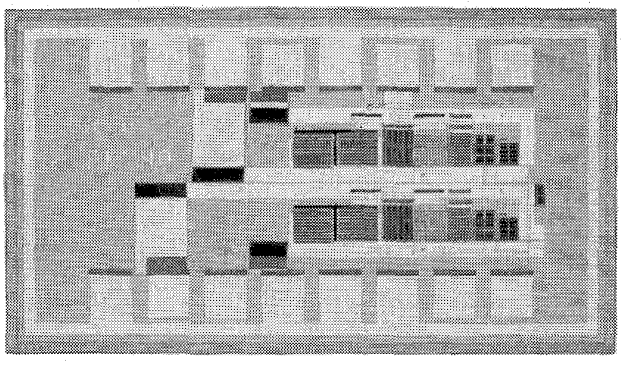

Fig. 16. Micrograph of the LNA.

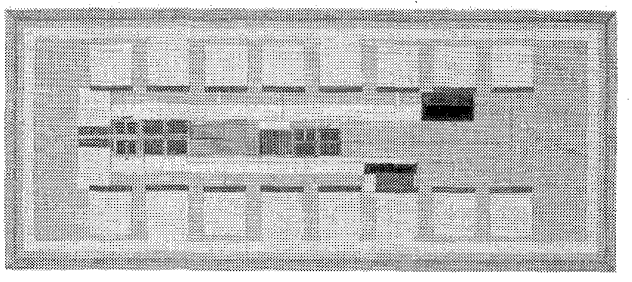

Fig. 17. Micrograph of the mixer.

VI. Conclusions

A two-stage LNA design with a 50 Ω output drive capability has been described. The LNA stages utilize a current reuse method in order to reduce the current consumption required to attain a performance level compatible with NADC. A mixer utilizing a current reuse method is described. The mixer transconductance amplifier is based on an LNA stage design and the mixer chopping cell is compatible with the current reuse method. Experimental results indicate that CMOS technology can be used to build an LNA and mixer while meeting output drive, noise, and linearity requirements for portable cellular systems.

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