A New Model for Thermal Channel Noise of Deep-Submicron MOSFETS and its Application in RF-CMOS Design

Gerhard Knoblinger, *Member, IEEE*, Peter Klein, and Marc Tiebout, *Member, IEEE*

***Abstract*—In this paper, we present a simple analytical model for the thermal channel noise of deep-submicron MOS transistors including hot carrier effects. The model is verified by measurements and implemented in the standard BSIM3v3 SPICE model. We show that the consideration of this additional noise caused by hot carrier effects is essential for the correct simulation of the noise performance of a low noise amplifier in the gigahertz range.**

***Index Terms*—Integrated circuit modeling, integrated circuit noise, MOSFETs, MOSFET amplifiers, semiconductor device modeling, semiconductor device noise.**

I. Introduction

DUE TO continuous reduction of minimum channel length in CMOS technologies in the last years, CMOS has become a candidate for RF applications. For quarter and subquarter micron technologies, transit frequencies (f_t) in the range of 40–70 GHz and maximum oscillation frequencies up to 40 GHz and more are possible for nMOS transistors [1]. For these devices, the classical assumption of thermal equilibrium in the calculation of the channel noise is questionable. Additionally, so-called hot carrier noise is observed for short-channel transistors [2]–[6].

The purpose of this work is to develop an analytical model for thermal channel noise of extreme short-channel transistors and the implementation in the BSIM3v3 model. With this model RF-CMOS designers are able to simulate the noise performance of their designs (e.g., low noise amplifiers (LNAs), which are an essential part of system-on-a-chip solutions for wireless communication), and to find the optimum between noise performance and ac performance.

II. Thermal Channel Noise Model

A. Classical Models for Thermal Channel Noise

In most MOS SPICE models normally used, the following equation for the spectral noise density of the drain current S_i is implemented and widely used in noise simulations:

$$S_i = \tfrac{8}{3}\, kT_0(g_m + g_{ds} + g_{mb}). \tag{1}$$

Manuscript received July 24, 2000; revised December 1, 2000.

G. Knoblinger and P. Klein are with Infineon Technologies AG Germany, SIM PX1, D-81609, Munich, Germany (e-mail: gerhard.knoblinger@infineon.com).

M. Tiebout is with Infineon Technologies AG Germany, WS TI S RSC, D-81609 Munich, Germany.

Publisher Item Identifier S 0018-9200(01)03027-X.

g_m is the gate transconductance, g_{ds} is the channel conductance, and g_{mb} is the bulk transconductance.

In [7] the following formula is derived:

$$S_i = \frac{4kT_0}{L^2}\,\mu Q_{\text{inv}}. \tag{2}$$

Q_{inv} is the inversion layer charge, L is the channel length, and μ is the mobility.

In general, an effective mobility μ_{eff} is used in compact models, taking into account the influence of vertical and lateral electric fields, giving

$$S_i = \frac{4kT_0}{L^2}\,\mu_{\text{eff}} Q_{\text{inv}} \tag{3}$$

$$\mu_{\text{eff}} = \frac{\mu_S}{\left(1 + \left(\dfrac{E_X}{E_{\text{crit}}}\right)^{\beta}\right)^{1/\beta}}. \tag{4}$$

$E_X = V_{d\text{seff}}/L_{\text{eff}}$ is the lateral electric field, $E_{\text{crit}} = v_{\text{sat}}/\mu_s$, v_{sat} is the saturation velocity, $\beta = 2$ for electrons [8], μ_s is the surface mobility in the BSIM3v3 model, and

$$V_{d\text{seff}} = \begin{cases} V_{ds} & \text{in lin. region} \\ V_{d\text{ssat}} & \text{in saturation.} \end{cases}$$

B. Extraction of Thermal Channel Noise out of RF Noise Measurements

A commercial noise-figure measurement setup was used (ATN) and on wafer measurements from 600 MHz up to 6 GHz have been performed. This frequency range is high enough to clearly separate $1/f$ and white noise. The noise measurements are de-embedded with the noise de-embedding method presented in [9]. Exact de-embedding of the noise measurements is very important, because the influence of the parasitics (pads and substrate resistors) on the NF50 (noise figure with 50-Ω source resistance) value can be significant. At the same structures, S parameters are also measured and de-embedded with usual standard methods. For the exact extraction of the thermal noise, all additional noise sources in the small-signal equivalent circuit have to be considered. It is not necessary to have an exact small-signal equivalent circuit of the transistor, because the measured S or y parameters are used directly for the calculations. The circuits in Figs. 1 and 2 are used to calculate the contributions of the noise sources to the NF50 value, where Fig. 1 is only used for the calculation

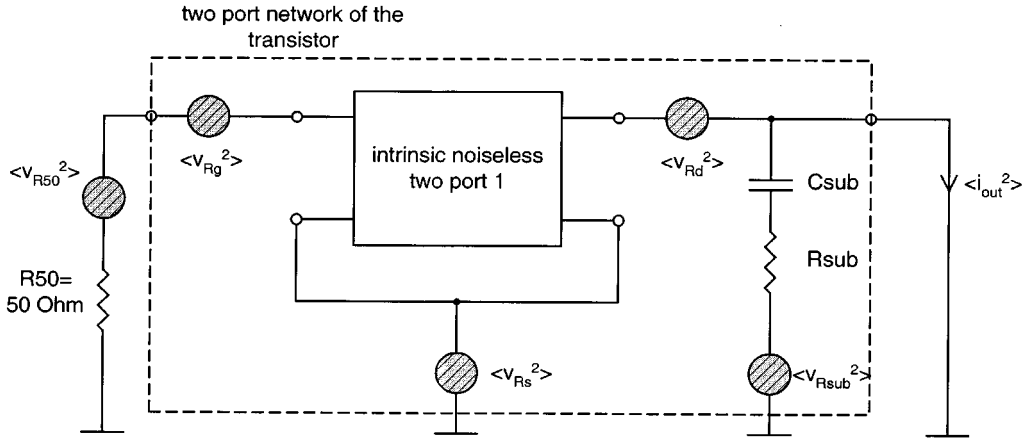


Fig. 1. Circuit for the calculation of the contribution of gate resistance ($\langle v_{Rg}^2 \rangle$), source resistance ($\langle v_{Rs}^2 \rangle$), drain resistance ($\langle v_{Rd}^2 \rangle$), substrate resistance ($\langle v_{Rsub}^2 \rangle$) and the 50-$\Omega$ resistance ($\langle v_{R50}^2 \rangle$) to the NF50 value. The intrinsic noiseless two-port represents the whole transistor except the substrate components (separated with y parameter subtraction).

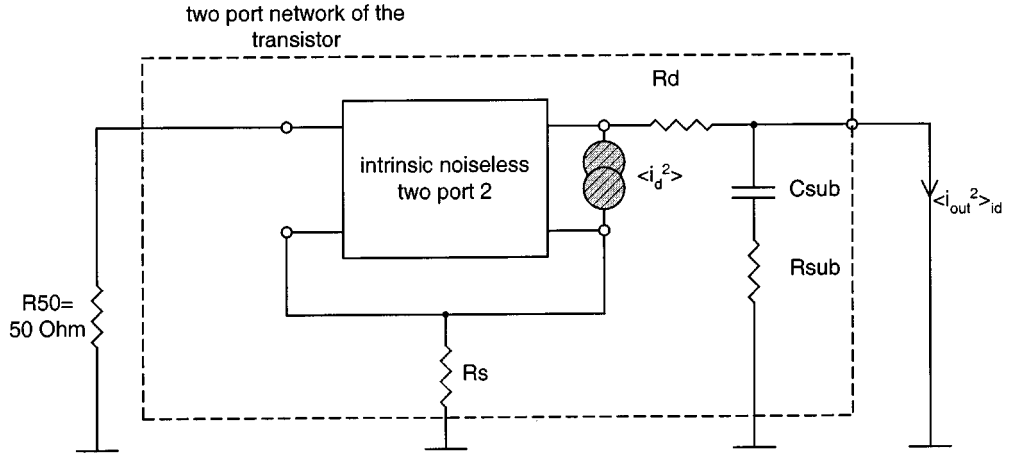


Fig. 2. Circuit for the calculation of the contribution of the channel noise ($\langle i_d^2 \rangle$) to the NF50 value. The intrinsic noiseless two-port represents the whole transistor except the substrate components (separated with y parameter subtraction) and drain (R_d) and source (R_s) resistors (separated with z parameter subtraction).

of the parasitics and R_{50} contribution, and Fig. 2 is used for the calculation of the channel noise contribution. The gate resistance is extracted from the layout and the source and drain resistors are extracted from dc measurements. The substrate resistor and the junction substrate capacitor are extracted from the two-port parameter $z22$. The NF50 value of the whole circuit is calculated using (5). In this equation, all values are known except the contribution of the channel noise $(\overline{i_{\text{out}}^2})_{id}$ as shown in (5), at the bottom of the page.

With the help of Fig. 2 and (5), the channel noise $\overline{i_d^2}$ is calculated. In Fig. 3 the extracted channel noise is plotted for two different bias points versus frequency. To make sure, the gate-induced noise is negligible for all test structures, only frequencies up to 2 GHz ($<f_t/10$) are taken into account for the calculation of the mean value for each bias point. Details of the extraction procedure of the channel noise are described in [10].

In Fig. 4, simulation results with (1) and (3) are compared with values of the spectral noise density of the drain current extracted from NF50 measurements for different V_{gs} and constant V_{ds}. Depending on the bias point and the model which is used, the simulation could be up to a factor 4 smaller than the measurement.

C. New Model Including Hot Carrier Effects

According to [7], the contribution of a small element of the channel dx to the spectral noise density of the current is

$$dS_i = \frac{4kT_e W \mu(x) Q_{\text{inv}}(x)}{L^2}\, dx \tag{6}$$

$$\text{NF50} = \frac{\left(\overline{\text{i}_{\text{out}}^2}\right)_{R50} + \left(\overline{\text{i}_{\text{out}}^2}\right)_{Rg} + \left(\overline{\text{i}_{\text{out}}^2}\right)_{Rs} + \left(\overline{\text{i}_{\text{out}}^2}\right)_{Rd} + \left(\overline{\text{i}_{\text{out}}^2}\right)_{Rsub} + \left(\overline{\text{i}_{\text{out}}^2}\right)_{id}}{\left(\overline{\text{i}_{\text{out}}^2}\right)_{R50}}. \tag{5}$$

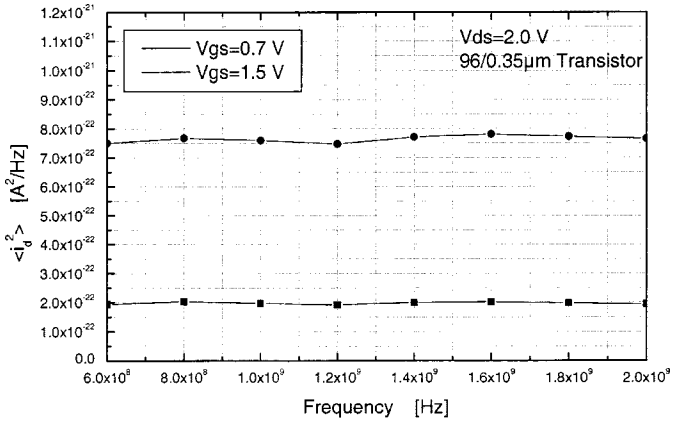


Fig. 3. Extracted thermal channel noise versus frequency for two different operating points of a 96/0.35-μm nMOS transistor.

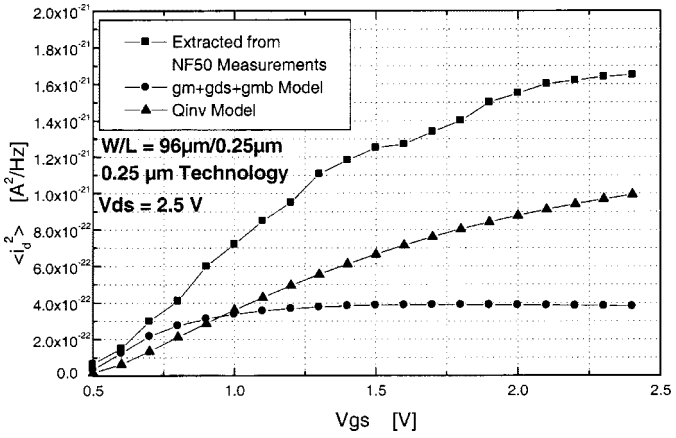


Fig. 4. Comparison between noise model (1) and (3) and measurement results for a 0.25-μm nMOS transistor.

where T_e is the electron temperature. In [7], $T_e = T_0$ is assumed, although T_e depends on the electric field $E(x)$ [11]

$$T_e = T_0 + \delta T_0 \frac{E(x)^2}{E_{\text{crit}}^2} \tag{7}$$

with δ being a parameter to adjust the simulation to the measurement.

For the calculations, the transistor channel is divided into a gradual channel region (I) and a velocity saturation region (II) [6]; see Fig. 5.

Combining (6) and (7) and integrating over the channel length gives

$$S_{iI} = \frac{4k}{L^2}\left[\underbrace{\int_0^{L_{\text{eff}}} WT_0\mu(x)Q_{\text{inv}}(x)\,dx}_{Ia} + \underbrace{\delta\int_0^{L_{\text{eff}}} WT_0\frac{E(x)^2}{E_{\text{crit}}^2}\mu(x)Q_{\text{inv}}(x)\,dx}_{Ib}\right] \tag{8a}$$

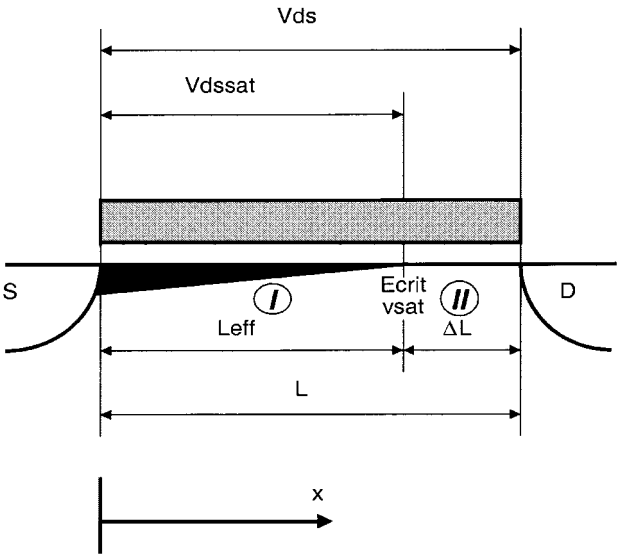


Fig. 5. Separation of the transistor channel in a gradual channel region (I) and a velocity saturation region (II).

$$S_{iII} = \frac{4k}{L^2}\left[\underbrace{\int_{L_{\text{eff}}}^{L} WT_0\mu(x)Q_{\text{inv}}(x)\,dx}_{IIa} + \underbrace{\delta\int_{L_{\text{eff}}}^{L} WT_0\frac{E(x)^2}{E_{\text{crit}}^2}\mu(x)Q_{\text{inv}}(x)\,dx}_{IIb}\right] \tag{8b}$$

where S_{iI} is the spectral noise density of region I and S_{iII} the density of region II. The whole spectral noise density is the sum of these two values: $S_i = S_{iI} + S_{iII}$.

With the use of $\mu(x) = v(x)/E(x)$ and $I_D = Wv(x)Q_{\text{inv}}(x)$ [where $v(x)$ is the velocity and I_D is the dc drain current] and the relation for the electric field in region II from [12]

$$E(x) = E_{\text{crit}}\cosh(\alpha x) \tag{9}$$

the formula for the spectral noise density of the thermal channel noise including hot carrier effects is [for α see (14)]

$$\begin{aligned} S_i = {} & \underbrace{\frac{4kT_0}{L^2}\mu_{\text{eff}}Q_{\text{inv}}}_{Ia} + \underbrace{\delta\frac{4kT_0I_D}{L^2E_{\text{crit}}^2}V_{d\text{seff}}}_{Ib} \\ & + \underbrace{\frac{4kT_0I_D}{L^2E_{\text{crit}}}\frac{2}{\alpha}\left\{\arctan\left[\exp(\alpha\,\Delta L)\right] - \arctan(1)\right\}}_{IIa} \\ & + \underbrace{\delta\frac{4kT_0I_D}{L^2E_{\text{crit}}}\frac{1}{\alpha}\sinh(\alpha\,\Delta L)}_{IIb}. \end{aligned} \tag{10}$$

In Fig. 6, the four parts of (10) are plotted for a 0.18-μm nMOS transistor versus V_{gs} at $V_{ds} = 1.8$ V. It can be seen that Part Ib (hot carrier effects in region I) and IIa (thermal equilibrium part

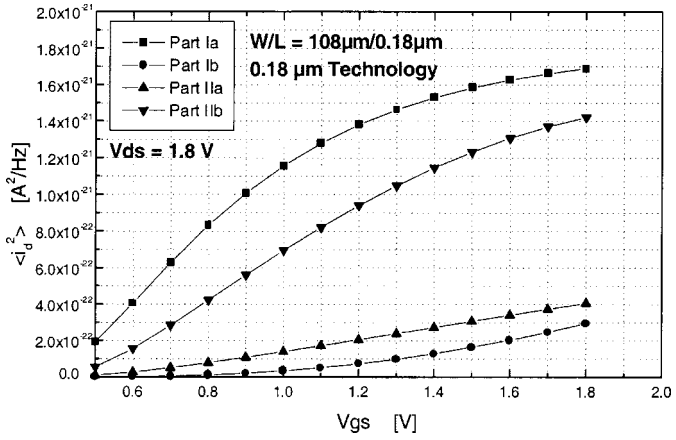


Fig. 6. Contribution of the different parts of (10) to the spectral noise density of the drain current of a 0.18-μm nMOS transistor.

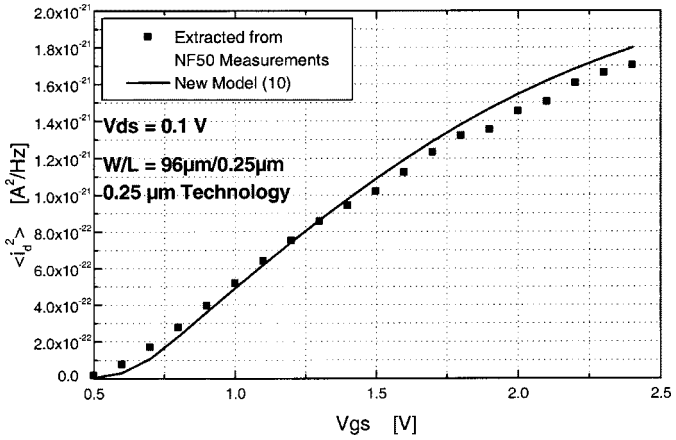


Fig. 7. Comparison between thermal channel noise extracted from NF50 measurements and simulation with (11) for a 0.25-μm nMOS in linear region versus V_{gs}.

of region II) are relatively small compared to Ia (thermal equilibrium part of region I) and IIb (contribution of the hot carriers in the saturation region II).

To get a simple analytical model, Parts Ib and IIa are neglected and we obtain

$$S_i = \underbrace{\frac{4kT_0}{L^2}\,\mu_{\text{eff}} Q_{\text{inv}}}_{Ia} + \underbrace{\delta \frac{4kT_0 I_D}{L^2 E_{\text{crit}}}\,\frac{1}{\alpha}\,\sinh(\alpha\,\Delta L)}_{IIb} \qquad (11)$$

where ΔL is the length of the velocity saturation region [13] (Fig. 5).

$$\Delta L = \frac{1}{\alpha}\ln\left[\frac{\alpha(V_{ds}-V_{d\text{sat}})+E_D}{E_{\text{crit}}}\right] \qquad (12)$$

$$E_D = E_{\text{crit}}\sqrt{1+\left[\frac{\alpha(V_{ds}-V_{d\text{sat}})}{E_{\text{crit}}}\right]^2} \qquad (13)$$

$$\alpha = \lambda\sqrt{\frac{3}{2}\,\frac{C_{\text{ox}}}{x_j \varepsilon_{si}\varepsilon_0}}\,. \qquad (14)$$

x_j is the junction depth of the source and drain region, C_{ox} is the gate–oxide capacitance, and λ is an additional parameter to adjust the channel length modulation (in this work: $\lambda = 3$). As it can be seen from (11), δ is the only noise parameter to adjust the noise simulation to the measurement results.

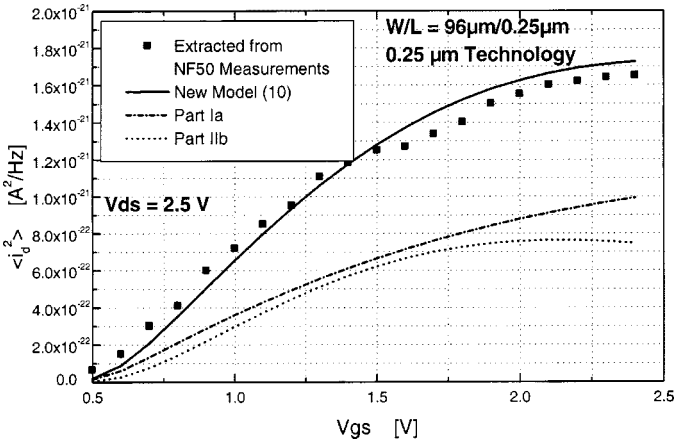


Fig. 8. Comparison between thermal channel noise extracted from NF50 measurements and simulation with (11) for a 0.25-μm nMOS at $V_{ds} = 2.5$ V versus $V_{gs}(\delta = 0.4)$.

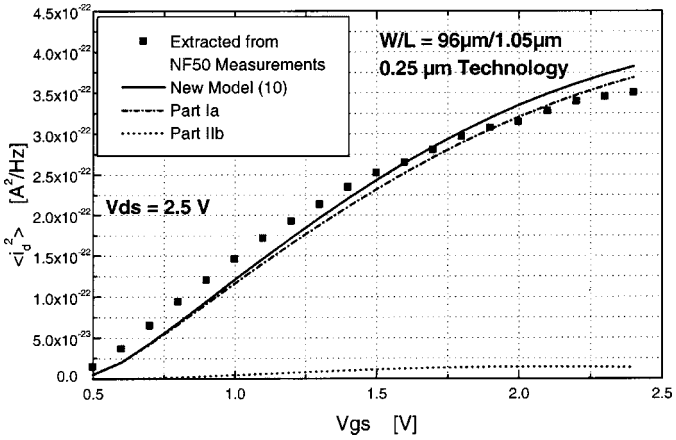


Fig. 9. Comparison between thermal channel noise extracted from NF50 measurements and simulation with (11) for a 1.05-μm nMOS at $V_{ds} = 2.5$ V versus V_{gs}.

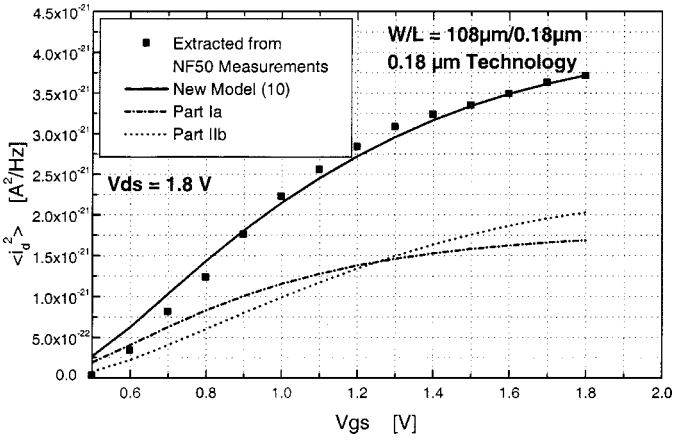
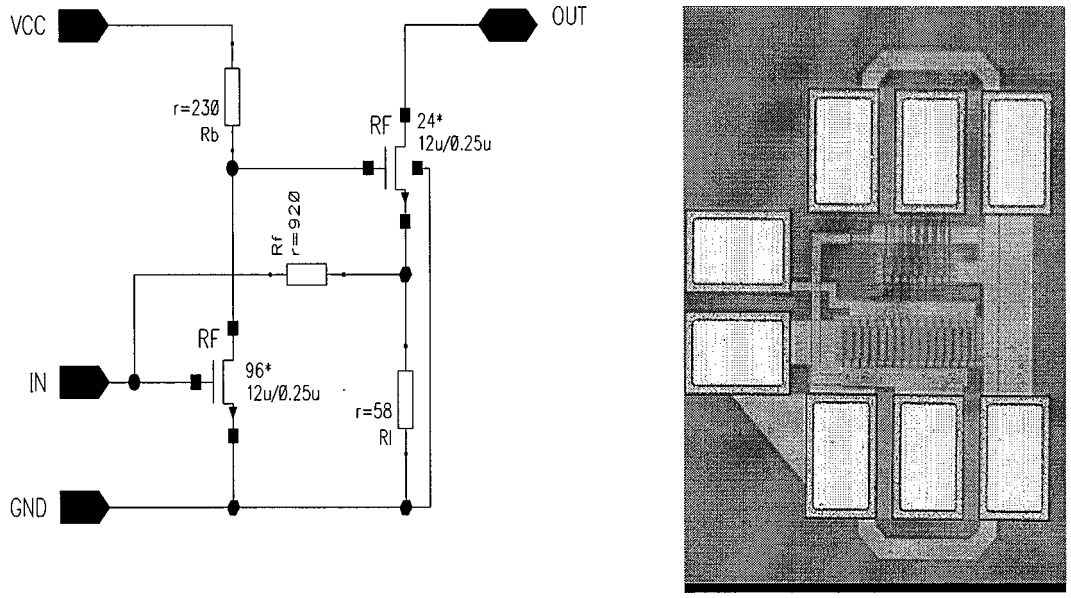
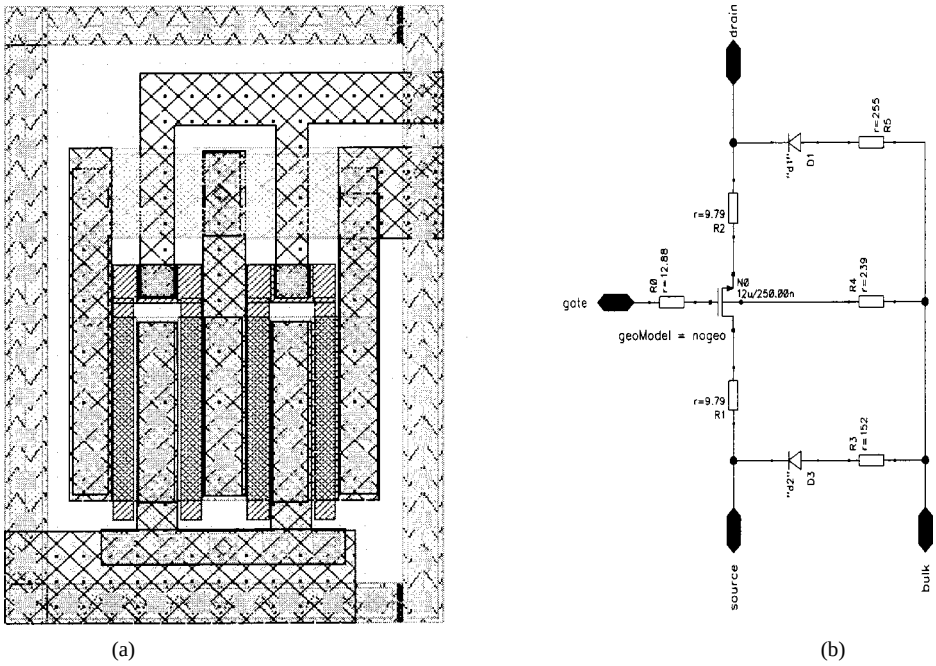


Fig. 10. Comparison between thermal channel noise extracted from NF50 measurements and simulation with (11) for a 0.18-μm nMOS at $V_{ds} = 1.8$ V versus $V_{gs}(\delta = 1.0)$.



(a) (b)

Fig. 11. (a) Schematic and (b) chip photo of the transimpedance LNA.



(a) (b)

Fig. 12. (a) Layout and (b) RF subcircuit model of the 12-μm/0.25-μm standard nMOS cell.

III. Experimental Results

In Fig. 7, measurement and simulation are compared for a 0.25-μm nMOS in the linear region. In this region, the contribution of Part IIb is zero $(\Delta L = 0)$.

In Fig. 8, measurement and simulation are compared for the same transistor at $V_{ds} = 2.5$ V. It can be seen that at this bias condition the contribution of the saturation region is no longer negligible.

With the adjusted δ from the short-channel transistor (Fig. 8) the noise of a long-channel transistor was simulated and plotted in Fig. 9 to show the scalability of the model.

In Fig. 10 measurement and simulation of a 0.18-μm transistor in the saturation region ($V_{ds} = 1.8$ V) are compared.

A comparison of Figs. 8 and 10 shows that the part from the hot carriers in saturation region is rising in comparison to the classical Q_{inv} part.

IV. Application of the New Model In RF-CMOS Design

To verify the noise model, an LNA was designed (Fig. 11) using a set of well-characterized nMOS cells. The nMOS transistors are modeled by the RF subcircuit presented in Fig. 12. This figure also shows that the layout of the 12-μm-wide transistors was folded to reduce gate resistance and drain area. For

TABLE I
MEASURED AND SIMULATED NF50 VALUES OF THE LNA AT $VDD = 2.0$ V

Frequency [GHz]	Measured NF50 [dB]	Simulation with simple Q_{inv} Model (3) [dB]	Simulation with new Model (10) [dB]
1	2.46	1.75	2.42
2	4.20	3.10	4.00

the LNA, a transimpedance topology was chosen for the following reasons:

- Input impedance can be set to nearly 50 Ω, so noise can be measured accurately using a noise-figure meter in a 50-Ω system.
- Gain $|S_{21}|^2$ and input impedance S_{11} fit well between simulation and measurement, the first condition to be met before comparing simulated and measured noise ($|S_{21}|^2$ at 1 GHz: measured $\sim$10 dB, simulated $\sim$11 dB)
- Output noise is dominated by the MOS transistors ($\sim 70\%$ of the spectral noise density of the LNA is from the transistors).

Inductors were not used in order to avoid extra modeling uncertainties in the inductor model.

This LNA was fabricated and measured in Infineon standard 0.25-μm CMOS technology. Measured and simulated NF50 values are presented in Table I.

V. CONCLUSION

We have shown that the conventional models do not accurately predict the thermal channel noise of deep-submicron MOS transistors. Depending on the operating point, the standard g_m model (1) gives spectral noise densities up to a factor 4 lower than the measurement and the Q_{inv} model up to a factor 2.

A new model for thermal channel noise including hot carrier effects has been developed. This new model has been verified with measured data on single transistors and was implemented in the standard BSIM3v3 model.

Furthermore this model has been verified on a RF-CMOS test circuit (LNA) in 0.25-μm technology at 1 and 2 GHz. An excellent agreement between measured and simulated noise performance was achieved.

It was found that considering hot carrier effects is essential for a correct simulation of the noise performance of this RF-CMOS design.

ACKNOWLEDGMENT

The authors would like to thank Dr. U. Baumann from IMMS Ilmenau for making the measurements.

REFERENCES

[1] L. E. Larson, "Integrated circuit technology options for RFICs-present status and future directions," *IEEE J. Solid-State Circuits*, vol. 33, pp. 387–399, Mar. 1998.
[2] A. A. Abidi, "High-frequency noise measurements on FETs with small dimensions," *IEEE Trans. Electron Devices*, vol. ED-33, pp. 1801–1805, Nov. 1986.
[3] R. P. Jindal, "Hot-electron effects on channel thermal noise in file-line nMOS field-effect transistors," *IEEE Trans. Electron Devices*, vol. ED-33, pp. 1395–1397, Sept. 1986.
[4] P. Klein, "An analytical thermal noise model of deep-submicron MOSFETs for circuit simulation with emphasis on the BSIM3v3 SPICE model," in *Proc. ESSDERC*, 1998, pp. 460–463.
[5] S. Tedja *et al.*, "Analytical and experimental studies of thermal noise in MOSFETs," *IEEE Trans. Electron Devices*, vol. 41, pp. 2069–2075, Nov. 1994.
[6] D. Triantis, A. Birbas, and D. Kondis, "Thermal noise modeling for short-channel MOSFETs," *IEEE Trans. Electron Devices*, vol. 43, pp. 1950–1955, Nov. 1996.
[7] Y. P. Tsividis, *Operation and Modeling of the MOS Transistor*. New York: McGraw-Hill, 1988.
[8] D. M. Caughey and R. E. Thomas, "Carrier mobilities in silicon empirically related to doping and field," *Proc. IEEE*, vol. 52, pp. 2192–2193, 1967.
[9] K. Aufinger and J. Böck, "A straightforward noise de-embedding method and its application to high-speed silicon bipolar transistors," in *Proc. ESSDERC*, 1996, pp. 957–960.
[10] G. Knoblinger, P. Klein, and U. Baumann, "Thermal channel noise of quarter and subquarter micron NMOS FETs," in *Proc. ICMTS*, 2000, pp. 95–98.
[11] D. Gasquet, "Noise temperature and hot-carrier thermal conductivity in semiconductors," Ph.D. dissertation, Univ. de Montpellier II, Montpellier, France.
[12] Y. El-Mansy and A. Boothroyd, "A simple two-dimensional model for IGFET operation in the saturation region," *IEEE Trans. Electron Devices*, vol. ED-24, Mar. 1977.
[13] P. K. Ko, R. S. Muller, and C. Hu, "A unified model for the hot-electron currents in MOSFETs," in *IEDM Tech. Dig.*, 1981, pp. 600–603.

Gerhard Knoblinger (M'97) was born in Upper Austria in 1968. He received the Dipl.-Ing. degree in technical physics from the Technical University of Graz, Austria, in 1996.

From 1996 to 1998, he was with the Microelectronics Design Center of Siemens AG Austria, Villach. Since 1998 he has been with the Process and Device Characterization Department in the Semiconductor Group of Siemens AG Germany, now Infineon Technologies. His research interests are high-frequency and noise characterization of deep-submicron CMOS devices. In addition, he is working on the modeling of inductors and varactors and is interested in the design and simulation of RF-CMOS circuits in advanced CMOS technologies.

Peter Klein was born in Bad Aibling, Germany, in 1965. He received the Dipl.-Ing. degree in electrical engineering from the Technical University of Munich, Munich, Germany, in 1992, and the Ph.D. degree from the University of Bundeswehr, Munich, in 1996.

From 1992 to 1995, he was a Research Assistant at the University of Bundeswehr. Since 1995, he has been with Siemens AG Semiconductors, now Infineon Technologies, working on compact CMOS-modeling, simulation, and characterization. Since 2000, he has worked as a Design Engineer on RF-CMOS circuits. He has published over 20 technical papers on device/circuits modeling.

Marc Tiebout (S'90–M'93) was born in Asse, Belgium, in 1969. He received the M.S. degree in electrical and mechanical engineering in 1992 from the Katholieke Universiteit Leuven, Belgium.

In 1992, he joined Siemens AG, Corporate Research and Development, Microelectronics, Munich, Germany. He is currently with Infineon Technologies AG, Wireless Products, a subsidiary of Siemens AG, working on RF CMOS circuits and transceivers for wireless communications.