DESIGN OF A 5.7 GHz 0.18 µm CMOS CURRENT-REUSED LNA FOR AN 802.11A WLAN RECEIVER

This article presents the design, implementation and measurement of a 5.7 GHz CMOS LNA for an IEEE 802.11a WLAN receiver. The LNA, fabricated with the 0.18 µm 1P6M standard CMOS process, uses a current-reuse technology to increase linear gain and save power consumption. The circuit measurements are performed using an FR-4 PCB test fixture. The fabricated LNA exhibits a linear gain of 11.2 dB, a noise figure of 4.5 dB and an input P1dB of –10 dBm at 5.8 GHz. The power consumption is 14.4 mW at V_{DD} = 1.8 V.

Due to the fast growing demand for broadband wireless communications, the operating frequency band is moving toward the 5 GHz U-NII band. The advantage of combining baseband and the RF front-end on one single chip for cost savings is strongly desired for highly integrated systems-on-chip (SoC) applications. Due to the improvements of the standard CMOS process, the unity gain frequency f_T of CMOS devices becomes comparable to that of GaAs. Recently, many RF circuits realized in the CMOS process have been reported and the 0.18 µm process is a good candidate for highly integrated SoC applications.[1] The requirements of low power and low cost push the trend toward the goal of a radio-on-a-chip (RoC).

For an 802.11a WLAN application (5.725 to 5.825 GHz), a proposed heterodyne receiver architecture is shown in ***Figure 1***. The RF (5.725 to 5.825 GHz) is downconverted to an IF of 280 MHz by a first LO (5.445 to 5.545 GHz) and is then further translated to zero by a 280 MHz LO to produce I and Q baseband components. In order to increase the linear gain and save power consumption, a current-reuse technology is adopted[2] instead of a conventional cascode LNA. Two topologies of current-reused LNA have been reported. One is made of inductively degenerated NMOS and PMOS pairs in shunt configuration to achieve current reuse.[2,3] Its linearity is of concern because of the different mobility of NMOS and PMOS devices. The other topology is made of a two-stage, common source amplifier to share the operating current and reduce current consumption.[4,5] In this article, a current-reuse topology consisting of a two-stage, common source amplifier is adopted for the LNA design to share the operating current.[4] The 5.7 GHz LNA is fabricated in a TSMC 0.18 µm standard CMOS process.

LNA TOPOLOGY AND CIRCUIT DESIGN

Figure 2 illustrates the LNA with a current-reuse topology. For the low power consumption requirement, the two-stage amplifier is folded into a single stage. It means that it is cascode for

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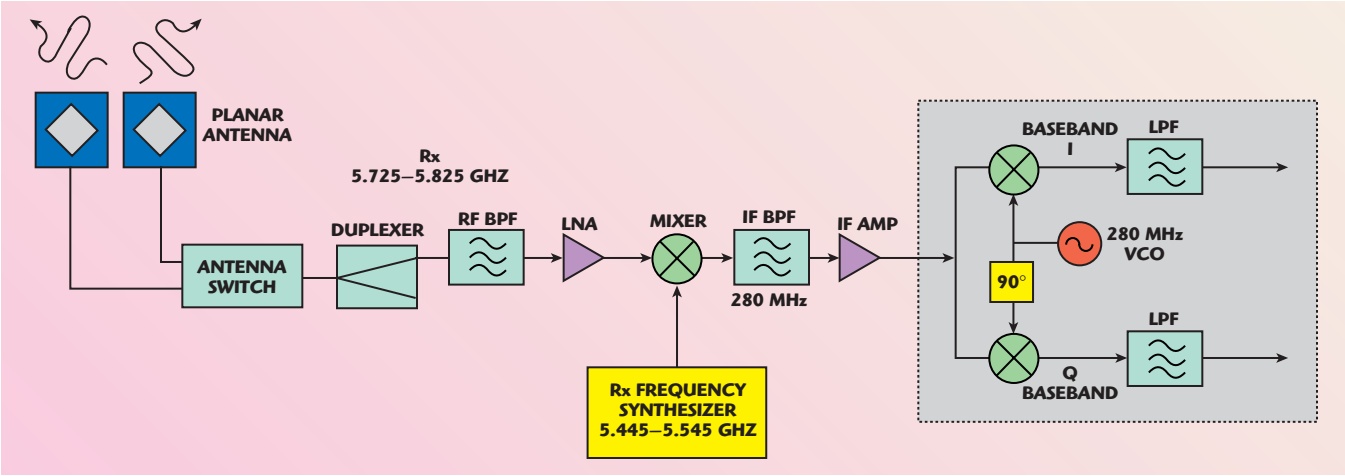

Fig. 1 Proposed 802.11a WLAN receiver architecture.

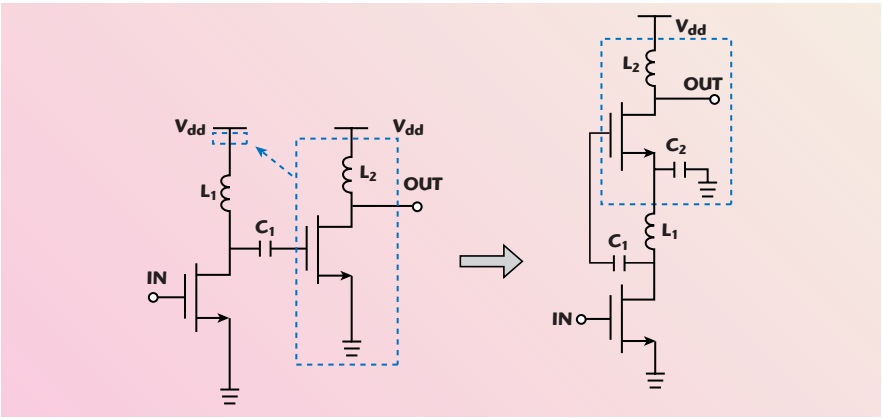

Fig. 2 CMOS LNA with a current-reuse topology.

DC and cascade for RF signals. The two cascading common source amplifiers share the same supply current to reduce power consumption. Hence, with the same gain performance, this circuit only consumes about half the power of the two-stage amplifier. C_1 is a coupling capacitor, L_1 is an RF choke and C_2 is a capacitor providing AC ground. In this topology, the Miller effect is more serious than in a cascode amplifier, since the first common source amplifier has a large voltage gain. This effect can be reduced by inserting an inductor before the gate of the second stage. The input impedance of the LNA is matched to 50 Ω since the bandpass filter (BPF) required in most conventional receiver architectures is in a 50 Ω system. The source degeneration method[6] for input matching is employed and is shown in ***Figure 3***. L_g and L_S can provide a 50 Ω input matching.

The circuit schematic of a 5.7 GHz CMOS LNA is shown in ***Figure 4***. In the CMOS LNA, design considerations include linearity, stability, noise figure, input and output matches, and DC bias. For low power consumption requirements, the DC current is set as low as possible. When the DC operating point is determined, the most important procedure is to choose the optimal NMOS transistor channel width that has the lowest noise figure,[6] and the gate-to-source capac-

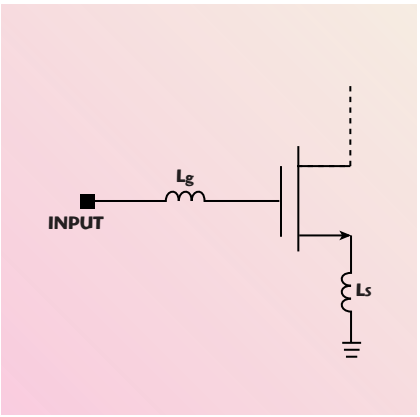

Fig. 3 Source degeneration topology for input matching.

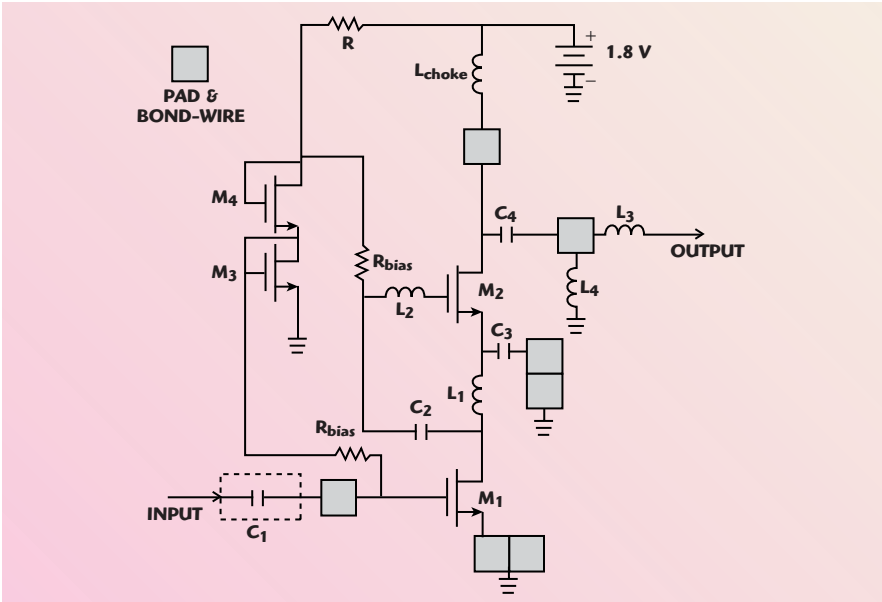

Fig. 4 Schematic of a 5 GHz LNA with current reuse.

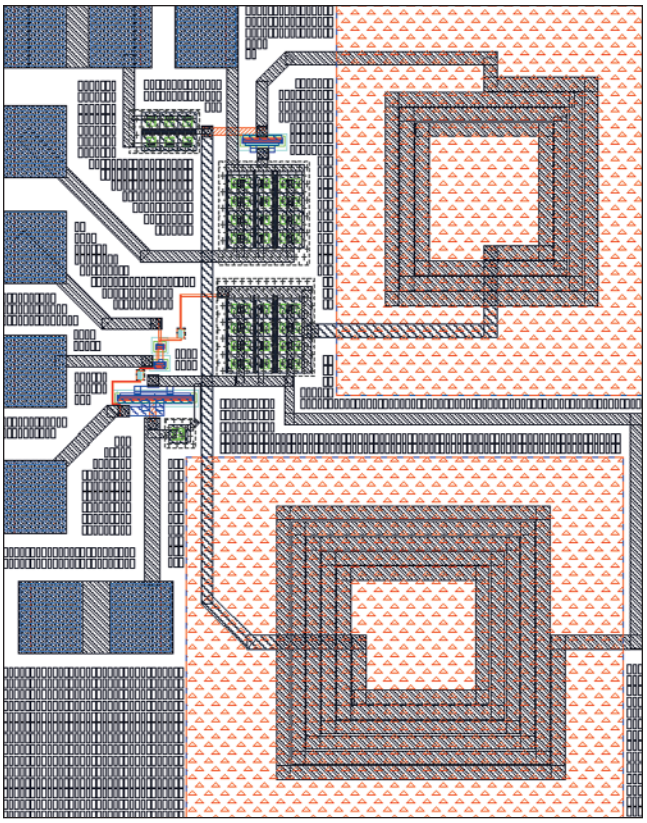

Fig. 5 5.7 GHz CMOS LNA layout.

itance (C_g) can then be derived. While the input impedance is 50 Ω, the inductance of L_g and L_s can be derived as

$$Z_{in} = s(L_s + L_g) + \frac{1}{sC_g} + \left(\frac{g_{m1}}{C_g}\right)L_s \quad (1)$$

$$s(L_s + L_g) + \frac{1}{sC_g} = 0 \quad (2)$$

$$\left(\frac{g_{m1}}{C_g}\right)L_s = 50 \quad (3)$$

where

g_{m1} = transconductance of M_1
C_g = gate-to-source capacitance of M_1
L_g = input inductor of the gate
L_s = source-degeneration inductor

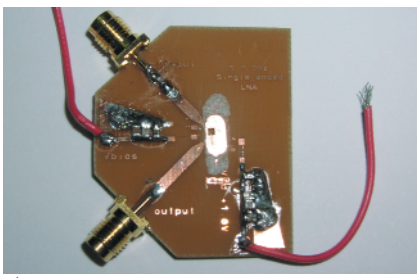

Fig. 6 5.7 GHz CMOS LNA on an FR-4 PCB test fixture.

Since the values of L_g and L_s are not very large, they can be realized by a well-controlled bond-wire with high Q value. An L_s with a high Q value is beneficial to the low noise performance. C_1 is an off-chip DC blocking capacitor. The Q value of an off-chip capacitor is higher than for an on-chip metal-insulator-metal (MIM) capacitor, and the noise figure can be reduced. C_2 and C_3 are coupling capacitors implemented by MIM capacitors. L_1 is an on-chip spiral inductor for an RF choke. L_{choke} is realized by a bond-wire for choking the RF signal. L_2 is an on-chip spiral inductor for inter-stage matching. C_4, L_3 and L_4 form an output matching network, while L_3 and L_4 are realized by well-controlled bond-wires. ***Figure 5*** shows the LNA layout.

MEASURED RESULTS

Agilent Advance Design System (ADS) is used for circuit simulation. The measurements are performed on an FR-4 PCB test fixture, as shown in ***Figure 6***. The LNA chip is connected to the test board with aluminum bond-wires. The equivalent inductance of the bond-wire is approximately 1 nH/mm. The effects of bond-wires and the FR-4 test board have been taken into account in the circuit simulation. The parasitic capacitance to ground is larger than for a conventional test fixture, since the die is mounted on the ground plane directly. By considering this effect, the input and output parasitic capacitance are modeled as 0.1 and 0.2 pF shunted to ground.

The CMOS LNA measurement results are shown in ***Figure 7***. The input and output return losses are approximately 10.5 and 5.6 dB at 5.8 GHz, respectively. The gain is approximately 11.2 dB and the two-tone test shows that the OIP3 is approximately 9.8 dBm. The noise figure is 4.5 dB and the input P1dB is –10 dBm. ***Table 1*** shows the summary of the simulated and measured performance of a 5.7 GHz 0.18 µm CMOS LNA.

CONCLUSION

This article presents the design, implementation and measurement of a 5.7 GHz CMOS LNA for an IEEE 802.11a WLAN receiver application. The LNA with a current-reuse topology to increase linear gain and save power consumption is fabricated in a TSMC 0.18 µm 1P6M CMOS process.

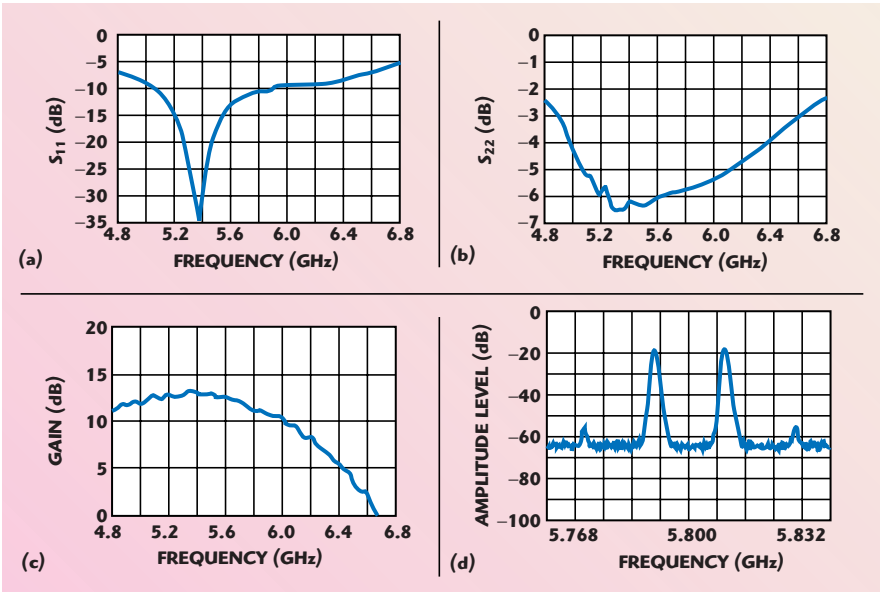

Fig. 7 Measured performance of a 5.7 GHz CMOS LNA with current reuse; (a) input return loss, (b) output return loss, (c) gain and (d) two-tone intermodulation.

TABLE I

SIMULATED AND MEASURED PERFORMANCE OF A 5.7 GHz 0.18 μm CMOS LNA

Frequency Range	5.725 to 5.825 GHz	
	Simulation	Measurement @ 5.8 GHz
DC (V)	+1.8	+1.8
DC current (mA)	7.4	8.0
Input return loss (dB)	11.8	10.5
Output return loss (dB)	29.3	5.6
Gain (dB)	14.1	11.2
Noise figure (dB)	4.8	4.5
Input P1dB (dBm)	–14	–10
OIP3 (dBm)	10.8	9.8

The measurements are performed by using an FR-4 PCB test fixture. The fabricated LNA exhibits a linear gain of 11.2 dB, a noise figure of 4.5 dB, input/output return losses of 10.5 and 5.6 dB, an input P1dB of –10 dBm and an OIP3 of 9.8 dBm at 5.8 GHz. The power consumption is 14.4 mW at V_{DD} = 1.8 V. ■

ACKNOWLEDGMENT

The authors would like to thank the Chip Implementation Center (CIC) of the National Science Council, Taiwan, ROC, for its support of the TSMC CMOS process.

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